# Texas A\&M University Department of Electrical and Computer Engineering 

## ECEN 720 - High -Speed Links

## Spring 2023

## Exam \#1

## Instructor: Sam Palermo

- Please write your name in the space provided below
- Please verify that there are 7 pages in your exam
- Good Luck!

| Problem | Score | Max Score |
| :---: | :---: | :---: |
| 1 |  | 30 |
| 2 |  | 20 |
| 3 |  | 25 |
| 4 |  | 25 |
| Total |  | $\mathbf{1 0 0}$ |

Name: $\qquad$ PALERMO

UN:

## Problem 1 (30 points)

a) A 1 V step is launched onto the channel below at $\mathrm{t}=0 \mathrm{~ns}$. ( 20 points)
i. Calculate the reflection coefficient at the source, $\mathrm{k}_{\mathrm{r}}$, at the middle point for right traveling signals, $\mathrm{k}_{\mathrm{r}, \mathrm{R}, \mathrm{R}}$, and left traveling signals, $\mathrm{k}_{\mathrm{r} M, \mathrm{~L}}$, and the end termination, $\mathrm{k}_{\mathrm{r} T}$
ii. Fill in the lattice diagram below until $\mathrm{t}=4 \mathrm{~ns}$.
iii. Also plot the source voltage, $\mathrm{V}_{\mathrm{S}}$, and the termination voltage, $\mathrm{V}_{\mathrm{T}}$ until 4 ns .


$$
\begin{aligned}
& k_{r S}=\frac{30-60}{30+60}=-\frac{1}{3} \\
& k_{r_{M, L}}=\frac{60-70}{60+70}=-\frac{1}{13} \\
& k_{m, R}=\frac{70-60}{70+60}=\frac{1}{13} \\
& k_{r_{T}}=\frac{40-70}{40+70}=-\frac{3}{11}
\end{aligned}
$$

$$
I_{\text {riitial Voltage }}=\frac{60}{30+60}(1 V)=667 \mathrm{mV}
$$


b) For the circuit below, design a three-terminal resistive matching network to eliminate any reflections in any direction and make $\mathrm{V}_{\mathrm{OI}}=\mathrm{V}_{\mathrm{O} 2}$. If a 1 V step is launched onto the network, what is the step value at the two outputs? ( 10 points)


$$
R=16.71
$$

Equivalent Circuit


$$
V_{0_{1}}=V_{02}=\frac{\left(\frac{50}{50+50 / 9}\right)\left(\frac{50+50 / 3}{2}\right)}{50+\frac{50}{3}+\frac{50+50 / 3}{2}}=0.25 \mathrm{~V}
$$

$$
V_{01}=V_{01}=V_{02}=\frac{\left(\frac{50}{50+50}\right)\left(\frac{50+50}{2}\right)}{50+\frac{50+50}{2}}=0.25 \mathrm{~V}
$$

Problem 2 (20 points)
A channel has the pulse response, $y^{(1)}$, below for a " 1 " bit.
a. Find the channel's worst-case eye height at this bit rate.
b. Give the channel's worst-case bit pattern at this bit rate.

$$
\begin{aligned}
& y^{(1)}=\left[\begin{array}{lllll}
0.1 & 0.7 & -0.05 & 0.2 & 0.05
\end{array}\right] \\
& \prod_{1}^{v .7} \begin{array}{l}
y_{0}{ }^{(1)}=0.7 \\
\left.\sum_{k \neq 0}{ }_{\gamma}^{(1)}\right|_{y<0}=-0.05
\end{array} \\
& \begin{aligned}
\left.\sum_{x \neq 0} y^{(x)}\right|_{y>0} & =0.1+0.2+0.05 \\
& =0.35
\end{aligned}
\end{aligned}
$$

Problem 3 (25 points)
Answer the following questions for the pull-only, differential current-mode driver shown below.

a. What is the peak-to-peak differential output swing, $\mathrm{V}_{\mathrm{d}, 1}-\mathrm{V}_{\mathrm{d}, 0}$ ?
b. What is the average power consumption of the driver?

$$
\begin{aligned}
& V_{d, 1}-V_{d, 0}=I R-(-I R)=2 I R=2(5 \mathrm{~mA})(50 \Omega)=50 \mathrm{~m}^{\prime} \mathrm{V} \\
& V_{\mathrm{out}, \mathrm{dpp}}=V_{\mathrm{d}, 1}-V_{d, 0}=500 \mathrm{ml}
\end{aligned}
$$

Now consider the push-pull differential current-mode driver shown below. Note that the bias current has been reduced from 5 mA to 2.5 mA .


$$
\begin{aligned}
& V_{U_{1},}-V_{d, 0}= \\
& 2 I R-(-2 I R)=4 I R \\
&= 4(2,-n A)(500)=500 \mathrm{~m}
\end{aligned}
$$

c. What is the peak-to-peak differential output swing, $\mathrm{V}_{\mathrm{d}, \mathrm{l}}-\mathrm{V}_{\mathrm{d}, 0}$ ?
d. What is the average power consumption of the driver?

$$
P_{a v g}=2.5 \mathrm{~m} A((V)=2.5 \operatorname{si} W
$$

$$
\begin{aligned}
\mathrm{V}_{\text {out, dep }}=\mathrm{V}_{\mathrm{d}, 1}-\mathrm{V}_{\mathrm{d} .0} & =500 \mathrm{ml} \\
\text { Average Power } & =2.5 \mathrm{ma}
\end{aligned}
$$

e. Why doesn't this push-pull driver dissipate half the power of the pull-only driver, for the same signal swing? In particular, explain the factor that constrains the supply voltage (1V) or the termination voltage $(0.5 \mathrm{~V})$.

For the push-pull driver, we need both the top (emos) and the bottom (NMOS) current sources to stay in saturation.

Thus, we need about twice the supply voltage.

Problem 4 (25 points)
The NMOS sampler below is used to sample a 5 GHz sinusoidal signal at $\mathrm{t}=0$. Assume that the sampler displays the triangular sampling function, $\mathrm{h}(\mathrm{t})$.
i. Setup, but do not calculate, the integral expression for the sampled output voltage.
ii. Calculate the sampler aperture time from the sampling function. Assume that the aperture time is defined as the time where $80 \%$ of the sampler sensitivity is confined.


## Key MOS Equations \& Scratch Paper



Saturation: $N M O S I_{D S}=\frac{1}{2} K P_{N} \frac{W}{L}\left(V_{G S}-V_{T N}\right)^{2}$
Saturation: $P M O S I_{S D}=\frac{1}{2} K P_{P} \frac{W}{L}\left(V_{S G}-\left|V_{T P}\right|\right)^{2}$
Triode: NMOS $I_{D S}=K P_{N} \frac{W}{L}\left(V_{G S}-V_{T N}-\frac{V_{D S}}{2}\right) V_{D S}$
Triode: PMOS $I_{S D}=K P_{P} \frac{W}{L}\left(V_{S G}-\left|V_{T P}\right|-\frac{V_{S D}}{2}\right) V_{S D}$

$$
\text { NMOS } g_{m}=\frac{\partial I_{D S}}{\partial V_{G S}}, \text { PMOS } g_{m}=\frac{\partial I_{S D}}{\partial V_{S G}}
$$

NMOS $g_{o}=\frac{\partial I_{D S}}{\partial V_{D S}}, \quad$ PMOS $g_{o}=\frac{\partial I_{S D}}{\partial V_{S D}}$

