Texas A&M University
Department of Electrical and Computer Engineering

ECEN 720 – High-Speed Links

Spring 2017

Exam #1

Instructor: Sam Palermo

- Please write your name in the space provided below
- Please verify that there are **6** pages in your exam
- You may use one double-sided page of notes and equations for the exam
- Good Luck!

Problem	Score	Max Score
1		30
2		20
3		20
4		30
Total		**100**

Name: SAM PALERMO

UIN:

Problem 1 (30 points)

a) A 1V step is launched onto the channel below at t=0ns. (20 points)

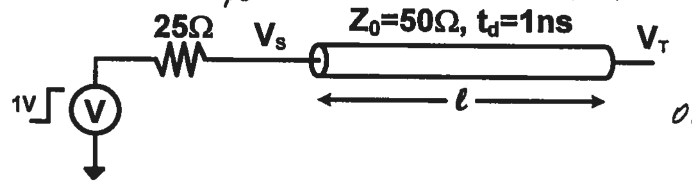
i. Calculate the reflection coefficient at the source, k_{rS}, and at the end termination, k_{rT}

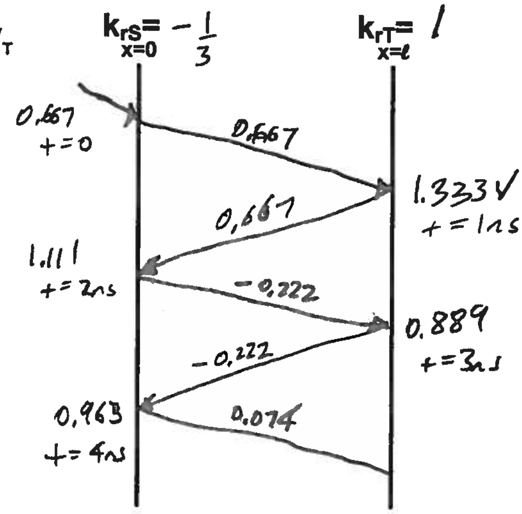
ii. Fill in the lattice diagram below until the source voltage, V_S, has reached to within 100mV of its final value.

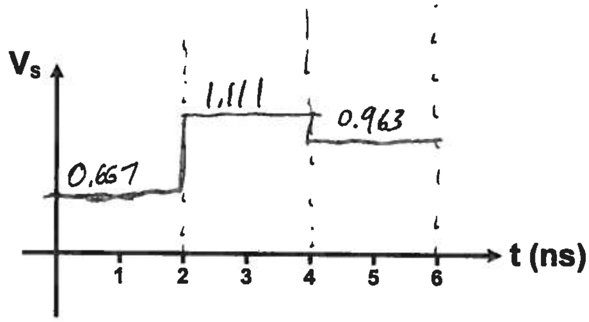
iii. Also plot the source voltage, V_S, and make sure to label the voltage values in the transient plot.

Open Termination ⟹ Final V_s should be 1V

Initial Voltage $= \frac{50}{75} = 0.667$

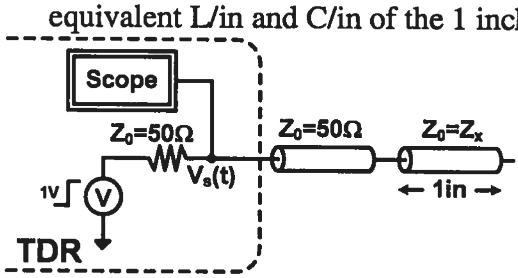


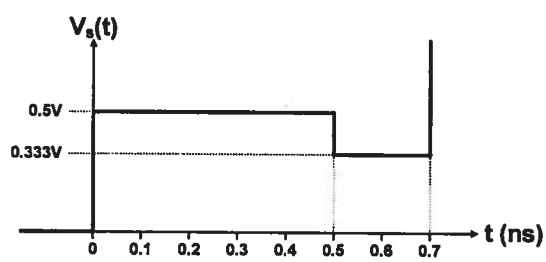




$$K_{rS} = \frac{Z_S - Z_o}{Z_S + Z_o} = \frac{25-50}{25+50} = -\frac{1}{3} \qquad K_{rT} = \frac{Z_T - Z_o}{Z_T + Z_o} = \frac{\infty - 50}{\infty + 5} = +1$$

b) An ideal TDR (t_r~0) yields the following response with a channel consisting of a 50Ω trace, a 1 inch trace with Z_x impedance, and ends in an open termination. Calculate Z_x and the equivalent L/in and C/in of the 1 inch trace. Assume all traces are loss-less. (15 points)





Z_x impedance discontinuity is detected at TDR at t = 0.5ns

$$Z_x = Z_o\left(\frac{V(0.5ns)}{1V - V(0.5ns)}\right) = 50\Omega\left(\frac{0.333}{1-0.333}\right) = 25\Omega$$

$$Z_x = \sqrt{\frac{L}{C}}$$

$$t_d = \frac{1}{v} = \sqrt{LC} = \frac{200ps}{2(1in)} = 100\frac{ps}{in}$$

$$\frac{L}{in} = Z_x t_d = \sqrt{\frac{L}{C}}\sqrt{LC} = (25\Omega)(100\frac{ps}{in}) = 2.5\frac{nH}{in}$$

$$C = \frac{L}{Z_x^2} = \frac{2.5nH/in}{(25\Omega)^2} = 4\frac{pF}{in}$$

Z_x = 25Ω

L/in = $2.5\frac{nH}{in}$

C/in = $4\frac{pF}{in}$

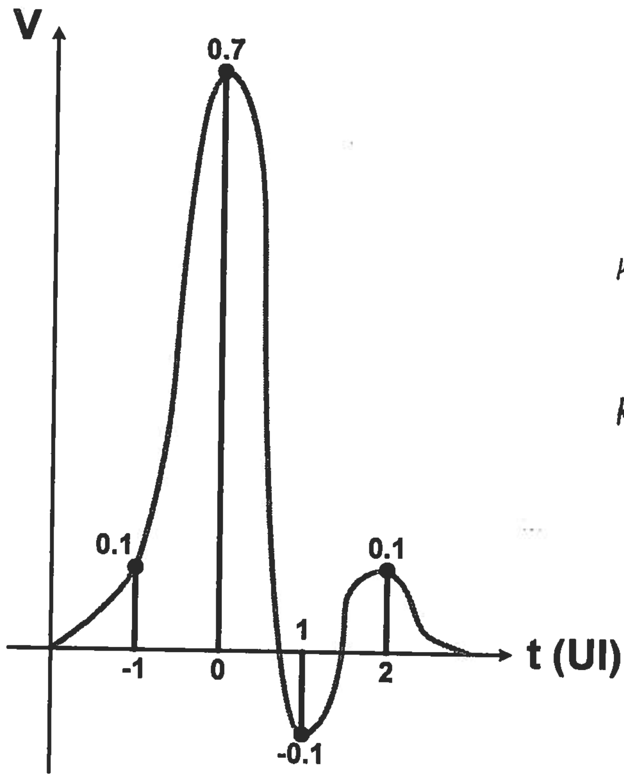
Problem 2 (20 points)

A channel has the pulse response, $y^{(1)}$, below for a "1" bit.

a. Find the channel's worst-case eye height at this bit rate.

b. Give the channel's worst-case bit pattern at this bit rate. Make sure to label the cursor in the bit pattern.

$$y^{(1)} = [0.1 \;\; 0.7 \;\; -0.1 \;\; 0.1]$$



$$y_0^{(1)} = 0.7$$

$$\sum_{k \neq 0} y_k^{(1)} \Big|_{y<0} = -0.1$$

$$\sum_{k \neq 0} y_k^{(1)} \Big|_{y>0} = 0.1 + 0.1 = 0.2$$

W.C. Eye Height $= 2(0.7 - 0.1 - 0.2) = 0.8$

To find W.C. Bit Pattern: Flip around cursor and invert all but cursor

$[0.1 \;\; 0.7 \;\; -0.1 \;\; 0.1] \Rightarrow [-0.1 \;\; +0.1 \;\; 0.7 \;\; -0.1]$

Then take sign

$[-0.1 \;\; +0.1 \;\; 0.7 \;\; -0.1] \Rightarrow [-1 \;\; 1 \;\; 1 \;\; -1]$

Worst-Case Eye Height = 0.8

Cursors

Worst-Case Bit Pattern = $[-1 \;\; 1 \;\; 1 \;\; -1]$ (Worst-Case "1")

$[1 \;\; -1 \;\; -1 \;\; 1]$ (Worst-Case "-1")

by linearity

Problem 3 (20 points)

For the circuit below, use the following NMOS parameters

$KP_N=\mu_n C_{ox}=600\mu A/V^2$, $V_{TN}=0.35V$, $\lambda_N=0V^{-1}$

and the following PMOS parameters

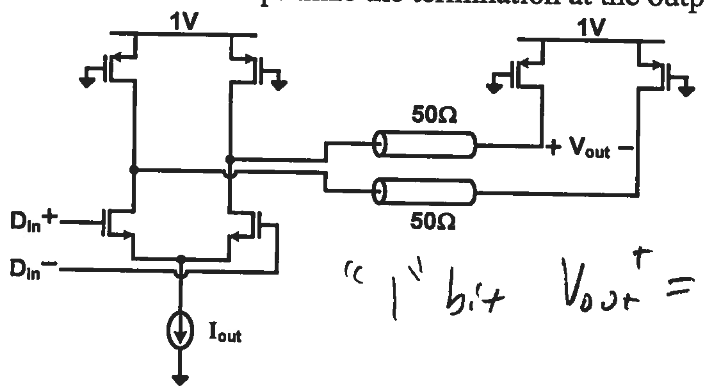
$KP_P=\mu_p C_{ox}=150\mu A/V^2$, $V_{TP}=-0.35V$, $\lambda_P=0V^{-1}$

For the current-mode driver below

i. Calculate the tail current I_{out} to generate a peak-to-peak differential voltage output swing of $700mV_{ppd}$.

ii. Give the common-mode value of the output voltage with the $700mV_{ppd}$ output swing.

iii. Give the PMOS termination transistors aspect ratios for proper termination. Include V_{SD} effects and optimize the termination at the output common-mode level.



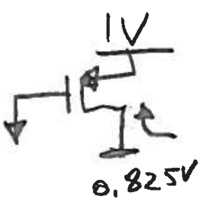
$I_{out} = \frac{V_{ppd}}{R} = \frac{700mV}{50\Omega} = 14m$

"1" bit $V_{out}^{+} = 1V$ $V_{out}^{-} = 1V - 7mA(50\Omega) = 0.65V$

"-1" bit $V_{out}^{+} = 0.65V$ $V_{out}^{-} = 1V$

$V_{out,CM} = \frac{1+0.65}{2} = 0.825V$

* Sizing PMOS termination at common-mode level



$R_p = \frac{1}{g_o} = \frac{1}{KP_p \frac{W}{L}(V_{SG} - |V_{TP}| - V_{SD})}$

$\frac{W}{L} = \frac{1}{R_p KP_p (V_{SG} - |V_{TP}| - V_{SD})} = \frac{1}{(50\Omega)(150\mu A/V^2)(1V - 0.35V - 0.175V)}$

$I_{out} =$ 14mA

$V_{out,CM} =$ 0.825V

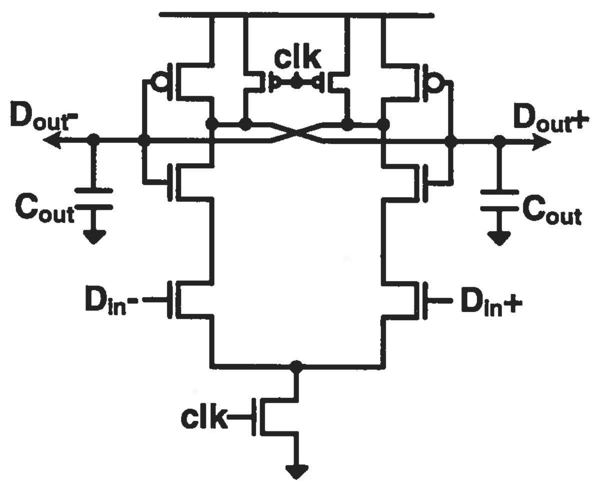
$(W/L)_P =$ 281

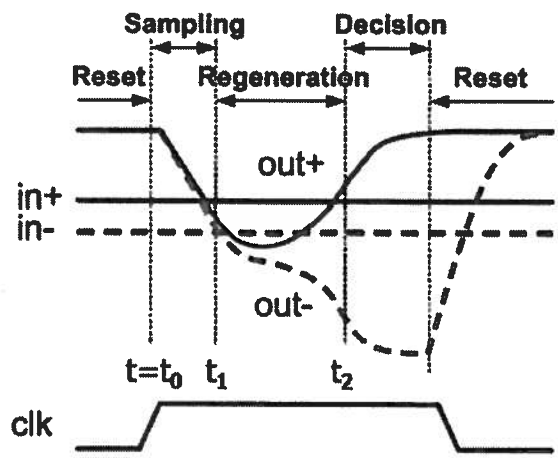
Problem 4 (30 points)

This problem involves analyzing the maximum performance of the comparator below. Assume that the **Sample Time=25ps** and the **Sample Gain=2.**

i. If the regeneration time constant τ_R=15ps and it is required to amplify a 10mV differential input voltage to 500mV for a reliable decision, what is the minimum time required to make a decision ($t_2 - t_0$)?

ii. Given the effective total regeneration transconductance g_{mr}=500µA/V, what is the maximum total output capacitance that the comparator can drive and maintain the 15ps τ_R?





Sample Gain = 2 ⇒ Need to amplify 10mV(2) = 20mV to 500mV ⇒ Need a regeneration time

$$\tau_R \ln(G_R) = 15ps \ln\left(\frac{500mV}{20mV}\right) = 48.3ps$$

Decision Time = Sample Time + Regeneration Time

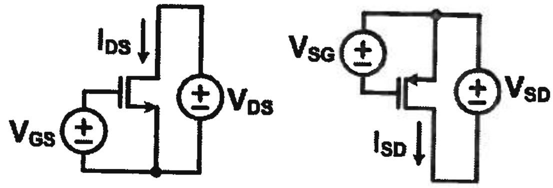
$$= 25ps + 48.3ps = 73.3ps$$

$$\text{Max } C_{out} = g_m \tau_R = (500\mu A/V)(15ps) = 7.5fF$$

Min ($t_2 - t_0$) = 73.3ps

Max C_{out} = 7.5fF

Key MOS Equations & Scratch Paper



Saturation: $NMOS\ I_{DS} = \frac{1}{2} KP_N \frac{W}{L} (V_{GS} - V_{TN})^2$

Saturation: $PMOS\ I_{SD} = \frac{1}{2} KP_P \frac{W}{L} (V_{SG} - |V_{TP}|)^2$

Triode: NMOS $I_{DS} = KP_N \frac{W}{L} \left(V_{GS} - V_{TN} - \frac{V_{DS}}{2}\right) V_{DS}$

Triode: $PMOS\ I_{SD} = KP_P \frac{W}{L} \left(V_{SG} - |V_{TP}| - \frac{V_{SD}}{2}\right) V_{SD}$

$$NMOS\ g_m = \frac{\partial I_{DS}}{\partial V_{GS}},\quad PMOS\ g_m = \frac{\partial I_{SD}}{\partial V_{SG}}$$

$$NMOS\ g_o = \frac{\partial I_{DS}}{\partial V_{DS}},\quad PMOS\ g_o = \frac{\partial I_{SD}}{\partial V_{SD}}$$