Texas A&M University
Department of Electrical and Computer Engineering

ECEN 720 – High-Speed Links

Spring 2015

Exam #1

Instructor: Sam Palermo

- Please write your name in the space provided below
- Please verify that there are **7** pages in your exam
- You may use one double-sided page of notes and equations for the exam
- Good Luck!

Problem	Score	Max Score
1		30
2		20
3		10
4		15
5		25
Total		**100**

Name: SAM PALERMO

UIN:

Problem 1 (30 points)

a) A 1V step is launched onto the channel below at t=0ns. (20 points)

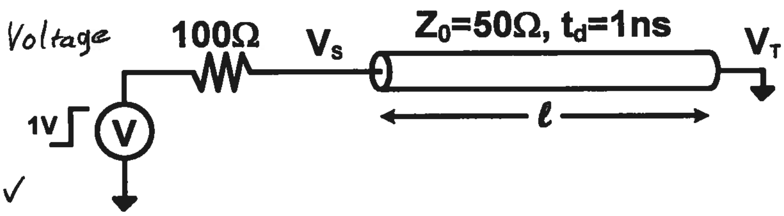
i. Calculate the reflection coefficient at the source, k_{rS}, and at the end termination, k_{rT}

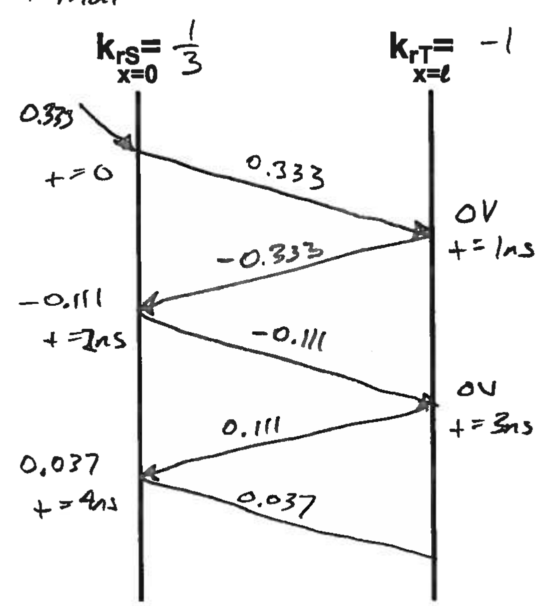
ii. Fill in the lattice diagram below until the source voltage, V_S, has reached to within 100mV of its final value.

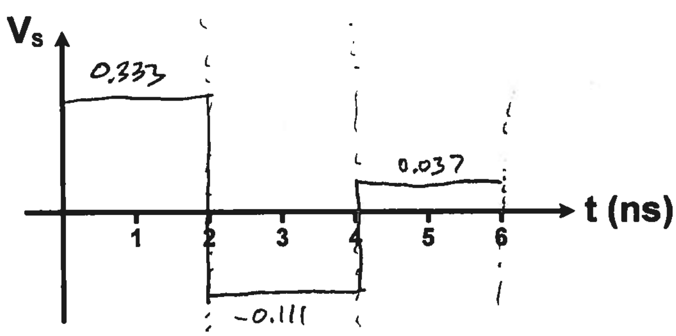
iii. Also plot the source voltage, V_S, and make sure to label the voltage values in the transient plot.

Source shorted to GND ⟹ Final V_S should be 0V

Initial Voltage $= \frac{50}{150} = 0.333V$

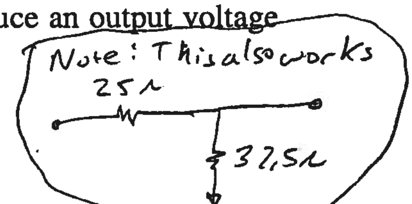


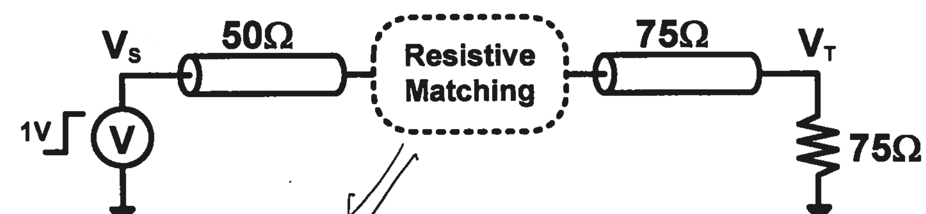


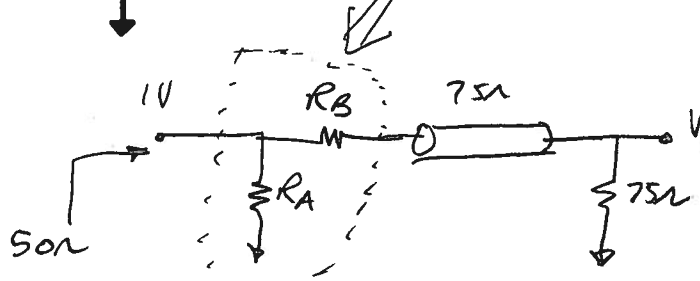


$$K_{rS} = \frac{Z_S - Z_0}{Z_S + Z_0} = \frac{100-50}{100+50} = \frac{1}{3} \qquad K_{rT} = \frac{Z_T - Z_0}{Z_T + Z_0} = \frac{0-50}{0+50} = -1$$

b) For the circuit below, design a resistive matching network to eliminate any reflections of the forward traveling wave originating from the source, V_S, and also produce an output voltage V_T=0.5V with a 1V input step. (10 points)







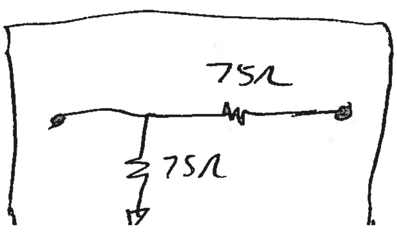
* To make $V_T = 0.5V$

$\Rightarrow R_B = 75\Omega$

* To satisfy no reflections

$$R_A \| (R_B + 75) = 50$$

$$\frac{R_A (150)}{R_A + 150} = 50 \Rightarrow R_A = 75\Omega$$



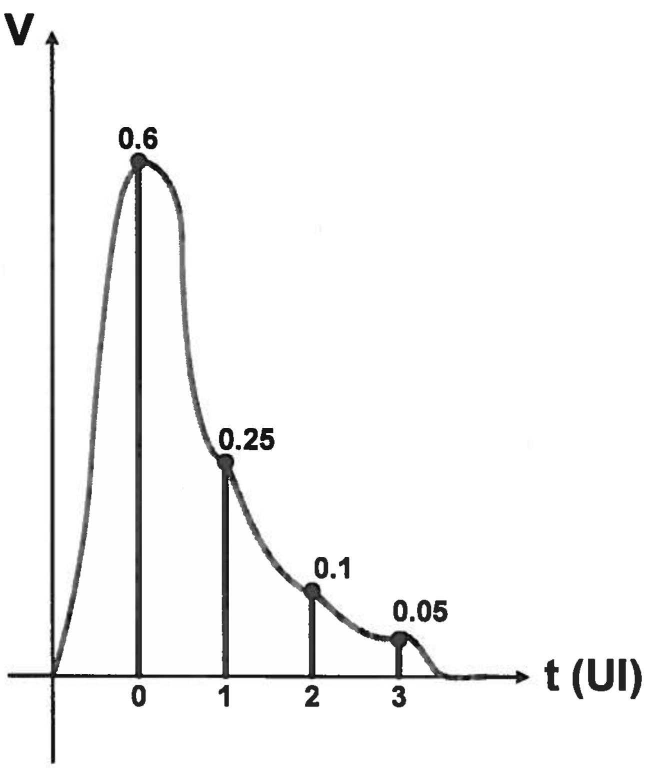
Problem 2 (20 points)

A channel has the pulse response, $y^{(1)}$, below for a "1" bit.

a. Find the channel's worst-case eye height at this bit rate.

b. Give the channel's worst-case bit pattern at this bit rate. Make sure to label the cursor in the bit pattern.

$$y^{(1)} = [0.6\ \ 0.25\ \ 0.1\ \ 0.05]$$



$y_0^{(1)} = 0.6$

$\sum_{k\neq 0} y_k^{(1)} \Big|_{y<0} = \phi$

$\sum_{k\neq 0} y_k^{(1)} \Big|_{y>0} = 0.25 + 0.1 + 0.05 = 0.4$

W.C. Eye Height $= 2(0.6 - 0.4) = 0.4$

To find W.C. Bit Pattern: Flip about cursor and invert all but cursor

$[0.6\ \ 0.25\ \ 0.1\ \ 0.05] \Rightarrow [-0.05\ \ -0.1\ \ -0.25\ \ 0.6]$

Then take sign

$[-0.05\ \ -0.1\ \ -0.25\ \ 0.6] \Rightarrow [-1\ \ -1\ \ -1\ \ 1]$

Worst-Case Eye Height = 0.4

Cursors

Worst-Case Bit Pattern = $[-1\ \ -1\ \ -1\ \ 1]$ (Worst-Case "1")

$[1\ \ 1\ \ 1\ \ -1]$ (Worst-Case "-1") by linearity

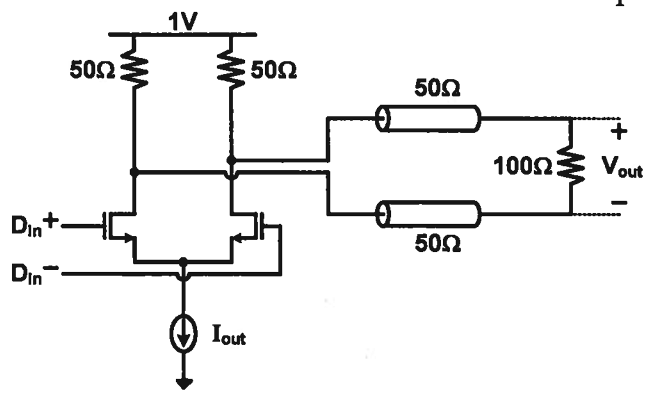
3

Problem 3 (10 points)

Answer the following questions for the current-mode driver below

i. Calculate the tail current I_{out} to generate a peak-to-peak differential voltage output swing of $0.6V_{ppd}$.

ii. Give the common-mode value of the output voltage with the $0.6V_{ppd}$ output swing.



$$I_{OUT} = \frac{V_{ppd}}{R} = \frac{0.6V}{50\Omega} = 12mA$$

During "1" bit $V_{OUT}^{+} = 0.85V$ $V_{OUT}^{-} = 0.55V$

"−1" bit $V_{OUT}^{+} = 0.55V$ $V_{OUT}^{-} = 0.85V$

$$V_{OUT,CM} = \frac{0.85+0.55}{2} = 0.7V$$

I_{out} = 12mA

$V_{out,CM}$ = 0.7V

Problem 4 (15 points)

For the circuit below, use the following NMOS parameters

$KP_N=\mu_n C_{ox}=600\mu A/V^2$, $V_{TN}=0.35V$, $\lambda_N=0V^{-1}$

and the following PMOS parameters

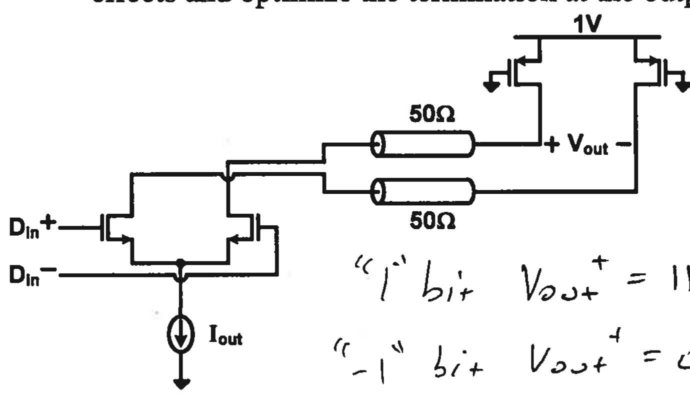
$KP_P=\mu_p C_{ox}=150\mu A/V^2$, $V_{TP}=-0.35V$, $\lambda_P=0V^{-1}$

For the current-mode driver below

i. Calculate the tail current I_{out} to generate a peak-to-peak differential voltage output swing of $600mV_{ppd}$.

ii. Give the common-mode value of the output voltage with the $600mV_{ppd}$ output swing.

iii. Give the PMOS termination transistors aspect ratios for proper termination. Include V_{SD} effects and optimize the termination at the output common-mode level.



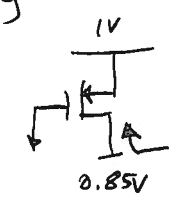
$$I_{OUT} = \frac{V_{ppd}}{2R} = \frac{600mV}{2(50\Omega)} = 6mA$$

"1" bit $V_{out}^+ = 1V$ $V_{out}^- = 1V - 6mA(50\Omega) = 0.7V$

"−1" bit $V_{out}^+ = 0.7V$ $V_{out}^- = 1V$

$$V_{out,CM} = \frac{1+0.7}{2} = 0.85V$$

* Sizing PMOS termination at common-mode level



Looking into drain of PMOS in deep triode

$$R_p = \frac{1}{g_o} = \frac{1}{KP_p \frac{W}{L}(V_{SG}-|V_{TP}|-V_{SD})}$$

$$\frac{W}{L} = \frac{1}{R_p KP_p (V_{SG}-|V_{TP}|-V_{SD})} = \frac{1}{(50\Omega)(150\mu A/V^2)(1V-0.35V-0.15V)} = 267$$

I_{out} = 6mA

$V_{out,CM}$ = 0.85V

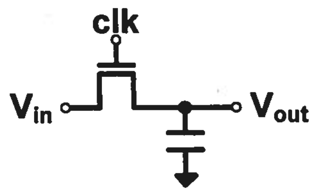
$(W/L)_P$ = 267

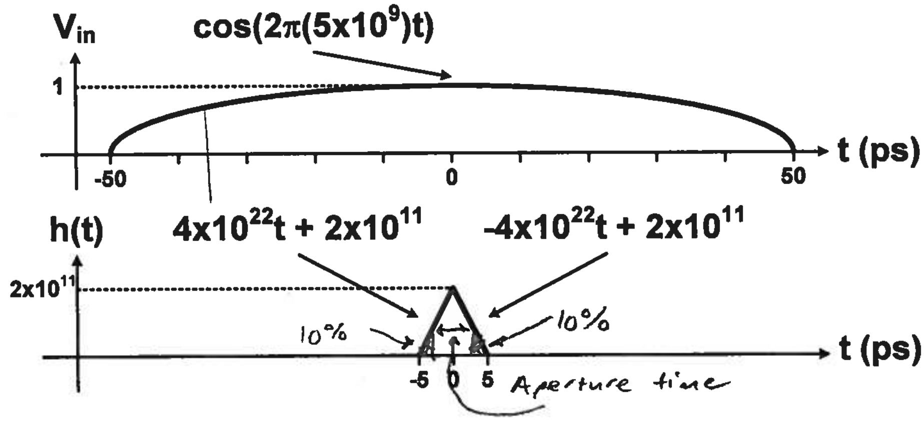
Problem 5 (25 points)

The NMOS sampler below is used to sample a 5GHz sinusoidal signal at t=0. Assume that the sampler displays the triangular sampling function, h(t).

i. Setup, **but do not calculate**, the integral expression for the sampled output voltage.

ii. Calculate the sampler aperture time from the sampling function. Assume that the aperture time is defined as the time where 80% of the sampler sensitivity is confined.





i. Sampled $V_{OUT} = \int_{-\infty}^{\infty} V_{in}(t)\,h(t)\,dt$

$$= \int_{-5ps}^{0} \cos\left(2\pi(5\times10^9)t\right)\left[4\times10^{22}t + 2\times10^{11}\right]dt + \int_{0}^{5ps} \cos\left(2\pi(5\times10^9)t\right)\left[-4\times10^{22}t + 2\times10^{11}\right]dt$$

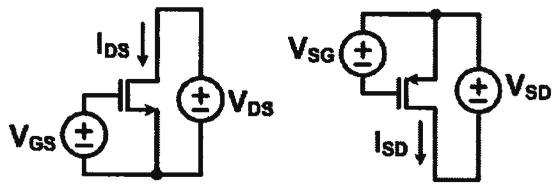
ii. Need to find how much time = 10% of area of 0.1 because

$$\int_{-\infty}^{\infty} h(t) = 1$$

($4\times10^{22}t$, t) Area $= 0.1 \Rightarrow \frac{1}{2}\left(4\times10^{22}t\right)(t) = 0.1 \Rightarrow t = 2.24ps$ for 10% area

Aperture time $= 10ps - 2(2.24ps) = 5.53ps$

Key MOS Equations & Scratch Paper



$$\text{Saturation: } NMOS\ \ I_{DS} = \frac{1}{2} KP_N \frac{W}{L} (V_{GS} - V_{TN})^2$$

$$\text{Saturation: } PMOS\ \ I_{SD} = \frac{1}{2} KP_P \frac{W}{L} (V_{SG} - |V_{TP}|)^2$$

$$\text{Triode: NMOS } I_{DS} = KP_N \frac{W}{L} \left(V_{GS} - V_{TN} - \frac{V_{DS}}{2} \right) V_{DS}$$

$$\text{Triode: } PMOS\ I_{SD} = KP_P \frac{W}{L} \left(V_{SG} - |V_{TP}| - \frac{V_{SD}}{2} \right) V_{SD}$$

$$NMOS\ g_m = \frac{\partial I_{DS}}{\partial V_{GS}}, \quad PMOS\ g_m = \frac{\partial I_{SD}}{\partial V_{SG}}$$

$$NMOS\ \ g_o = \frac{\partial I_{DS}}{\partial V_{DS}}, \quad PMOS\ \ g_o = \frac{\partial I_{SD}}{\partial V_{SD}}$$