ECEN 720: High-Speed Links

Final Project

Instructor: Sam Palermo

Project teams can consist of 1-3 students.

Project Topics

Project #1 – Voltage-Mode Transmitter with High-Resolution Equalization

The objective of this project is to design a voltage-mode transmitter with 3-tap FIR equalization at 6-bit resolution. The driver can either be a low-swing version ($V_{out} \le 400 \text{mV}_{ppd}$) or a high-swing version ($V_{out} \ge 800 \text{mV}_{ppd}$). Design the transmitter to operate at maximum data rate of 10Gb/s. Quantify the maximum data rate you can achieve over the B1, C4, and T20 channels assuming a receiver sensitivity of 20mV_{ppd} and 0.3UI timing margin at a BER=10⁻¹².

Key References:

- [1] H. Hatamkhani *et al.*, "A 10mW 3.6Gbps I/O Transmitter," *IEEE Symposium on VLSI Circuits*, June 2003.
- [2] W. Dettloff *et al.*, "A 32mW 7.4Gb/s Protocol-Agile Source-Series Terminated Transmitter in 45nm CMOS SOI," *IEEE International Solid-State Circuits Conference*, Feb. 2010.
- [3] R. Sredojevic and V. Stojanovic, "Digital Link Pre-emphasis with Dynamic Driver Impedance Modulation," *IEEE Custom Integrated Circuits Conference*, Sept. 2010.

Project #2 – DFE-IIR Equalization

The objective of this project is to design a 10Gb/s DFE with a combination of FIR and IIR feedback filtering. Optimize the FIR tap number and IIR filter response to (attempt to) achieve 10Gb/s operation over the B1, C4, and T20 channels assuming a receiver sensitivity of 20mVppd and 0.3UI timing margin at a BER=10⁻¹². Quantify the performance impact of including the IIR feedback filter versus only using an FIR feedback filter.

Key References:

- [1] B. Kim *et al.*, "A 10Gb/s Compact Low-Power Serial I/O with DFE-IIR Equalization in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, Dec. 2009, pp. 3526-3538.
- [2] Y.-C. Huang and S.-I. Liu, "A 6Gb/s Receiver with 32.7dB Adaptive DFE-IIR Equalization," *IEEE International Solid-State Circuits Conference*, Feb. 2011.

Project #3 – TX Clock Generation, Distribution, and Local Clocking

The objective of this project is to design/model a global clock generation PLL and distribution network to support 20 transmit channels operating at 10Gb/s. A jitter budget for the transmit clocking network should be produced to allow 10Gb/s operation over the T20 channel assuming a receiver sensitivity of $20mV_{ppd}$ and 0.3UI timing margin at a BER= 10^{-12} . For the PLL, design the VCO at the transistor-level and the rest of the blocks may be macro-modeled. The clock distribution network should be designed to drive a distance of 2.5mm in two directions, modeling 10 transmit channels on each side of the global TX PLL. Accurate wire models must be used! The local clocking should produce CMOS-level clock signals to drive a 20fF load per clock phase. Extract the relevant random and deterministic jitter values of the entire clocking network. One component of the deterministic jitter should be the clock network response to a 200MHz signal on the power supply with amplitude of 5% of the supply.

Key References:

- [1] F. O'Mahony *et al.*, "A Low-Jitter PLL and Repeaterless Clock Distribution Network for a 20Gb/s Link," *IEEE Symposium on VLSI Circuits*, June 2006.
- [2] K. Hu, T. Jiang, and P. Chiang, "Comparison of On-die Global Clock Distribution Methods for Parallel Serial Links," *IEEE International Symposium on Circuits and Systems*, June 2009.

Project #4 – Forward-Clock Distribution and Per-Channel De-Skew

The objective of this project is to design/model a forward-clock distribution network and per-channel deskew circuitry to support 20 receive channels operating at 10Gb/s. Optimistically assume that a jitter-free $1V_{ppd}$ clock is forwarded from the TX over the T20 channel to the RX. At the receive side, this clock must be distributed over a distance of 5mm using accurate wire models. The per-channel de-skew circuitry (DLL/PI, ILRO, other) should provide ±0.5UI deskew range and CMOS-level clock signals to drive a 20fF load per clock phase. Extract the relevant random and deterministic jitter values of the entire clocking network. One component of the deterministic jitter should be the clock network response to a 200MHz signal on the power supply with amplitude of 5% of the supply. The target performance is 0.3UI peak-to-peak jitter at a BER=10⁻¹².

Key References:

- [1] G. Balamurugan *et al.*, "A Scalable 5-15Gbps, 14-75mW Low-Power I/O Transceiver in 65nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, Apr. 2008, pp. 1010-1019.
- [2] S. Shekhar *et al.*, "Strong Injection Locking in Low-Q LC Oscillators: Modeling and Application in a Forwarded-Clock I/O Receiver," *IEEE TCAS-I*, vol. 56, no. 8, July 2009, pp. 1818-1829.

Project #5 – DFE-Compatible CDR

The objective of this project is to design a 10Gb/s CDR which is compatible with a DFE. The DFE can be macro-modeled and should have adequate complexity to, potentially along with TX-side FIR and RX-CTLE, allow 10Gb/s operation over the T20 channel assuming a receiver sensitivity of $20mV_{ppd}$ and 0.3UI timing margin at a BER=10⁻¹². The majority of the CDR can be macro-modeled, except for the phase adjustment circuitry (DLL/PI, VCO, etc.) which must be designed at the transistor level. Design the CDR to have a minimum of 1MHz tracking bandwidth. You are encouraged, but not required, to investigate a baud-rate phase detector.

Key References:

- [1] J. Bulzacchelli *et al.*, "A 10Gb/s 5-Tap DFE/4-Tap FFE Transceiver in 90nm CMOS Technology," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, Dec. 2006, pp. 2885-2900.
- [2] F. Spagna *et al.*, "A 78mW 11.8Gb/s Serial Link Transceiver with Adaptive RX Equalization and Baud-Rate CDR in 32nm CMOS," *IEEE ISSCC*, Feb. 2010.
- [3] J. Sonntag and J. Stonick, "A Digital Clock and Data Recovery Architecture for Multi-Gigabit/s Binary Links," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, Aug. 2006, pp. 1867-1875.

Project #6 – Equalization and Crosstalk Cancellation

The objective of this project is to design circuits to cancel far-end crosstalk (FEXT) and near-end crosstalk (NEXT) at 10Gb/s. With ADS, determine the equalization complexity required to allow 10Gb/s operation over the B1, C4, and T20 channels assuming a receiver sensitivity of 20mVppd and 0.3UI timing margin at a BER=10⁻¹². Do this for 4 crosstalk combinations: no crosstalk, 2 FEXT, 1FEXT & 1NEXT, and 2 NEXT aggressors. Design cross-talk cancellation circuitry at the transistor level and in combination with equalization circuitry (which can be macro-modeled) quantify the performance impact of the cross-talk cancellation circuitry.

Key References:

- [1] M. Nazari and A. Emami-Neyestanak, "A 15Gb/s 0.5mW/Gb/s 2-Tap DFE Receiver with Far-End Crosstalk Cancellation," *IEEE International Solid-State Circuits Conference*, Feb. 2011.
- [2] J.-H. Lu *et al.*, "A Merged CMOS Digital Near-End Crosstalk Canceller and Analog Equalizer for Multi-Lane Serial Link Receivers," *IEEE Symposium on VLSI Circuits*, June 2008.

Project #7: 33Gb/s Multi-Channel Forwarded-Clock Optical Transceiver Design

This project involves the design of the circuits for a high-density multi-channel forwarded-clock optical transceiver. The transmitter should perform an 8:1 serialization operation and drive a ring resonator modulator (RRM) that requires a minimum $1.3V_{ppd}$ swing to achieve a 10dB extinction ratio. The RRMs can be modeled electrically as a 15fF capacitor. The receiver should perform a 1:8 deserialization operation and interface with a photodetector that has 0.8A/W responsivity and 14fF total capacitance. The receiver should achieve -20dBm sensitivity for a BER=10⁻¹². Either global or local clocking circuitry should be designed to produce the necessary CMOS-level clocks at each transmitter channel. At the receive side, a clock channel receives a -20dBm 8.25GHz optical clock signal and must amplify and distribute this again to 31 receiver channels spaced at a 20µm pitch. Either global or local clocking circuitry should be designed to produce the necessary CMOS-level clocks to drive the receiver samplers.

Project #8 – 64Gb/s Simultaneous Bidirectional Die-to-Die Multi-Channel Transceiver

This project involves the design of a multi-channel die-to-die transceiver that communicates over a silicon interposer channel with simultaneous bidirectional signaling. The transceiver should be architected as a 20-wire system, with 18 single-ended wires for data transmission at 64Gb/s simultaneous bidirectional and 2 wires for unidirectional 1/8th-rate forwarded clocks. The transceiver should include 16:1 serialization at the transmitter and 1:16 deserialization at the receiver, along with the transmit driver, receiver front-end, and hybrid circuitry to separate the inbound and outbound signals. The necessary transmit and receive clock generation, distribution, and per-channel deskew circuitry should also be designed.

Project #9 – 224Gb/s Coherent Transceiver

This project involves the design of a transceiver for a 224Gb/s dual-polarization QAM16 coherent system. The 28GBaud transmitter should support PAM-4 modulation at a minimum $2V_{ppd}$ output swing, allowing for 224Gb/s operation with a silicon photonic dual-polarization coherent modulator. A receiver front-end should be designed to achieve BER<10⁻⁴. A complete link model should be constructed with models for the transmit-side modulator and receiver-side coherent demodulator and operation with BER<10⁻⁴ should be verified.

Project #10 – Topic of Your Choice

I welcome any project suggestions related to high-speed links circuits and systems.

Note, while key references are listed for the project topics, a comprehensive literature search of the most recent and existing related material is expected.

Project Channel Responses





Important Dates

- April 15 Preliminary Report
- April 29 Final Report Due.

Project Grading

- Preliminary Report 10%
- Final Report 90%

Preliminary Report Required Sections

- 1. Motivation and Project Overview
- 2. Literature Survey
- 3. Proposed Architecture
 - a. This can change for the final report
- 4. Initial Simulation Results
- 5. Plan of Work
 - a. A description of what will be completed for the final report

Final Report Required Sections

- 1. Motivation and Project Overview
- 2. Literature Survey
- 3. Architecture
- 4. Simulation Results
 - a. This section must include a Table comparing your design with current references
- 5. Conclusion