March 31, 2021

ECEN 720: High-Speed Links

Final Project

Instructor: Sam Palermo

Project teams can consist of 1-3 students.

Project Topics

Project #1 – Voltage-Mode Transmitter with High-Resolution Equalization

The objective of this project is to design a voltage-mode transmitter with 3-tap FIR equalization at 6-bit resolution. The driver can either be a low-swing version ($V_{out} \leq 400mV_{ppd}$) or a high-swing version ($V_{out} \geq 800mV_{ppd}$). Design the transmitter to operate at maximum data rate of 10Gb/s. Quantify the maximum data rate you can achieve over the B1, C4, and T20 channels assuming a receiver sensitivity of $20mV_{ppd}$ and 0.3UI timing margin at a BER=10^{-12}. Emphasize efficient realization of the equalization taps.

Key References:

[1] H. Hatamkhani *et al.*, "A 10mW 3.6Gbps I/O Transmitter," *IEEE Symposium on VLSI Circuits*, June 2003.

[2] W. Dettloff *et al.*, "A 32mW 7.4Gb/s Protocol-Agile Source-Series Terminated Transmitter in 45nm CMOS SOI," *IEEE International Solid-State Circuits Conference*, Feb. 2010.

[3] R. Sredojevic and V. Stojanovic, "Digital Link Pre-emphasis with Dynamic Driver Impedance Modulation," *IEEE Custom Integrated Circuits Conference*, Sept. 2010.

Project #2 – DFE-IIR Equalization

The objective of this project is to design a 10Gb/s DFE with a combination of FIR and IIR feedback filtering. Optimize the FIR tap number and IIR filter response to (attempt to) achieve 10Gb/s operation over the B1, C4, and T20 channels assuming a receiver sensitivity of 20mVppd and 0.3UI timing margin at a BER=10^{-12}. Quantify the performance impact of including the IIR feedback filter versus only using an FIR feedback filter.

Key References:

[1] B. Kim *et al.*, "A 10Gb/s Compact Low-Power Serial I/O with DFE-IIR Equalization in 65-nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 44, no. 12, Dec. 2009, pp. 3526-3538.

[2] Y.-C. Huang and S.-I. Liu, "A 6Gb/s Receiver with 32.7dB Adaptive DFE-IIR Equalization," *IEEE International Solid-State Circuits Conference*, Feb. 2011.

Project #3 – TX Clock Generation, Distribution, and Local Clocking

The objective of this project is to design/model a global clock generation PLL and distribution network to support 20 transmit channels operating at 10Gb/s. A jitter budget for the transmit clocking network should be produced to allow 10Gb/s operation over the T20 channel assuming a receiver sensitivity of $20mV_{ppd}$ and 0.3UI timing margin at a BER=10^{-12}. For the PLL, design the VCO at the transistor-level and the rest of the blocks may be macro-modeled. The clock distribution network should be designed to drive a distance of 2.5mm in two directions, modeling 10 transmit channels on each side of the global TX PLL. Accurate wire models must be used! The local clocking should produce CMOS-level clock signals to drive a 20fF load per clock phase. Extract the relevant random and deterministic jitter values of the entire clocking network. One component of the deterministic jitter should be the clock network response to a 200MHz signal on the power supply with amplitude of 5% of the supply.

Key References:

[1] F. O'Mahony *et al.*, "A Low-Jitter PLL and Repeaterless Clock Distribution Network for a 20Gb/s Link," *IEEE Symposium on VLSI Circuits*, June 2006.

[2] K. Hu, T. Jiang, and P. Chiang, "Comparison of On-die Global Clock Distribution Methods for Parallel Serial Links," *IEEE International Symposium on Circuits and Systems*, June 2009.

Project #4 – Forward-Clock Distribution and Per-Channel De-Skew

The objective of this project is to design/model a forward-clock distribution network and per-channel de-skew circuitry to support 20 receive channels operating at 10Gb/s. Optimistically assume that a jitter-free $1V_{ppd}$ clock is forwarded from the TX over the T20 channel to the RX. At the receive side, this clock must be distributed over a distance of 5mm using accurate wire models. The per-channel de-skew circuitry (DLL/PI, ILRO, other) should provide ±0.5UI deskew range and CMOS-level clock signals to drive a 20fF load per clock phase. Extract the relevant random and deterministic jitter values of the entire clocking network. One component of the deterministic jitter should be the clock network response to a 200MHz signal on the power supply with amplitude of 5% of the supply. The target performance is 0.3UI peak-to-peak jitter at a BER=10^{-12}.

Key References:

[1] G. Balamurugan *et al.*, "A Scalable 5-15Gbps, 14-75mW Low-Power I/O Transceiver in 65nm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 43, no. 4, Apr. 2008, pp. 1010-1019.

[2] S. Shekhar *et al.*, "Strong Injection Locking in Low-Q LC Oscillators: Modeling and Application in a Forwarded-Clock I/O Receiver," *IEEE TCAS-I*, vol. 56, no. 8, July 2009, pp. 1818-1829.

Project #5 – DFE-Compatible CDR

The objective of this project is to design a 10Gb/s CDR which is compatible with a DFE. The DFE can be macro-modeled and should have adequate complexity to, potentially along with TX-side FIR and RX-CTLE, allow 10Gb/s operation over the T20 channel assuming a receiver sensitivity of $20mV_{ppd}$ and 0.3UI timing margin at a BER=10^{-12}. The majority of the CDR can be macro-modeled, except for the phase adjustment circuitry (DLL/PI, VCO, etc.) which must be designed at the transistor level. Design the CDR to have a minimum of 1MHz tracking bandwidth. You are encouraged, but not required, to investigate a baud-rate phase detector.

Key References:

[1] J. Bulzacchelli *et al.*, "A 10Gb/s 5-Tap DFE/4-Tap FFE Transceiver in 90nm CMOS Technology," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 12, Dec. 2006, pp. 2885-2900.

[2] F. Spagna *et al.*, "A 78mW 11.8Gb/s Serial Link Transceiver with Adaptive RX Equalization and Baud-Rate CDR in 32nm CMOS," *IEEE ISSCC*, Feb. 2010.

[3] J. Sonntag and J. Stonick, "A Digital Clock and Data Recovery Architecture for Multi-Gigabit/s Binary Links," *IEEE Journal of Solid-State Circuits*, vol. 41, no. 8, Aug. 2006, pp. 1867-1875.

Project #6 – Equalization and Crosstalk Cancellation

The objective of this project is to design circuits to cancel far-end crosstalk (FEXT) and near-end crosstalk (NEXT) at 10Gb/s. With ADS, determine the equalization complexity required to allow 10Gb/s operation over the B1, C4, and T20 channels assuming a receiver sensitivity of 20mVppd and 0.3UI timing margin at a BER=10^{-12}. Do this for 4 crosstalk combinations: no crosstalk, 2 FEXT, 1FEXT & 1NEXT, and 2 NEXT aggressors. Design cross-talk cancellation circuitry at the transistor level and in combination with equalization circuitry (which can be macro-modeled) quantify the performance impact of the cross-talk cancellation circuitry.

Key References:

[1] M. Nazari and A. Emami-Neyestanak, "A 15Gb/s 0.5mW/Gb/s 2-Tap DFE Receiver with Far-End Crosstalk Cancellation," *IEEE International Solid-State Circuits Conference*, Feb. 2011.

[2] J.-H. Lu *et al.*, "A Merged CMOS Digital Near-End Crosstalk Canceller and Analog Equalizer for Multi-Lane Serial Link Receivers," *IEEE Symposium on VLSI Circuits*, June 2008.

Project #7 – Radiation-Hardened PLL

This project involves the design of a radiation-hardened 14-21GHz PLL. All key components of the PLL should implement radiation hardening techniques. Key simulations should be performed to quantify both the PLL building blocks and the complete loop response to single event effects and total ionizing dose.

Project #8 – 128Gb/s Multi-Carrier Receiver

This project involves the design of a 25Gb/s laser driver transmitter. The transmitter should perform an 8:1 serialization operation. A macromodel should be utilized to model the lasers electrical and optical characteristics. The transmitter should implement a 2-tap equalizer to compensate for laser bandwidth limitations. A 1mW optical modulation amplitude (OMA) should be achieved.

Project #9 – 112Gb/s PAM4 CDR-Based Optical Receiver

This project involves the development of an optical receiver with a CDR capable of supporting 112Gb/s PAM4 operation. The CDR should be designed in the context of an optical receiver that achieves -12dBm sensitivity at a BER=10^{-4} with an avalanche photodetector that has 3A/W responsivity and 80fF capacitance. Additional interconnect parasitics between the APD and the TIA include a 300pH bondwire inductance and 50fF for chip pad capacitance. The CDR should have the capability to optimize the sampling clock phase of the individual 2b flash comparators to compensate for PAM4 eye skew.

Project #10 – Topic of Your Choice

This project involves the design of a dual-differential high-swing highly-linear Mach-Zehnder modulator (MZM) transmitter for analog link applications. The driver should operate over a frequency range of 25-40GHz. The driver should implement linearization techniques to compensate for the inherent MZM non-linearity. Key specs are

Max Dual Differential Output Swing = $5V_{ppd}$

IM3 Suppression with 50% modulation index > 15dB

IIP_3 > 10dBm

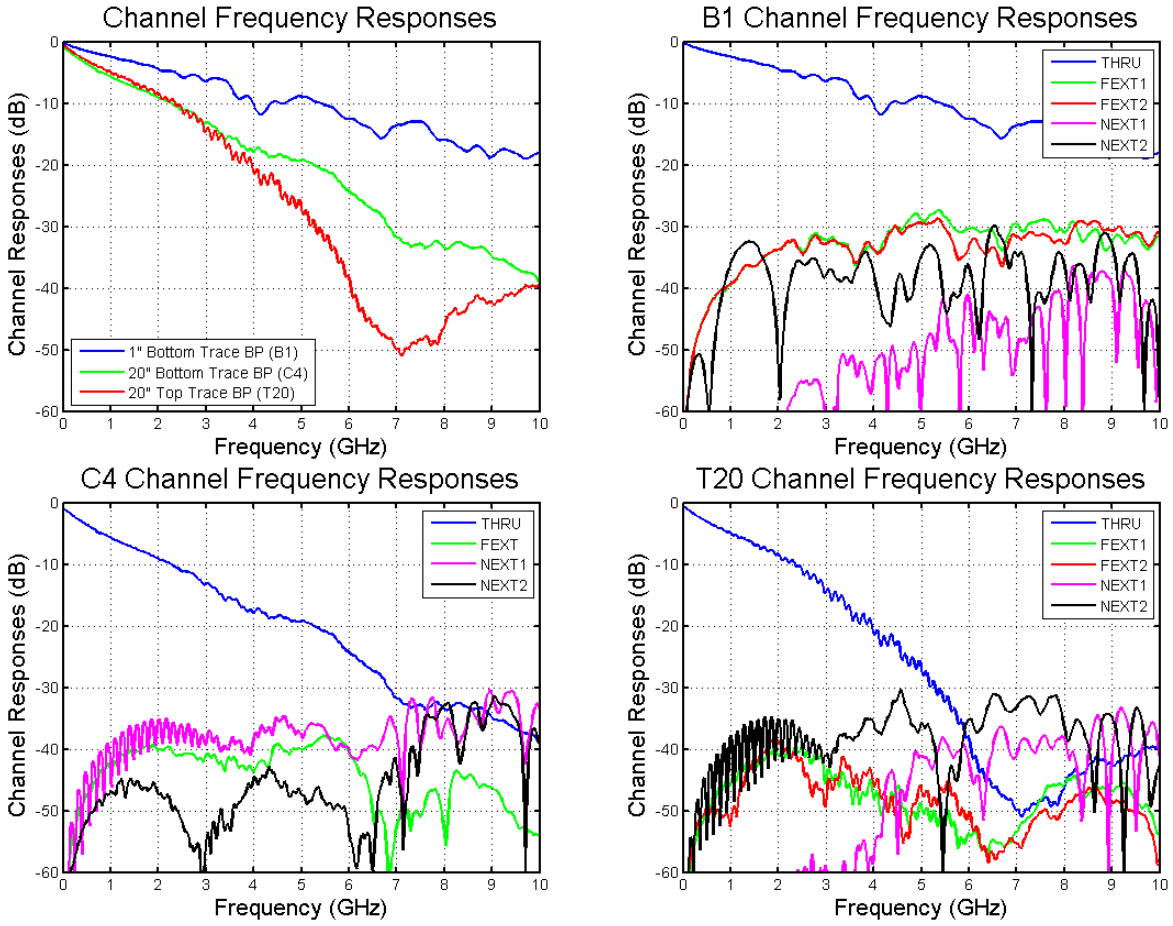
A macro-model of the MZM must be produced which captures both electrical and optical characteristics.

Project #11 – Topic of Your Choice

I welcome any project suggestions related to high-speed links circuits and systems.

Note, while key references are listed for the project topics, a comprehensive literature search of the most recent and existing related material is expected.

Project Channel Responses



Important Dates

- April 12 Inform Prof. Palermo of project choice
- April 19 Preliminary Report
- April 29 Final Report Due by email.
- May 4 Project Presentation (11:00AM-1:30PM).

Project Grading

- Preliminary Report 10%
- Report and Presentation 90%

Preliminary Report Requirements

The preliminary report should have the following sections:

1. Project Overview
2. Literature Survey
3. Initial Architecture. Note, this can change completely in your final report.
4. Initial Simulation Results. You must have at least one initial simulation result.

Final Report Requirements

The report must include a summary of the key specifications and background literature survey, with adequate references. A complete discussion of the architecture, with comments on the robustness should be included. There should be adequate simulations to justify the performance and a comparison with the current state-of-the-art. Project grading will be a function of the creativity and elegance of the design, completeness of the analysis, and the clarity of the report and presentation.