10-2

A 10Gb/s Compact Low-Power Serial I/O with DFE-IIR Equalization in 65nm CMOS

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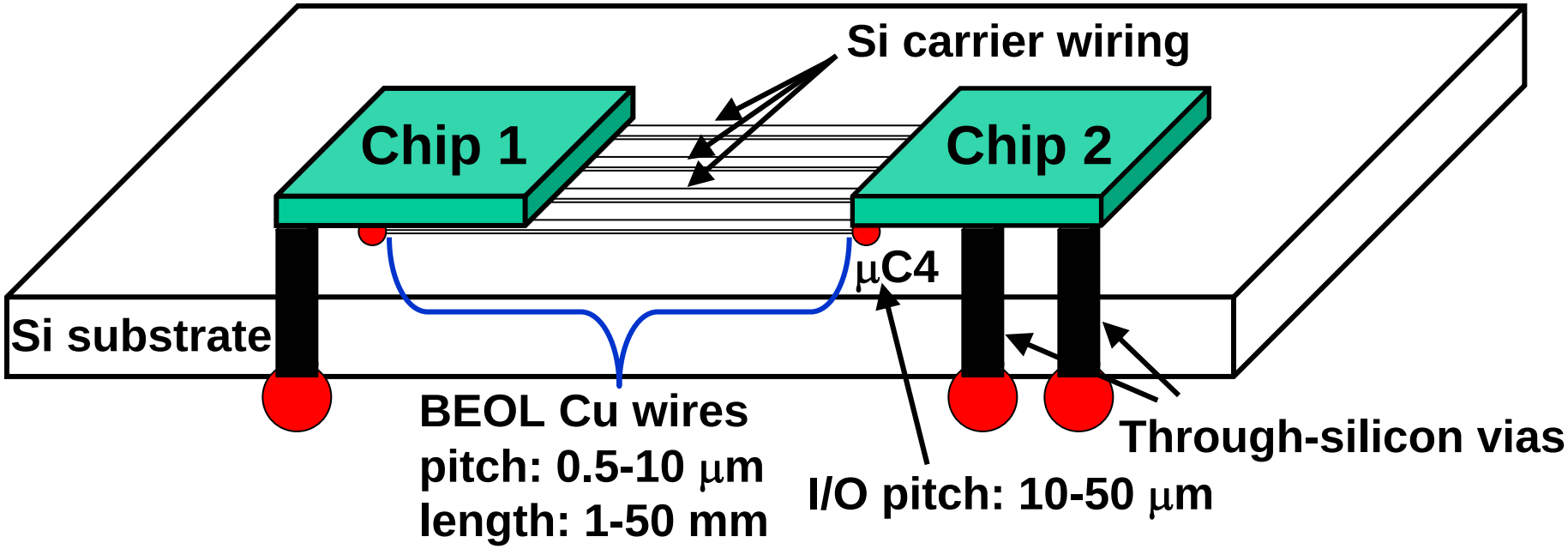
Outline

- **Introduction: silicon carrier channel**
- **Compact I/O with DFE-IIR equalization**
  - **Termination**
  - **Equalization**
  - **Circuit details**
- **Implementation and measurement**
- **Conclusions**

Short-Reach Links on Silicon Carrier

- **Silicon carrier: silicon with BEOL used as dense packaging medium**

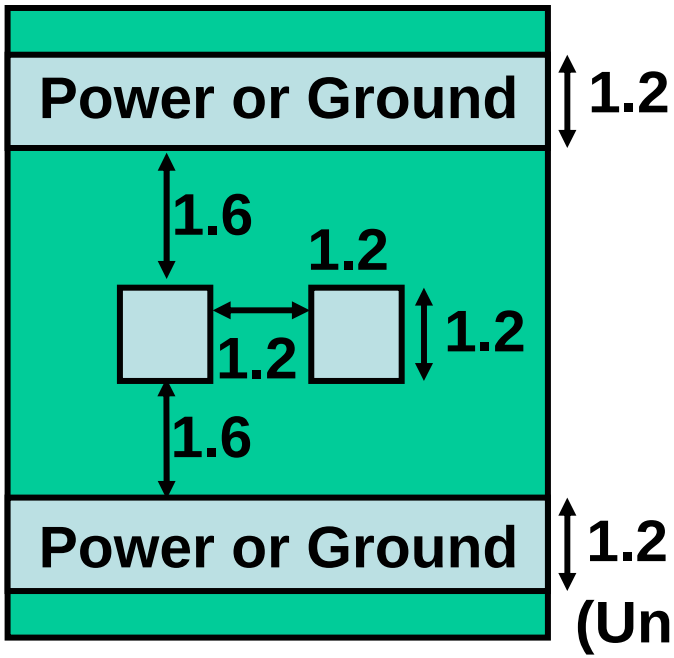


- **Advantage: high wiring density ➔ ultra-high chip-to-chip aggregate bandwidth**
- **Key I/O goal: low area and power costs**

Ref: J. Knickerbocker, *JSSC* 2006, p. 1718

Silicon Carrier Transmission Lines

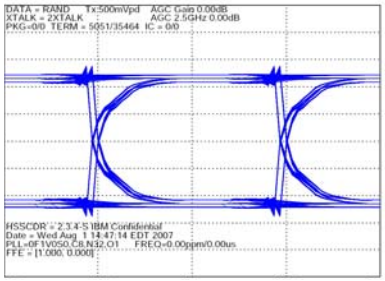
Example of differential wire pair in stripline structure



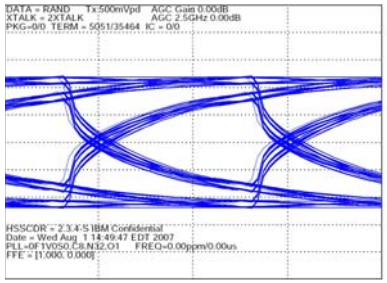
(Unit: μm)

Simulated eye diagrams @5 Gb/s

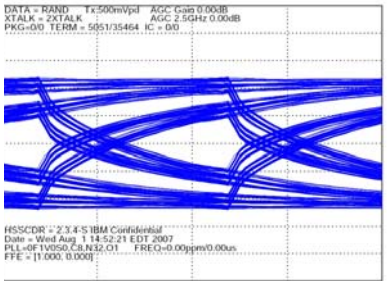
L=2.5 mm



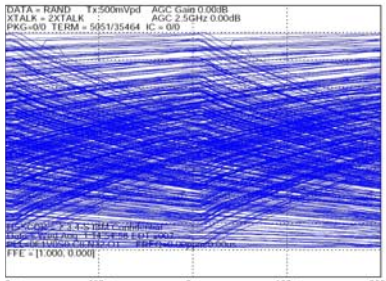
L=7.5 mm



L=10 mm



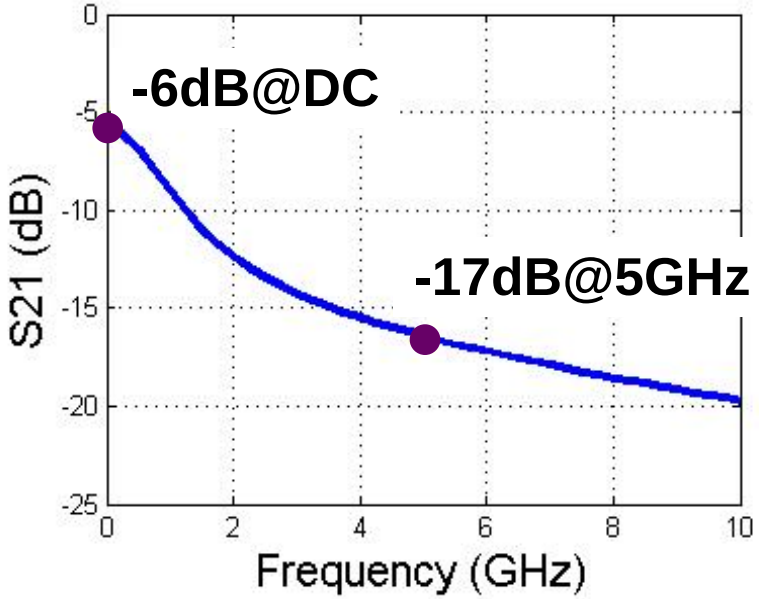
L=20 mm

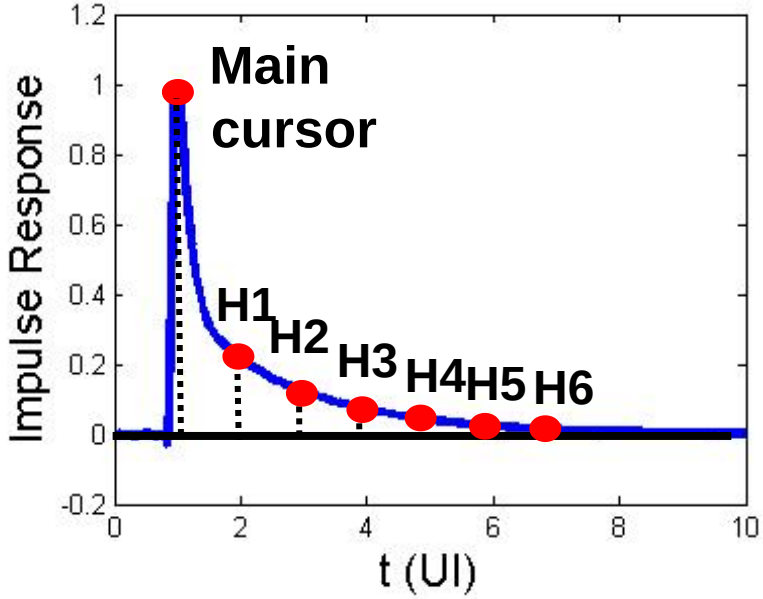


- **Wires are narrow and thin**
  - **Significant resistive losses for lengths >5 mm**
  - **Equalization needed for long channels**

Characteristics of Si Carrier Channels

20mm Si carrier channel characteristics





- **Long silicon carrier channels:**
  - **Significant DC attenuation**
  - **Smoothly varying S21 curve**
  - **Long impulse response tail**

Outline

- **Introduction: silicon carrier channel**
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  - **Termination**
  - **Equalization**
  - **Circuit details**
- **Implementation and measurement**
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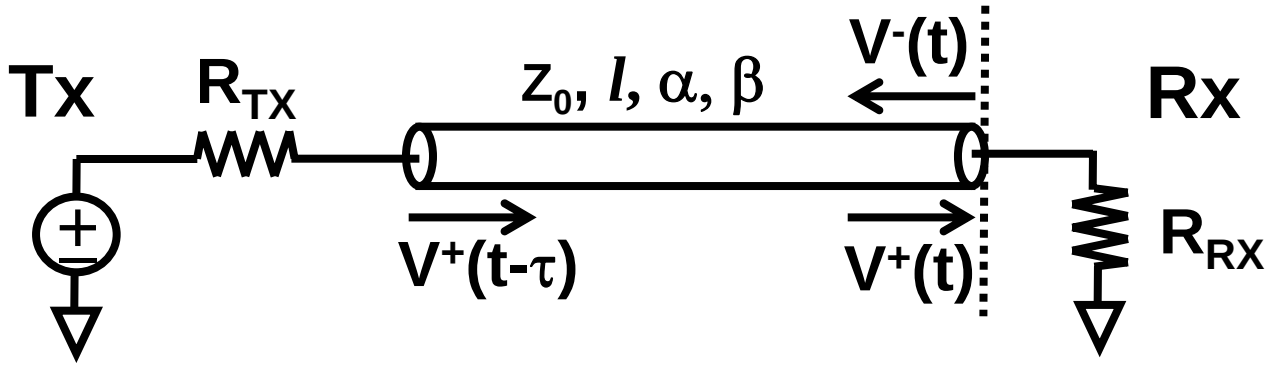
Tx, Rx Termination Strategy for Si Carrier Links



Si carrier channel: Z_0=50~80 Ω

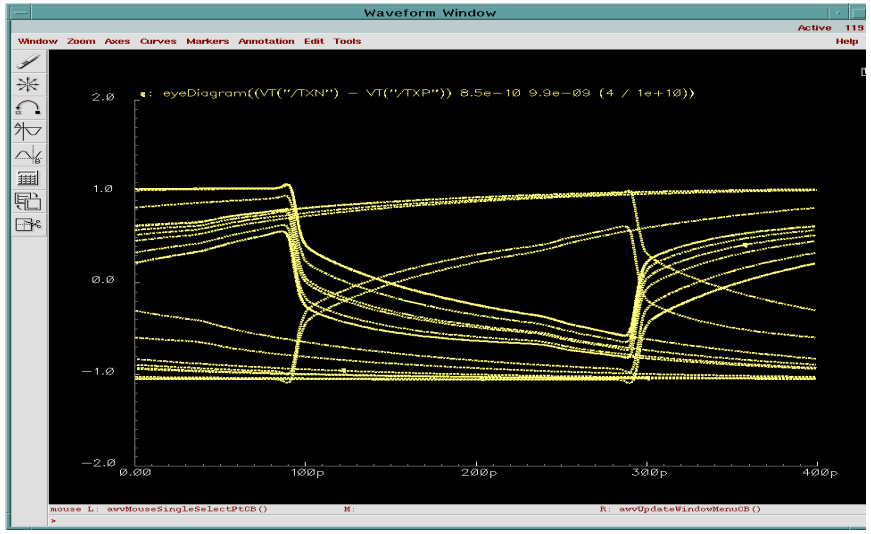
- **Power/performance joint optimization yields**
  - **Low-Z Tx (< 50 Ω) for high drive strength**
  - **High-Z Rx (e.g., 1 KΩ) for low power dissipation**

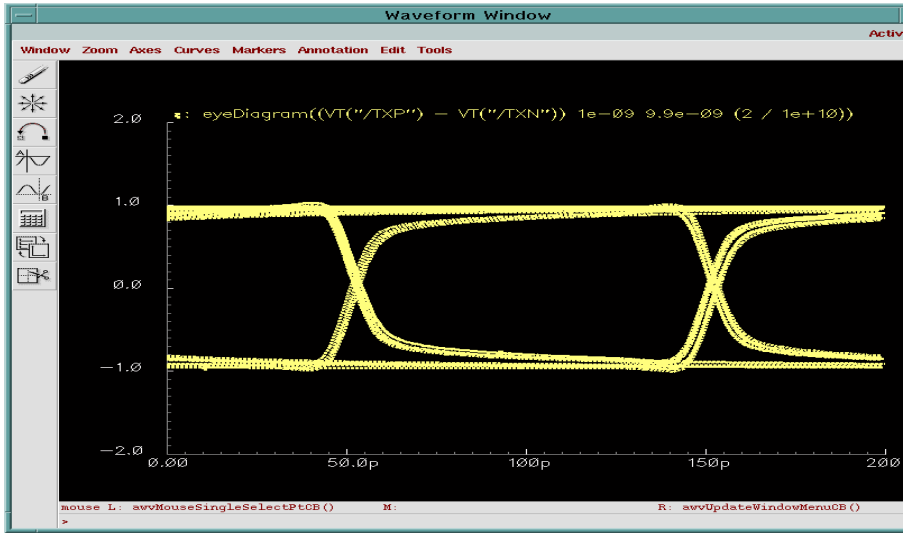
- ***Is the performance impact acceptable?***

Tx Termination Strategy Analysis

- **Low-Z Tx (< 50 Ω) provides better performance than 50-Ω terminated Tx**

Simulated eye diagrams of Tx output





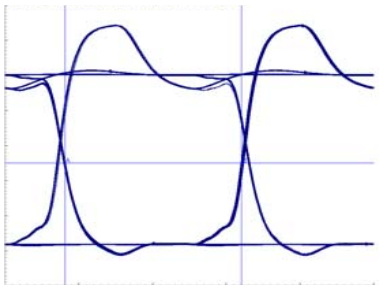
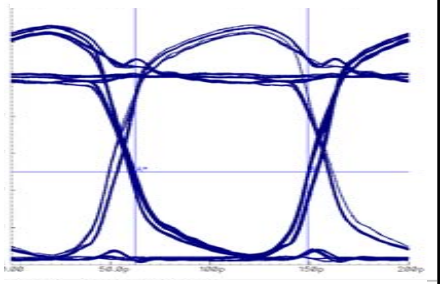
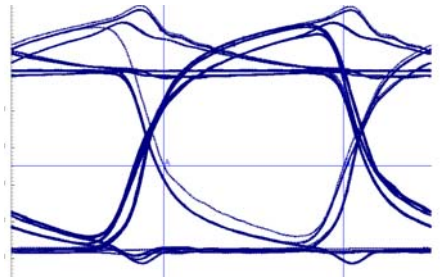
R_{TX}=50 Ω
10 mm channel 5 Gb/s

R_{TX}<50 Ω
40 mm channel 10 Gb/s

Rx Termination Strategy Analysis

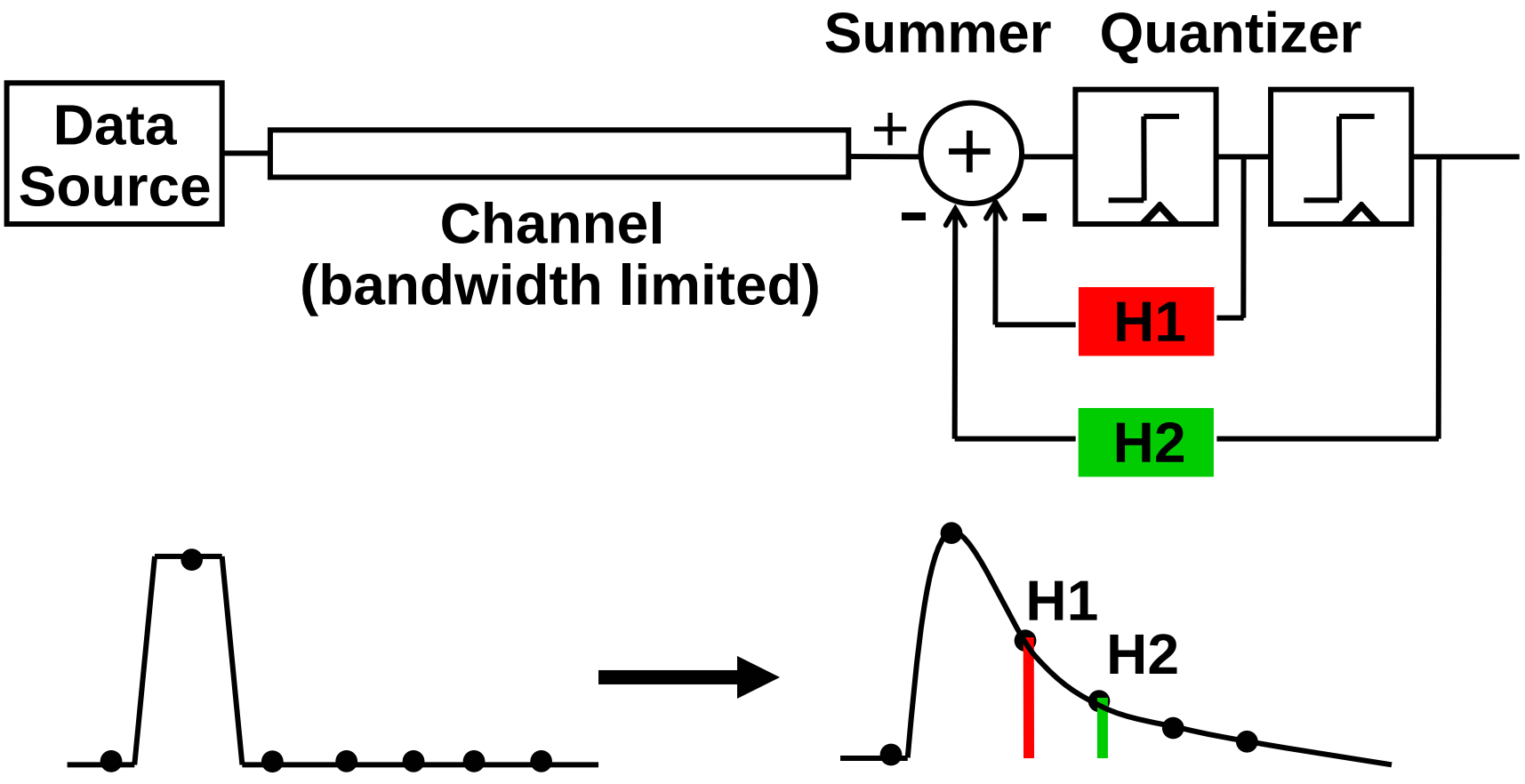
- **Key issue: reflections due to mismatch**
  - **–Long links(> 7.5 mm): mitigated by lossy channels**
  - **–Short links: detailed study required**

Simulated Rx eye diagrams @10 Gb/s, R_{TX}<50 Ω, R_{RX}=1 KΩ

Rx Eye			
Channel Length	**2.5 mm**	**5 mm**	**7.5 mm**
Channel Delay	**16 ps**	**33 ps**	**50 ps (0.5 UI) (worst-case)**

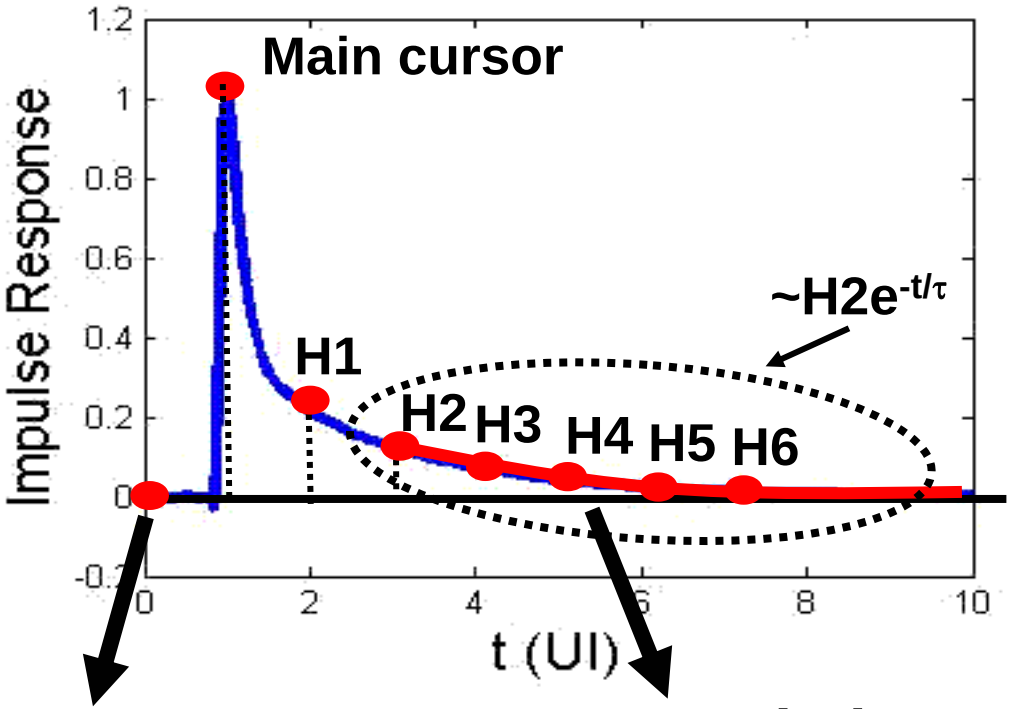
- **Conclusion: minor performance impact**

Background: Decision Feedback Equalization (DFE)



- 2-tap DFE: Set H1 and H2 tap weights to cancel the ISI of the previous two bits

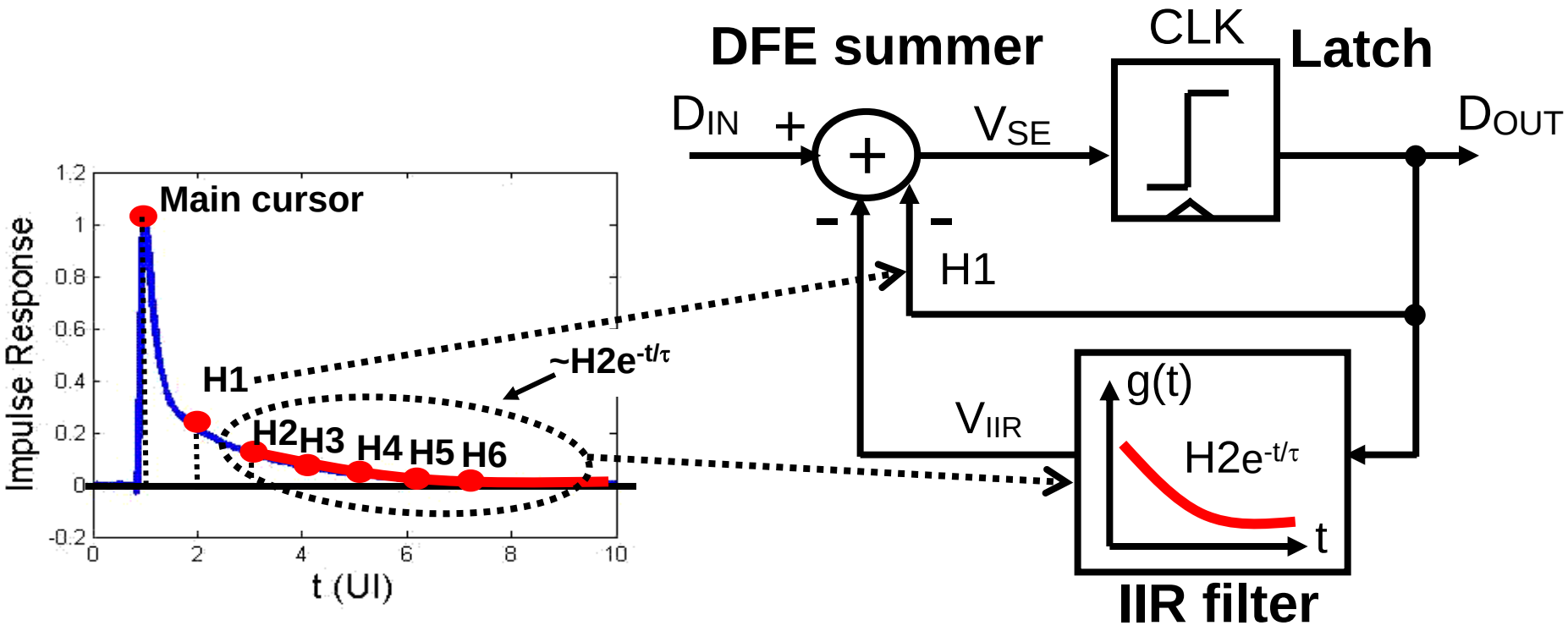
Equalization Strategy for Si Carrier Links



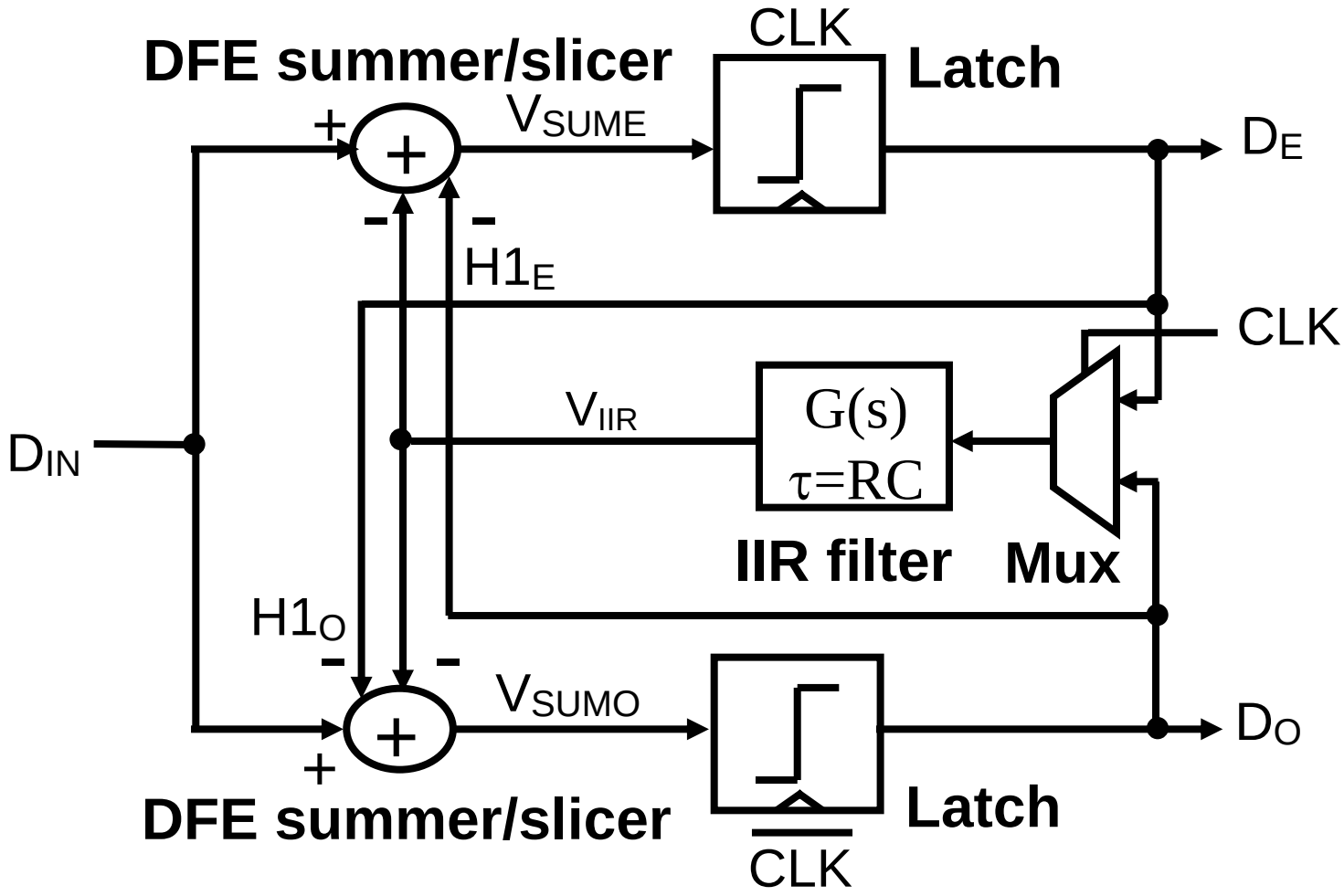
- **Minimal precursor content**
  - **–Tx: no FFE**
- **Extended postcursor tail**
  - **–Rx: high tap count DFE (ideally)**
- **Challenge: to achieve the performance of high tap-count DFE without paying area and power penalty**
- **Strategy: to take advantage of Si carrier channel characteristics to meet the challenge**

Compact low-power Rx: DFE with IIR Filter

- **Observation: Si carrier channel impulse response well modeled by 1 discrete tap and 1 continuous-time filter**
- **Solution: DFE with 1 discrete tap and 1 adjustable continuous-time IIR filter-driven tap**

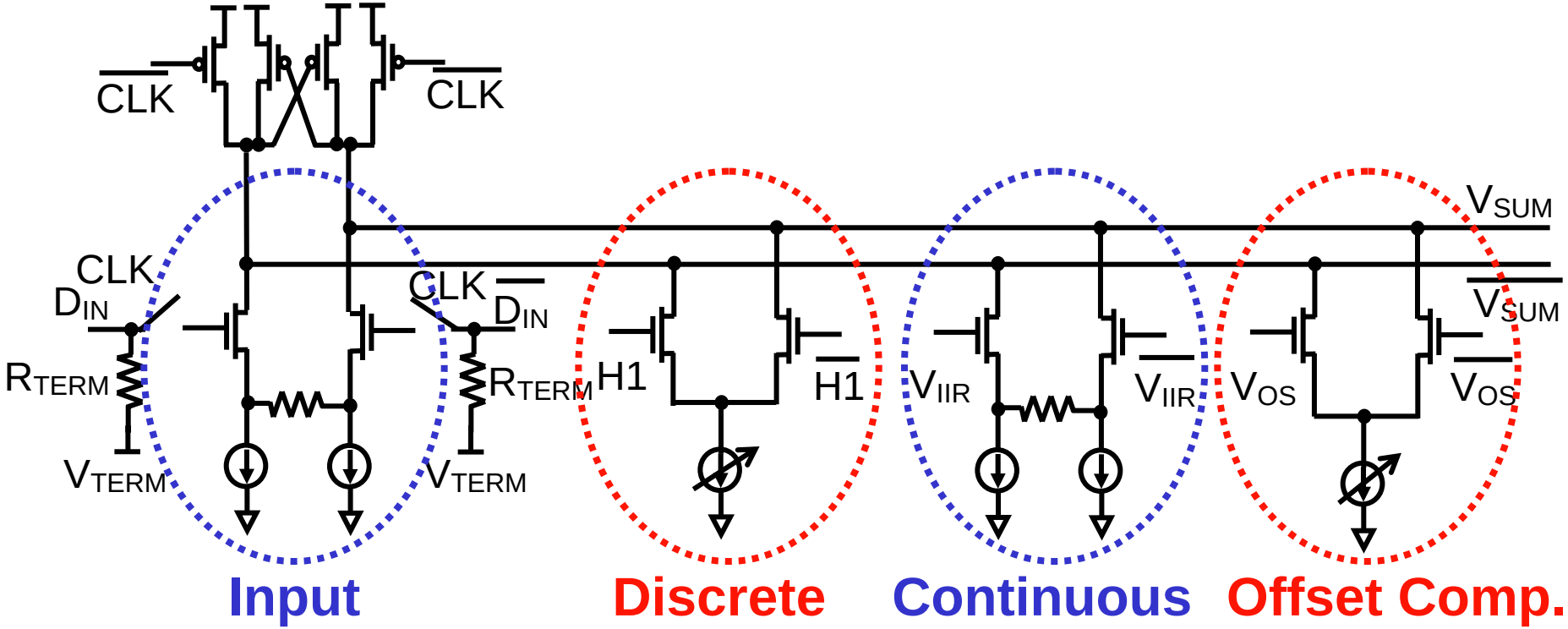


Half-Rate DFE-IIR Rx Architecture



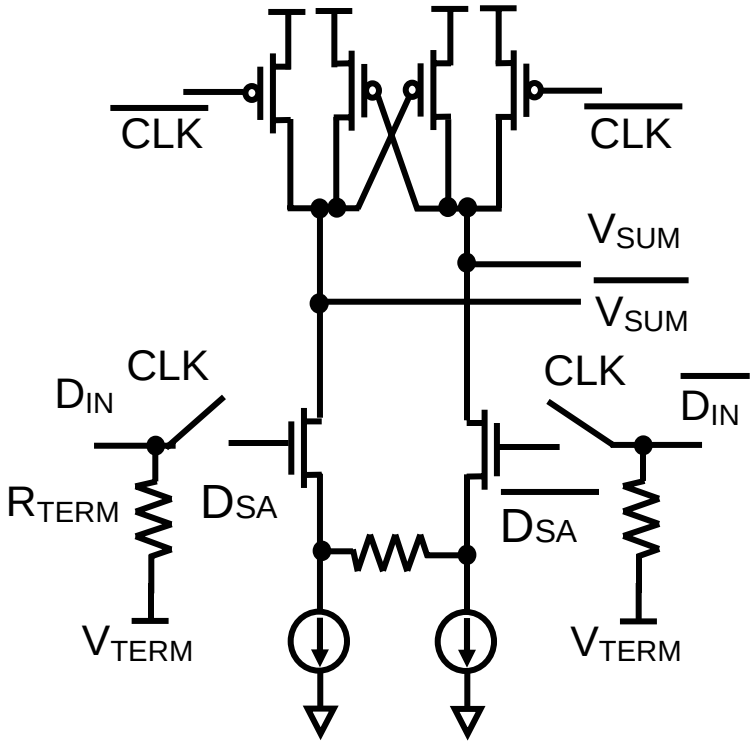
- **Key features:**
  - **Slicer, DFE summing stage merged**
  - **Full-rate adjustable continuous-time IIR filter + Mux**
  - **High-speed double-regenerating latch**

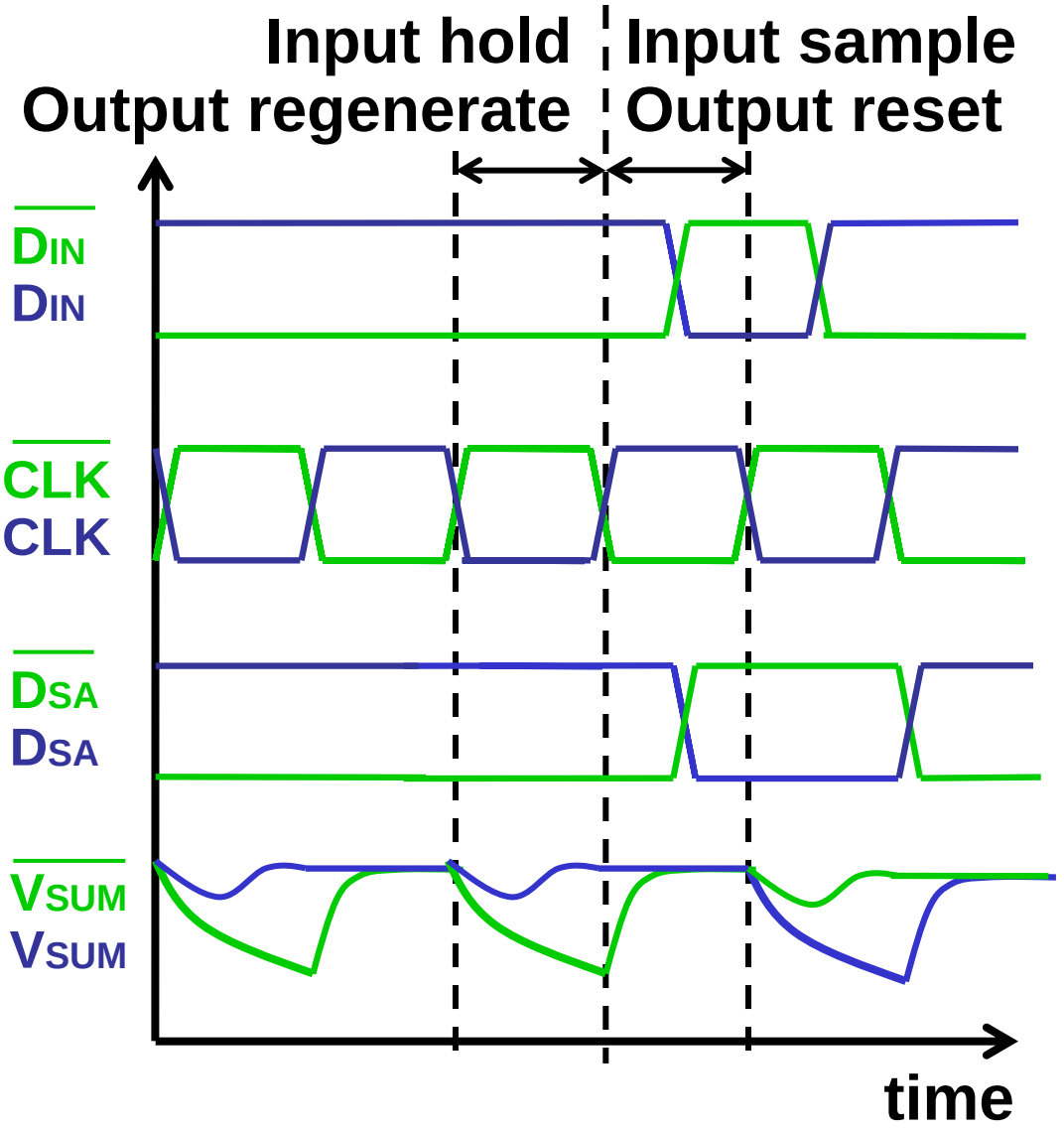
DFE Summer/Slicer



- **Summer architecture: high speed, low-power**
  - **Current integrator mitigates settling time constraint**
  - **Resettable current-comparator PMOS load (slicer)**
- **Transconductor configuration**
  - **Linear: input, continuous-time IIR filter feedback**
  - **Nonlinear: discrete H1 feedback, offset compensation**

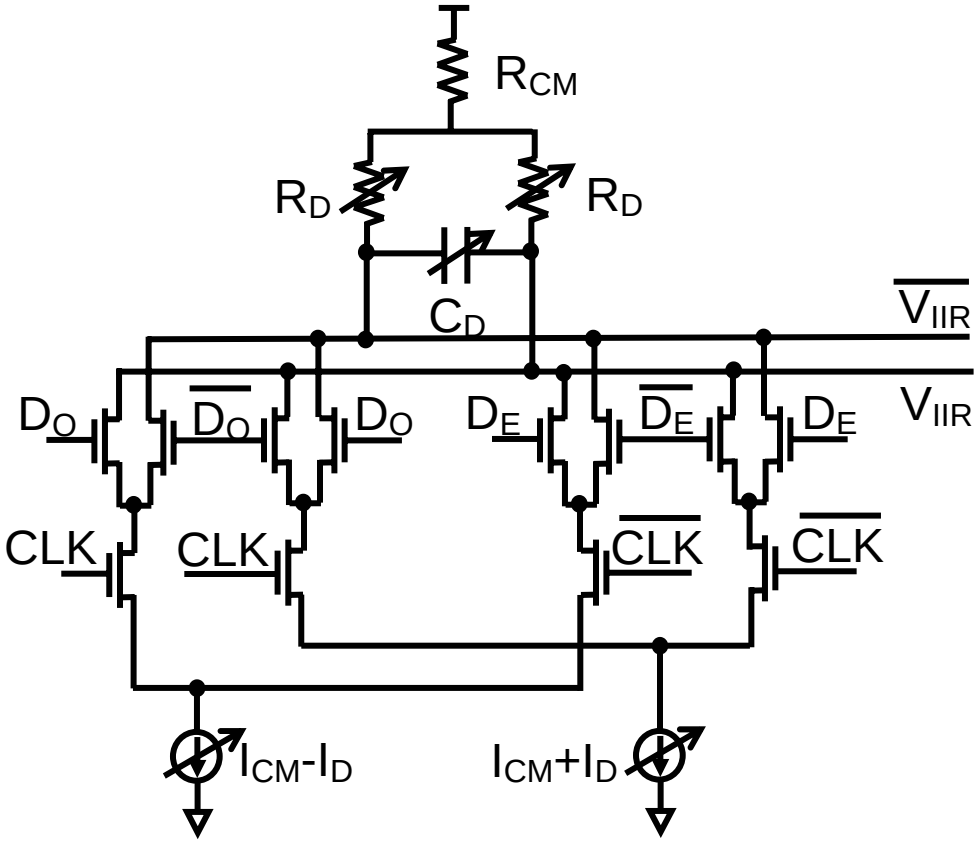
Operation of the DFE Summer/Slicer

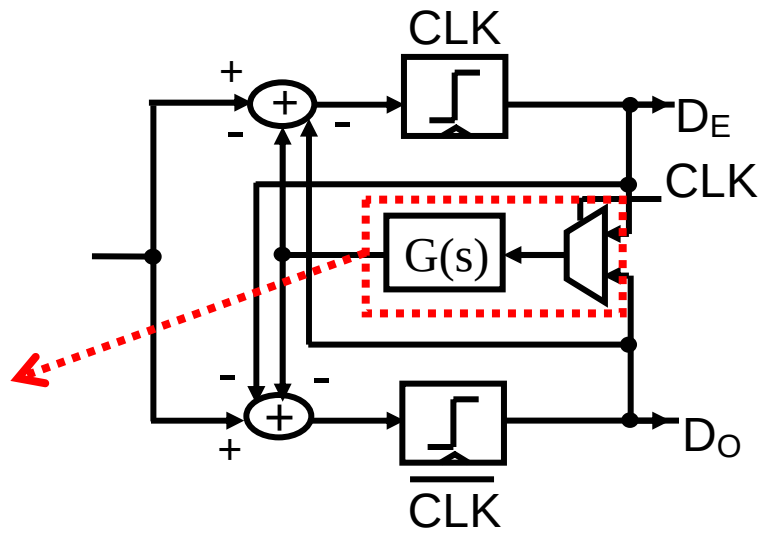




Ref: T. Dickson, *VLSI* 2008, p. 58

IIR Filter Merged with Mux

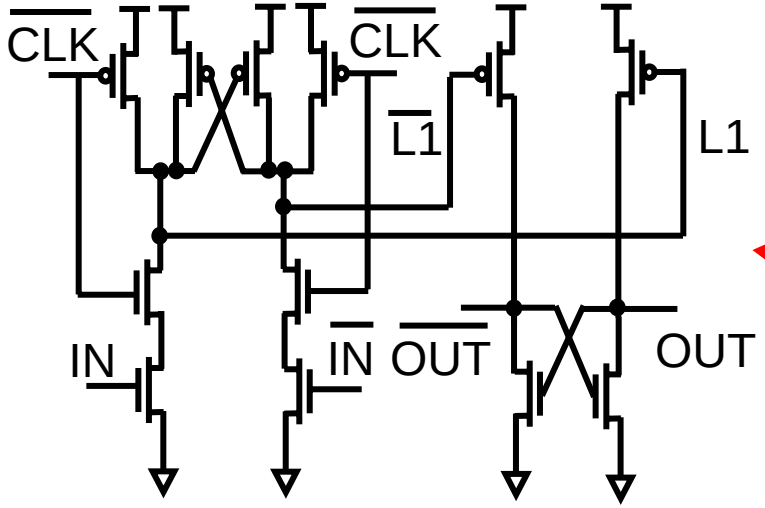


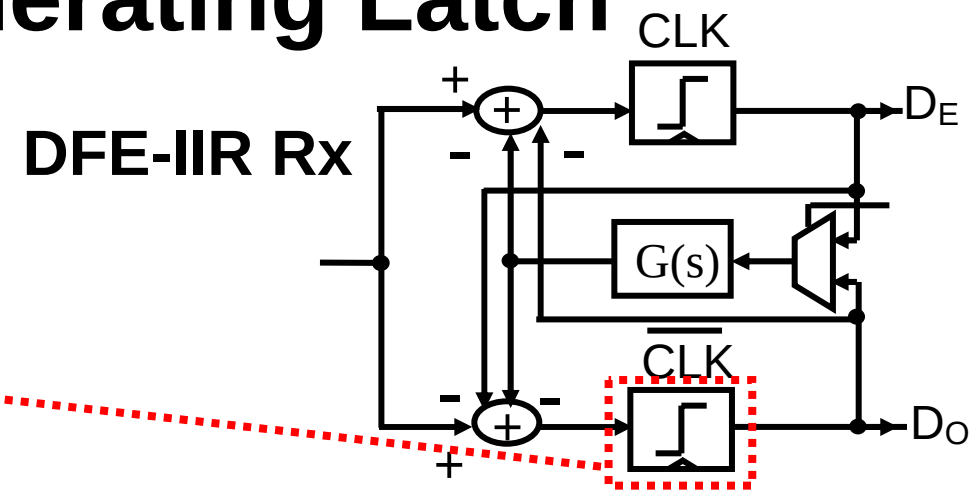


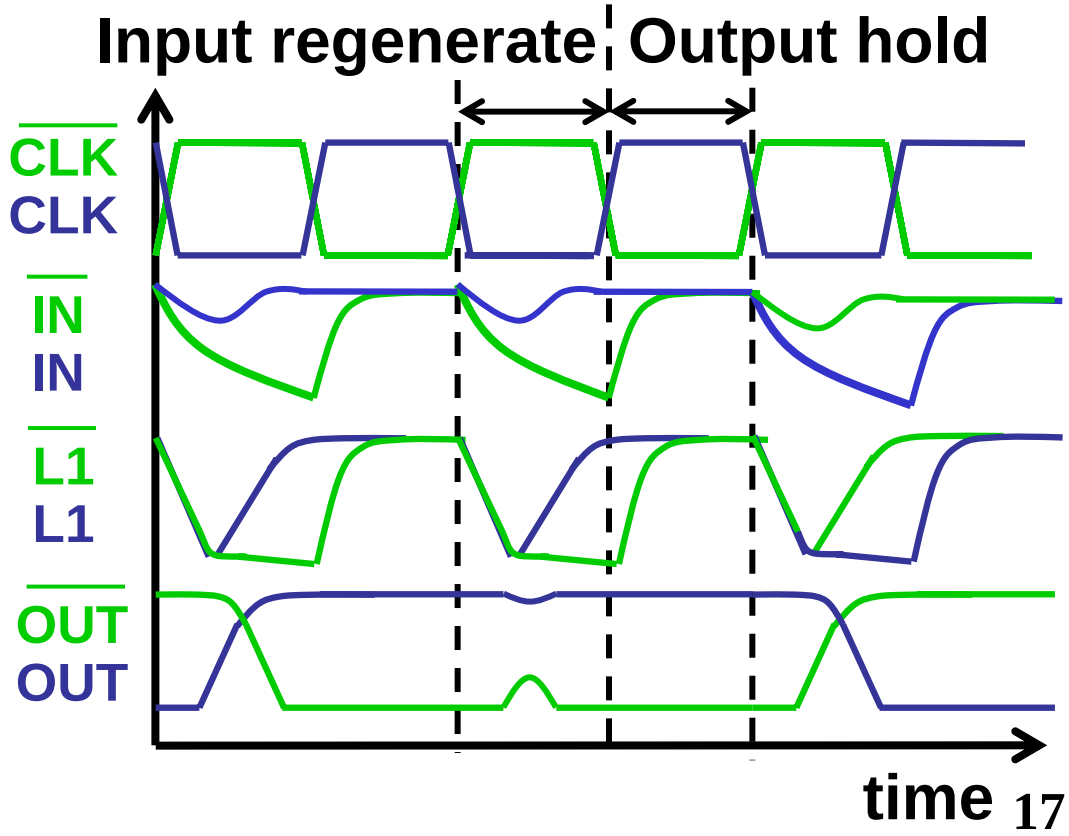
DFE-IIR Rx

- **Motivation for mux: to simplify IIR filter (full-rate channel)**
- **Time constant controlled by R_D and C_D**
- **Amplitude controlled by R_D and I_D**

Double-Regenerating Latch



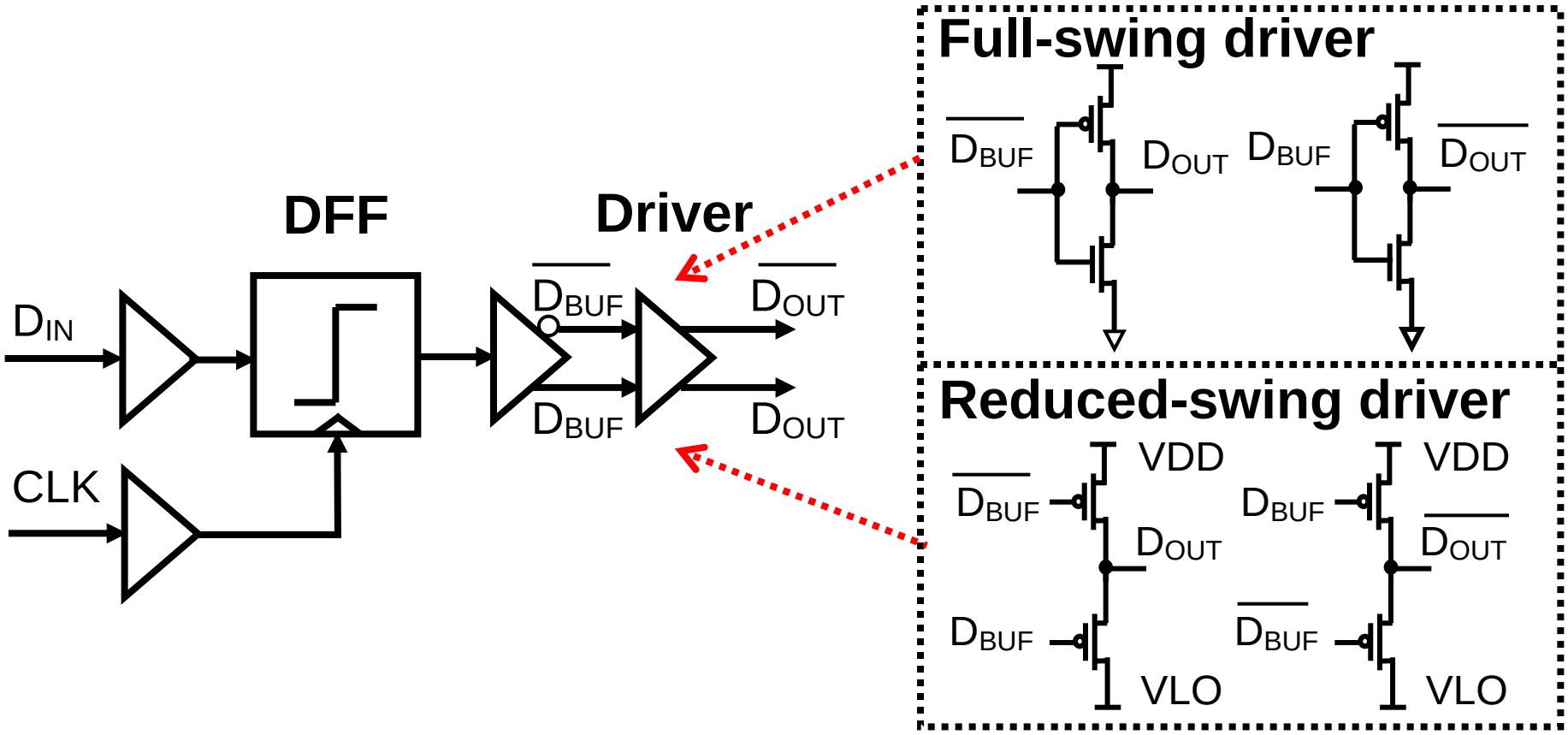




Key features:

- **High speed: two-stage data regeneration**
- **CMOS, CML compatible**

Full-Rate Transmitter



- **Driver selection based on channel characteristics**
  - **–Full swing for long channel**
  - **–Reduced swing for short channel**

Ref: K. Wong, *JSSC* 2004, p. 602

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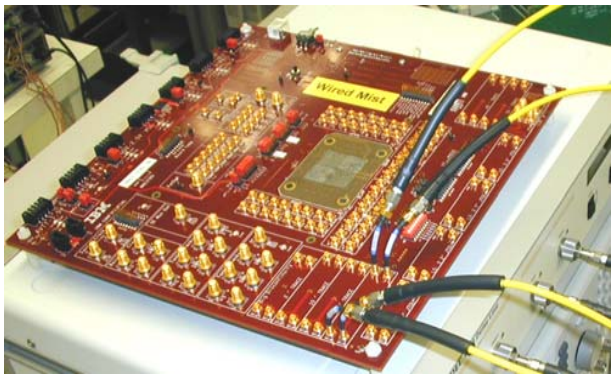
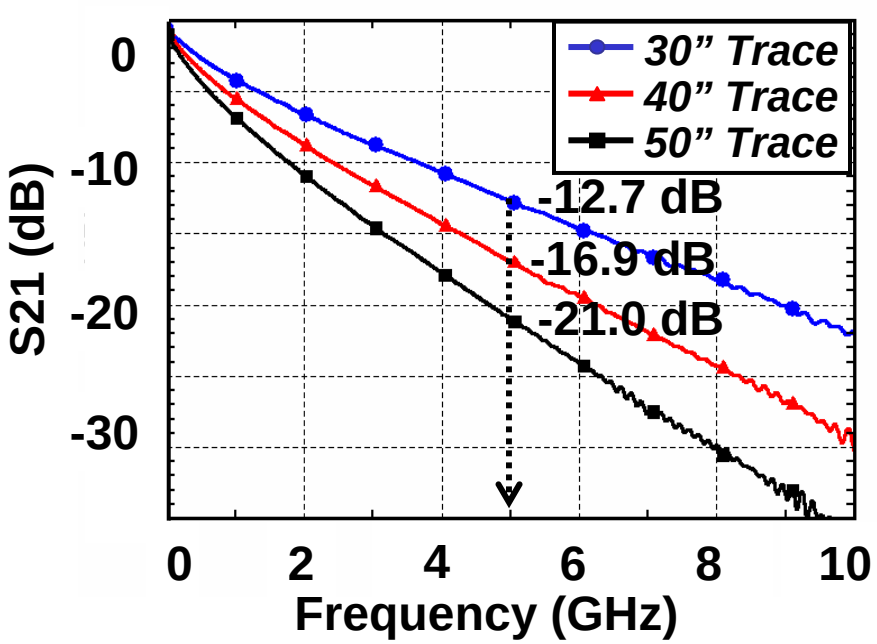
Compact I/O Test Site Overview

- **Technology:**
  - **IBM 65 nm bulk CMOS**
- **List of test sites:**
  - **Rx (4):**
    - **5 and 10 Gb/s DFE-IIR, 50 Ω terminated**
    - **5 and 10 Gb/s 2-tap DFE, 50 Ω terminated**
  - **Tx (2):**
    - **10 Gb/s full swing**
    - **10 Gb/s reduced swing**
  - **Tx-channel-Rx (12):**
    - **Channel realized on-chip, emulates Si carrier channel**
  - **Emulated channel measurement macro**

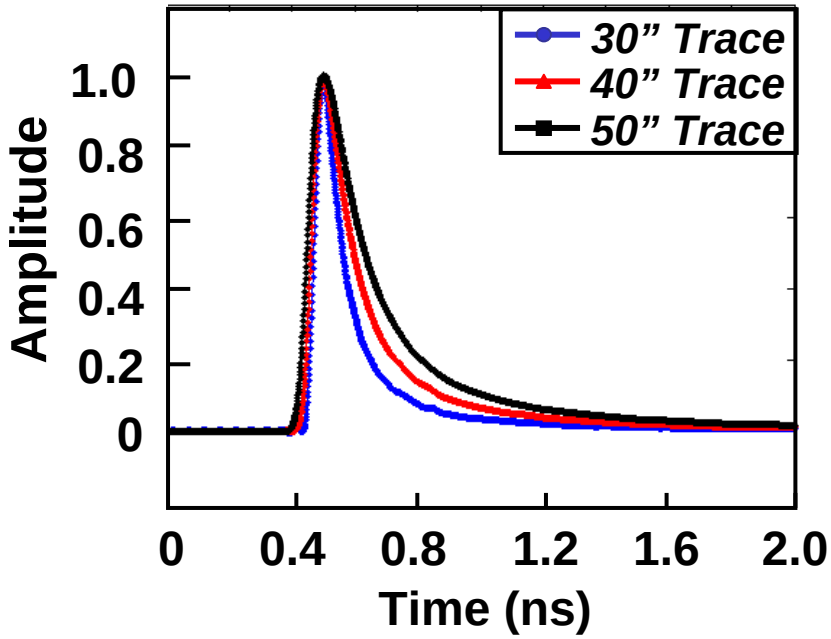
Si Carrier-like Channels: Lossy PCB Traces



PCB Traces



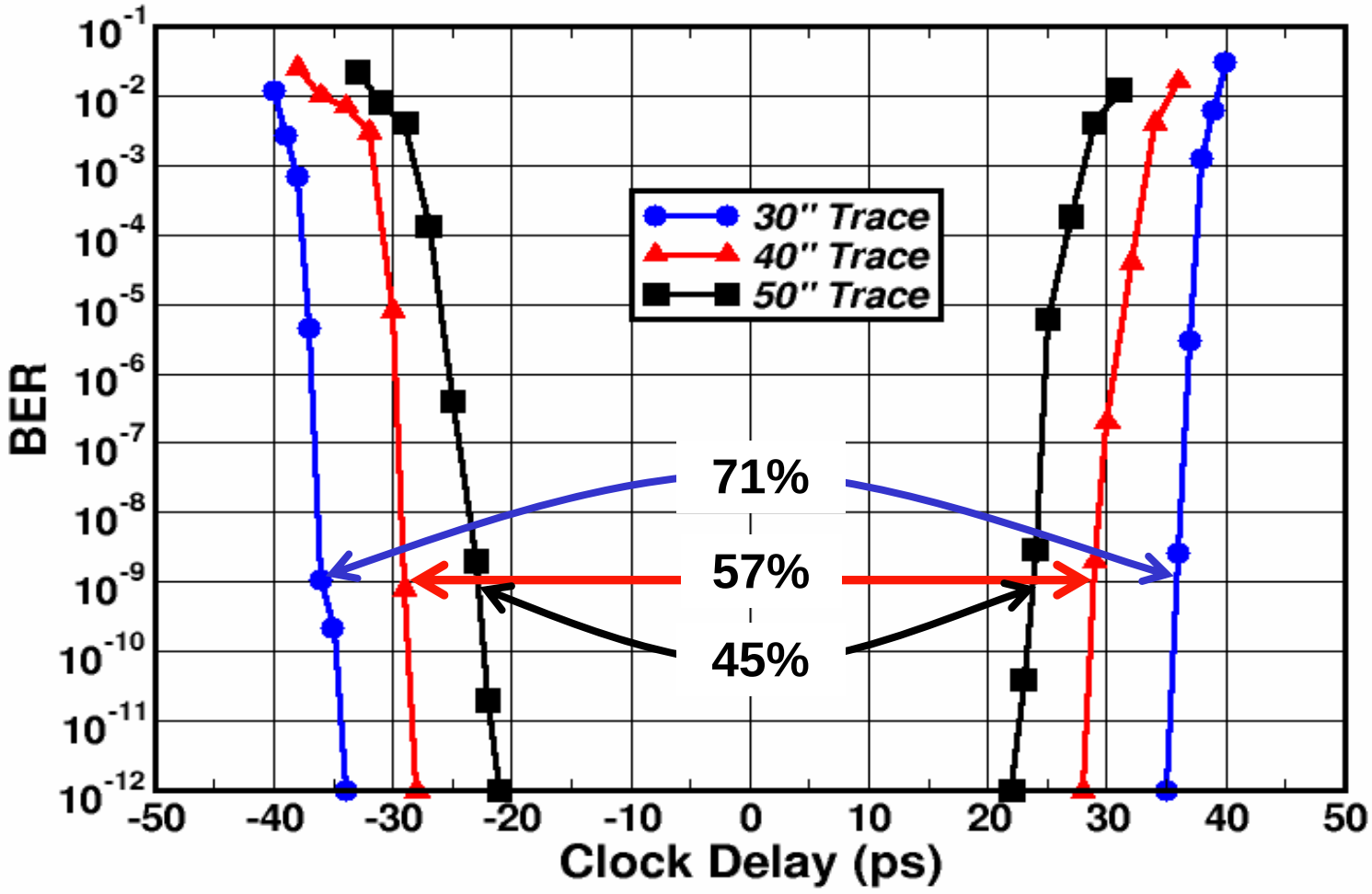
Transfer functions



Impulse responses

Note: setup adds ~2 dB additional loss

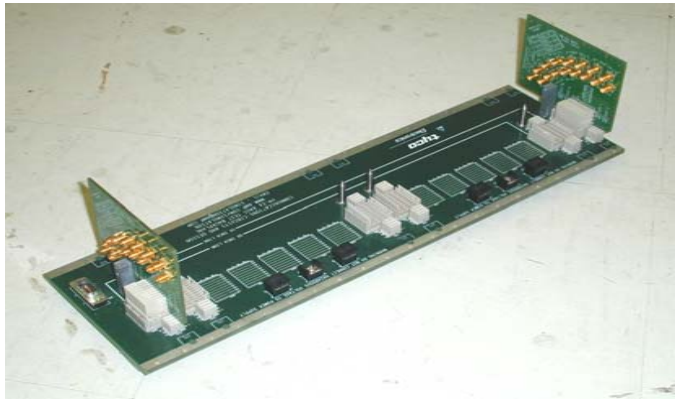
Stand-Alone DFE-IIR Rx Performance: PCB Traces



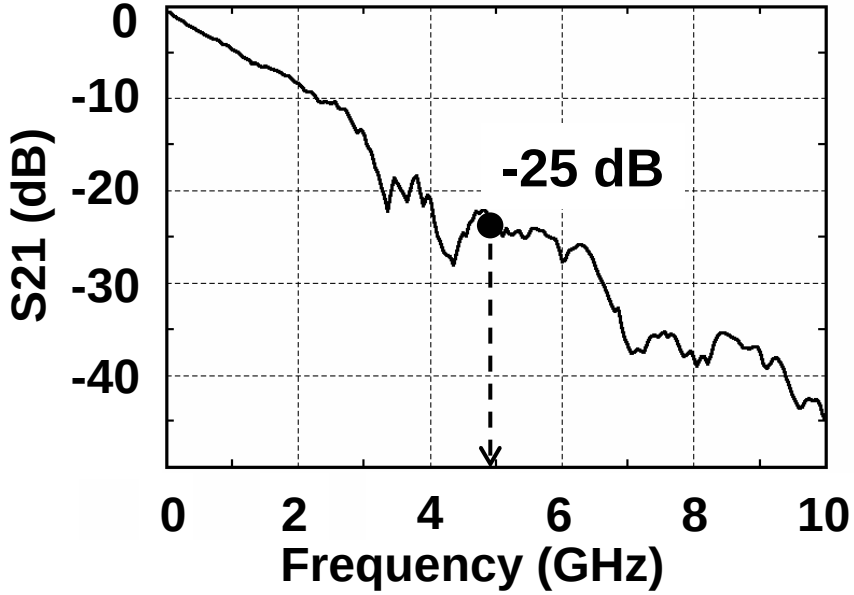
Bathtub curves (PRBS7) @ 10 Gb/s

- **Power dissipation: 7 mW from 1.0 V power supply**

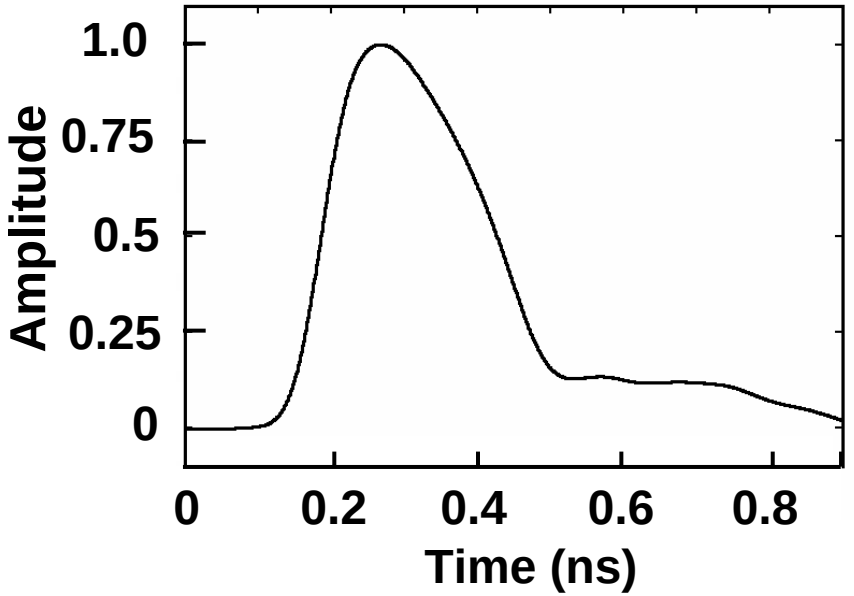
16” Tyco Backplane Channel



Backplane Channel



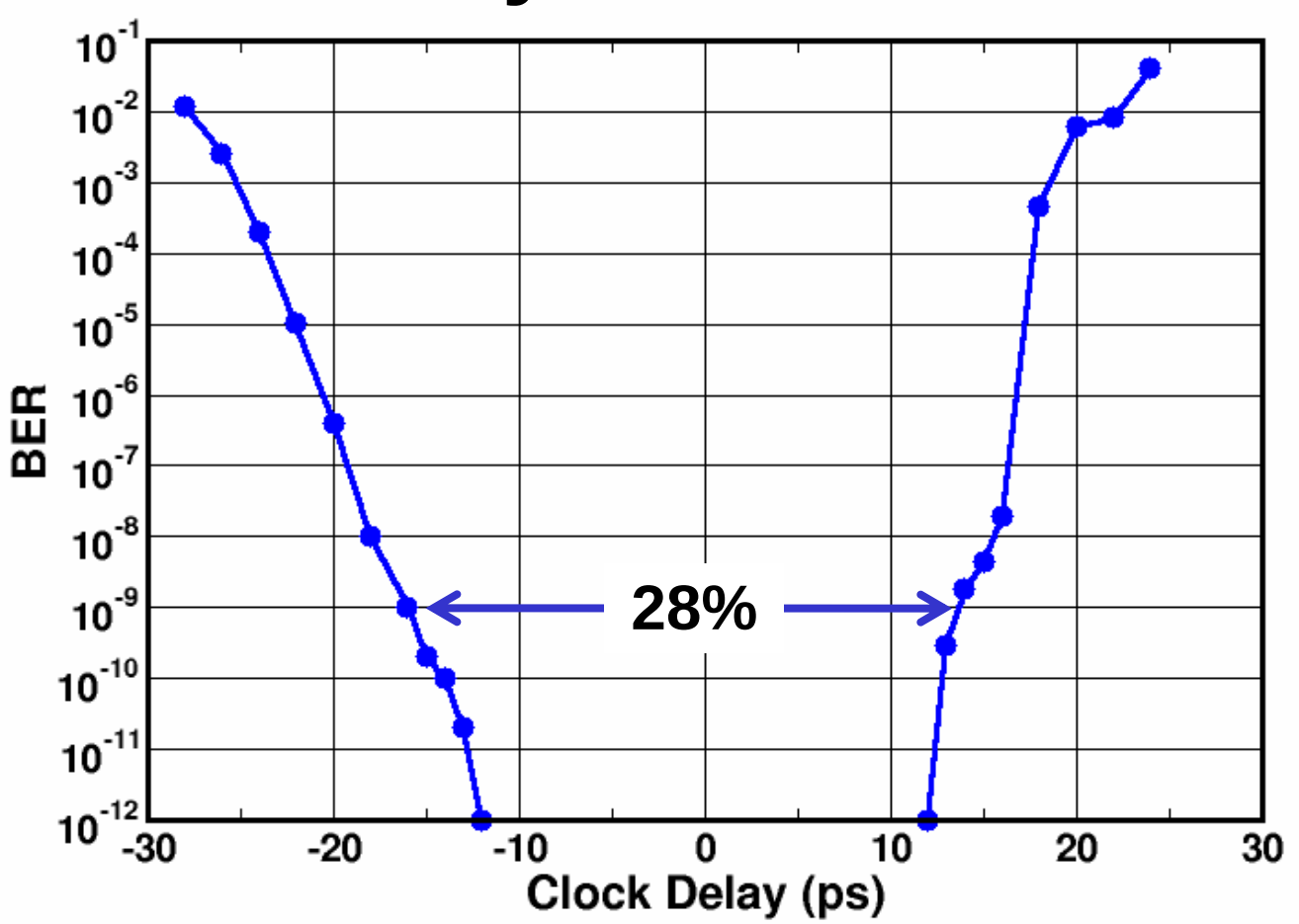
Transfer function



Impulse response

Note: setup adds ~2 dB additional loss

Stand-Alone DFE-IIR Rx Performance: 16” Tyco Channel



Bathtub curve (PRBS7) @ 10 Gb/s

- **Power dissipation: 7 mW from 1.0 V power supply**

Stand-Alone Test Sites Results Summary

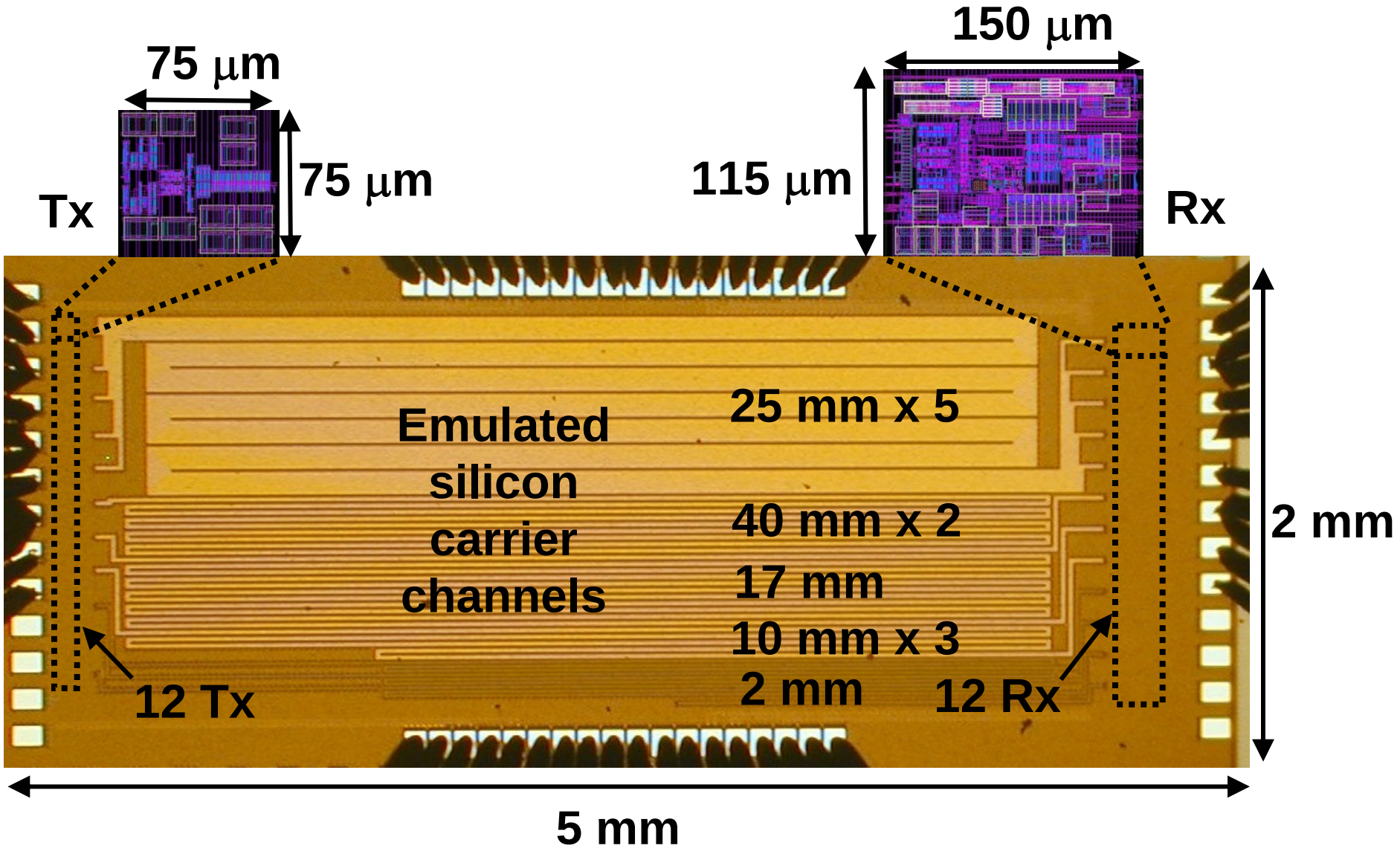
- **Tx: full/reduced swing designs fully functional 10.8 Gb/s**
- **Rx: DFE-IIR fully functional (open eye: 13 Gb/s) with 64 mVppd input sensitivity at 10 Gb/s**

Channel	Pattern	Horizontal eye opening (BER<1e-9) @ 10Gb/s	
		DFE-IIR [7mW from 1V]	2-tap DFE [7mW from 1V]
30” trace	PRBS7	*71%*	47%
	PRBS31	*57%*	24%
40” trace	PRBS7	*57%*	28%
	PRBS31	*41%*	Closed eye
50” trace	PRBS7	*45%*	Closed eye
16” Tyco	PRBS7	*28%*	Closed eye

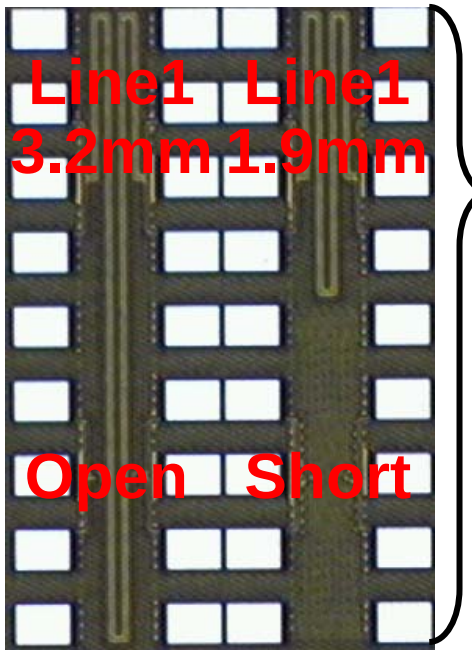
Carrier like PCB channels

Backplane channel

Tx–Emulated Channel–Rx Test Site

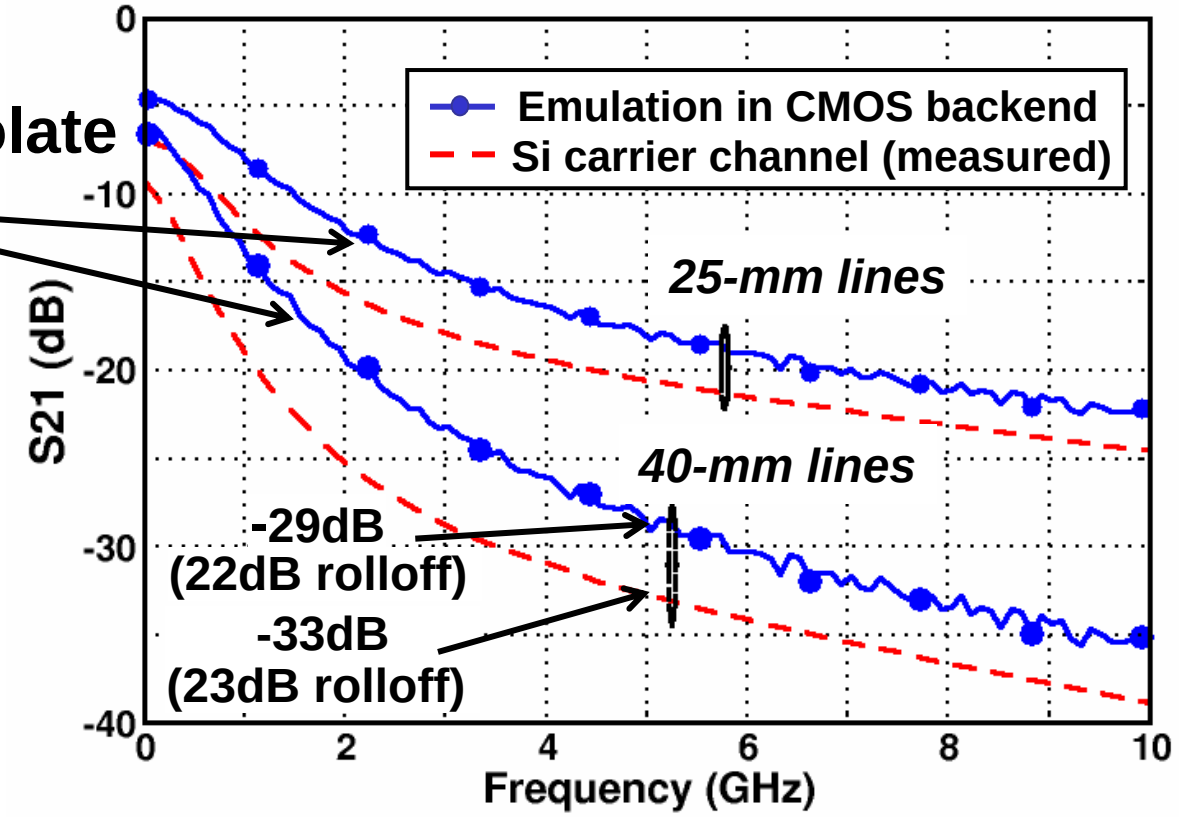


Emulated Channel Characterization



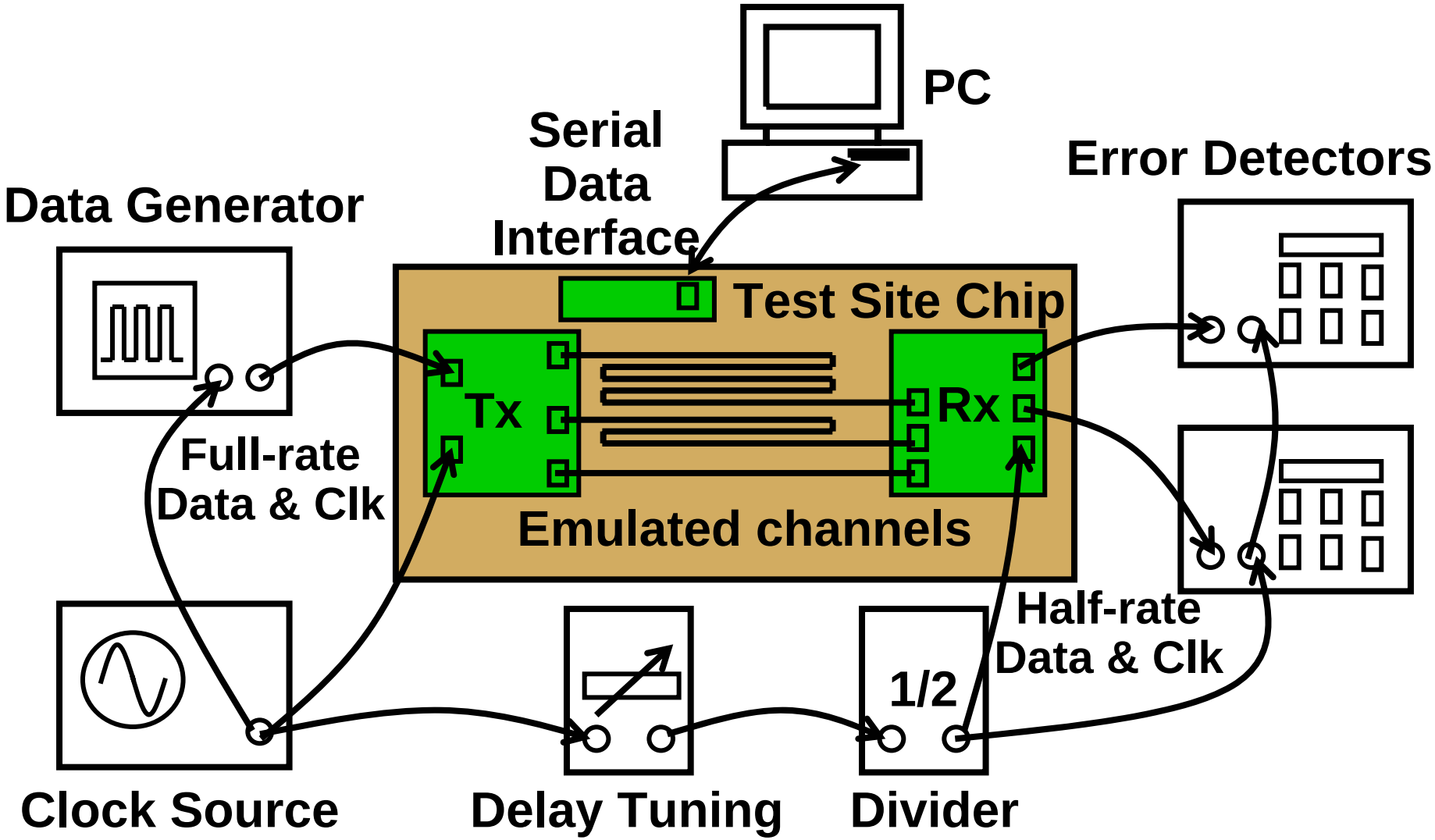
Channel macro

Extrapolate

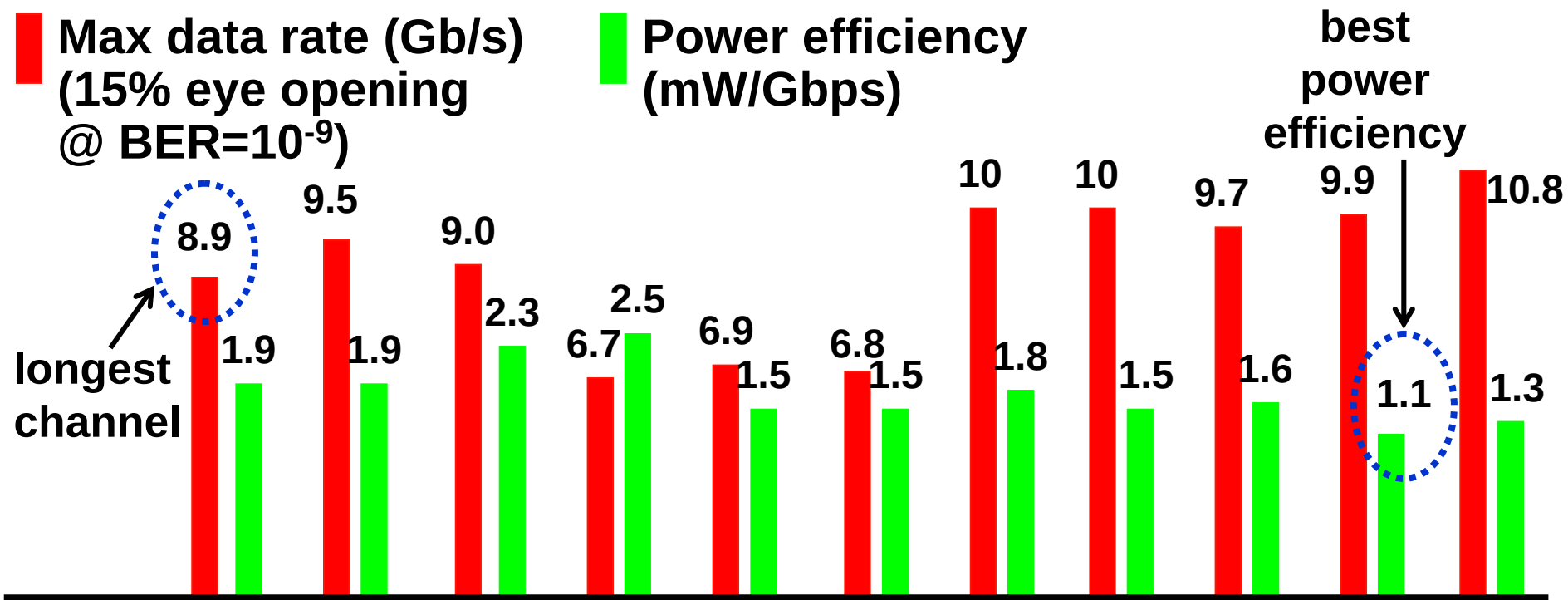


- **Goals:**
  - Characterize on-chip channel characteristics
  - Compare to actual carrier channel data to ensure results are relevant to target application

Tx- Emulated Channel-Rx Test Setup



Tx–Emulated Channel–Rx Test Results



TX	Full swing	Full swing	Full swing	Full swing	Reduced swing	Reduced swing	Full swing	Full swing	Full swing	Reduced swing	Reduced swing
Channel	40 mm	25 mm	25 mm	25 mm	25 mm	25 mm	17 mm	10 mm	10 mm	10 mm	2 mm
ESD	No	No	Yes	No	No	Yes	Yes	No	Yes	No	Yes
RX	DFE-IIR	DFE-IIR	DFE-IIR	2-tap DFE	DFE-IIR	DFE-IIR	DFE-IIR	2-tap DFE	2-tap DFE	2-tap DFE	2-tap DFE

Operation demonstrated across wide range of channels

Conclusions

- **Silicon carrier channel characteristics are well suited to**
  - **Low-Z Tx, high-Z Rx terminations**
  - **DFE-IIR based equalization approach**

- **DFE-IIR Rx performance demonstrated over range of channels**
  - **Smoothly varying PCB channels (>20 dB loss)**
  - **Legacy backplane: 16” Tyco channel (27 dB loss)**
  - **Emulated carrier channels, e.g., 40 mm (22 dB loss) @ 8.9 Gb/s, 1.9 mW/Gbps**

Acknowledgements

- **IBM Yorktown Research team:**
  - **Chirag Patel, Michael Beakes, Donald W. Beisser, Keith Jenkins, Ben Parker, Alexander Rylyakov, Daniel M. Kuchta, Arun S. Natarajan, Xiaoxiong Gu, Dong G. Kam, Zeynep Toprak Deniz, Sudhir Gowda, and Mehmet Soyuer**

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