20.6 A 6Gb/s Receiver with 32.7dB Adaptive DFE-IIR Equalization

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To ensure the signal integrity over a lossy channel, an analog equalizer and/or a decision-feedback equalizer (DFE) [2-6] are widely adopted in high-speed data transmission. An adaptive analog equalizer or adaptive DFE is also attractive to compensate the frequency-dependent loss due to the different channel lengths and environment variations. Conventionally, a multiple-tap DFE is adopted to compensate the inter-symbol interference (ISI), which is induced by postcursors due to the non-ideal channel impulse responses. To avoid the power and area penalty due to many postcursors, a DFE with infinite impulse response (IIR) filter feedback [2] has been presented. In [2], no adaptation scheme ensures that such IIR filter cancels the postcursors precisely, i.e., its RC time constant and amplitude need to be manually adjusted. In this work, a 6Gb/s receiver using a DFE with an adaptive continuous-time IIR filter and a clock/data recovery (CDR) circuit is presented. In a high loss environment, a conventional digital qaudricorrelator frequency detector (QFD) may fail due to the significant data dependent jitter. To integrate an adaptive DFE with a CDR circuit, a proposed frequency-sweeping frequency detector (FD) and a lock detector (LD) are presented in this work.

The receiver is shown in Fig. 20.6.1. It consists of a DFE with an IIR filter, a CDR circuit with the proposed frequency-sweeping FD and LD, an adaptive loop, and latches. When this CDR circuit does not lock, the LD disables the adaptive loop and the IIR filter. The proposed frequency-sweeping FD aids the CDR circuit to lock. When the output "Lock" of the LD goes high, it enables the adaptive loop and the IIR filter.

The DFE with a first-order continuous-time IIR filter is shown in Fig. 20.6.2. The summer is realized by a differential amplifier with resistive loads and RC source degeneration. The time constant and amplitude of this first-order continuous-time IIR filter are adjusted by a PMOS transistor and a NMOS one, respectively. The adaptive algorithm is realized by detecting data and edge information [1], as shown in Fig. 20.6.3. The normalized pulse responses before and after equalization are shown Fig. 20.6.3, where Tb is the bit time. To adjust the amplitude of this IIR filter, a special pattern of "110" is detected. For three sequent data (D2, D1, D0) is "110", the ISI at the edge E0 is given as

$$ISI_{E0} = h(1.5Tb)+h(0.5Tb)-h(-0.5Tb) \quad (1)$$

where the first two terms are postcursors and the last one is the precursor. If the sampled result ISI_{E0} is high, it implies the amplitude of this IIR filter should be increased and vice versa. To adjust the time constant of this IIR filter, a special pattern '1110' is detected. For four sequent data (D3, D2, D1, D0) is "1110", the ISI at the edge E0 is given as

$$ISI_{E0}=h(2.5Tb)+h(1.5Tb)+h(0.5Tb)-h(-0.5Tb) \quad (2)$$

If the sampled result ISI_{E0} is high, it implies the time constant of this IIR filter should be increased and vice versa. Once both the time constant and amplitude loops converge, Eq. (1) and Eq. (2) will be close to zero. Two equalities are obtained as

$$h(-0.5Tb)=h(0.5Tb)+h(1.5Tb) \;\&\; h(2.5Tb)=0 \quad (3)$$

By h(-0.5Tb)=h(0.5Tb)+h(1.5Tb), to adjust the amplitude of this IIR filter is equivalent to tune the tap weighting to cancel the ISI. By h(2.5Tb)=0, a long pulse response tail due to a high-loss channel is compensated. To adjust the RC time constant of this IIR filter, it is helpful to decrease the ISI due to a long pulse response tail and it is equivalent to have a multiple-tap DFE.

The CDR circuit consists of a conventional Alexander phase detector, a voltage-to-current converter (VIC), a loop filter, a proposed frequency-sweeping FD, and the LD. In Fig. 20.6.1, the first 7 latches (L1~L7) and two XOR gates realize the Alexander phase detector. The last 5 latches (L8~L12) with several logic gates, two voltage-to-current converters (VICs), two PMOS switches, and two capacitors realize the adaptive loop. When the signal "Lock" is low, the PMOS switches are on to disable the adaptive loop. As the channel loss exceeds 10dB, the conventional QFD may fail to work due to a large data dependent jitter. The proposed frequency-sweeping FD is presented to avoid this problem as shown in Fig. 20.6.4(a). When the signal "Lock" of the LD is low, this FD injects a constant current to charge or discharge the loop filter. It is equivalent to sweep the control voltage of a VCO within the high-level voltage of V_H and the low-level voltage of V_L. As the VCO's is sweeping to the vicinity of the target frequency, the LD disables the proposed FD and the Alexander PD takes over to complete the acquisition. This FD does not need a quadrature clock compared with a conventional QFD. The LD is shown in Fig. 20.6.4(b). The data are sampled by the clock CK and a delayed one CK_d with a time difference of 20ps. The results are compared and calculated by a 6-bits asynchronous counter. If the clock frequency is far from data rate, the clocks CK and CK_d will drift toward left or right in the eye diagram. As they drift to the edge of the eye diagram, their sampled results may be different within 64 bits. This asynchronous counter is reset, so the signal "Lock" still stays low. While their sampled results are the same within 64 bits, which means clock frequency is close to the data rate, the signal "Lock" goes high, and the LD disables the frequency-sweeping FD.

In this work, three different trace lengths of 60cm, 140cm, and 340cm are realized by the FR4 boards and their measured channel loss at 3GHz is 9.0dB, 15.0dB, and 32.7dB, respectively, as shown in Fig. 20.6.1. Figures 20.6.5(a) and Fig. 20.6.5(b) show the measured eye diagram before and after equalization under the above different channels. The measured rms jitters of the recovered data are 3.68ps, 3.97ps, and 4.16ps, respectively. The measured peak-to-peak jitters are 24.44ps, 26.67ps, and 27.78ps, respectively. The measured bit-error-rate is less than 10^{-12} for all the cases under a PRBS of 2^7-1.

The measured locking transient of the CDR circuit and the adaptive loop are shown in Fig. 20.6.6(a). This CDR circuit and the adaptive loop smoothly converge. The locking time of the CDR circuit, the time constant control, and the amplitude control of the adaptive loop are 9us, 160us, and 150us, respectively.

The die photo is shown in Fig. 20.6.7. It is fabricated in 90nm CMOS process. The total active area of this receiver is 0.089mm^2. The power consumption is 52mW, where the DFE and CDR dissipate 4mW and 48mW, respectively. Fig. 20.6.6(b) shows performance summary compared to that of the prior arts. The maximum loss is up to 32.7dB without an additional linear equalizer on a receiver and the pre-emphasis on a transmitter. This receiver has the outstanding equalization ability with the aid of the proposed adaptive algorithm.

Acknowledgements:
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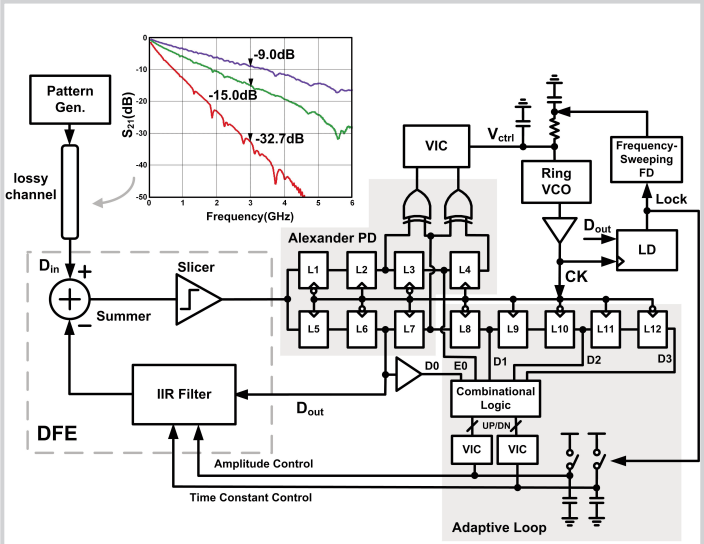


Figure 20.6.1: A receiver using a CDR circuit and an adaptive DFE-IIR.

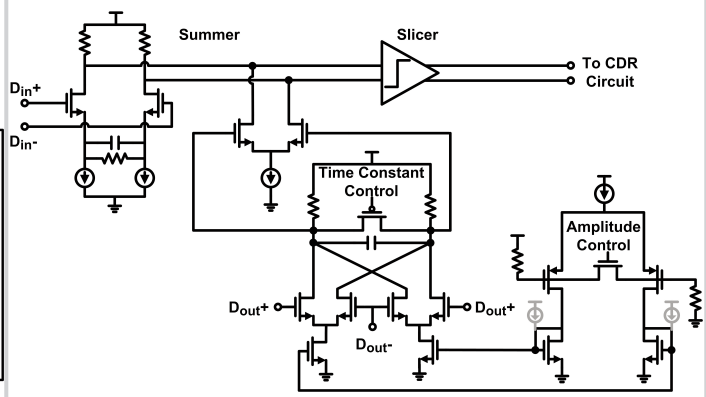
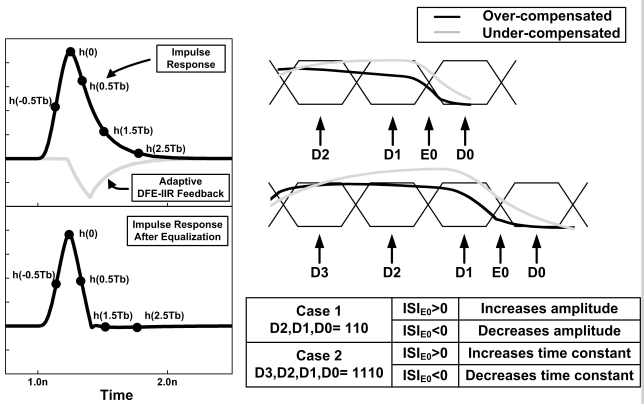


Figure 20.6.2: A DFE with an adaptive IIR filter.



Case 1 D2,D1,D0= 110	$ISI_{E0}>0$	Increases amplitude
	$ISI_{E0}<0$	Decreases amplitude
Case 2 D3,D2,D1,D0= 1110	$ISI_{E0}>0$	Increases time constant
	$ISI_{E0}<0$	Decreases time constant

Figure 20.6.3: Adaptive algorithm.

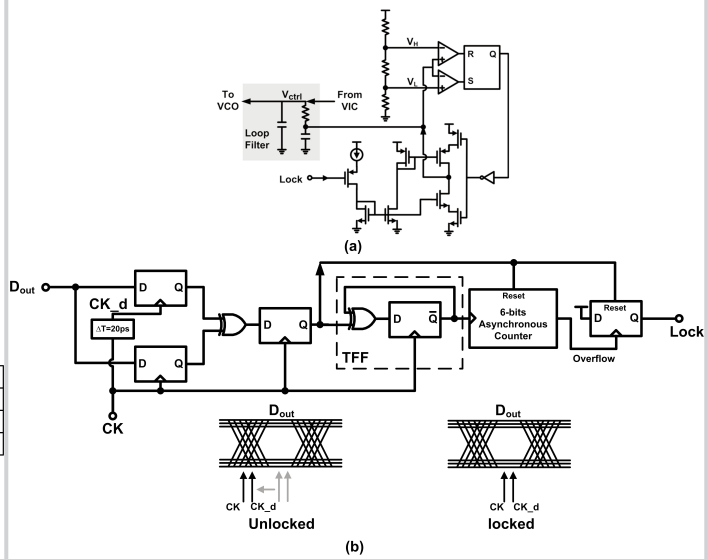


Figure 20.6.4: (a) Proposed frequency-sweeping FD, (b) proposed LD.

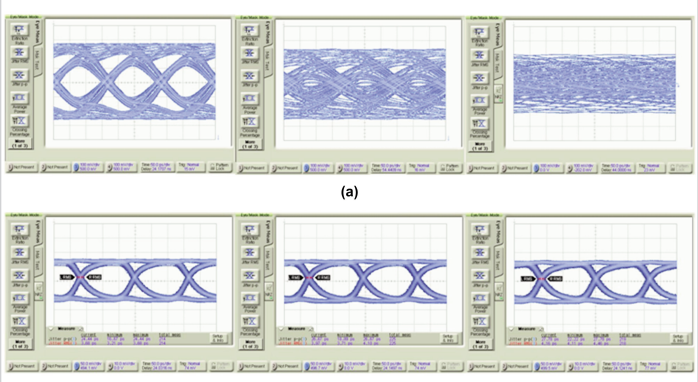
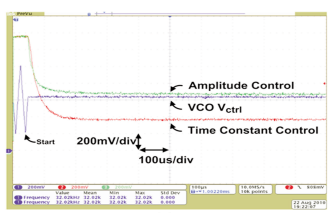


Figure 20.6.5: (a) Measured eye diagrams for 60cm, 140cm, and 340cm traces on FR4 board before equalization, (b) after equalization.



	[2]	[3]	[4]	[5]	[6]	This Work
Technology	65nm CMOS	65nm CMOS	90nm CMOS	130nm CMOS	130nm CMOS	90nm CMOS
DFE architecture	2 tap half-rate DFE-IIR	5 tap half-rate Current-Integrating	2 tap half-rate Current-Integrating	5 tap full-rate	4 tap full-rate	1 tap full-rate DFE-IIR
Adaptation	No	Yes	No	Yes	Yes	Yes
Data rate	10Gb/s	11.1Gb/s	7Gb/s	6.4Gb/s	6.25Gb/s	6Gb/s
Rx equalization	-27dB	-28dB	-15dB	-24.4dB	-20dB	-32.7dB
DFE power	7mW	N/A	9.3mW	N/A	N/A	4mW
Rx power	N/A	78.2mW	N/A	290mW*	180mW	52mW
Area	0.017mm^2	0.220mm^2	0.019mm^2	0.790mm^2*	0.240mm^2	0.089mm^2

*Include Tx

(b)

Figure 20.6.6: (a) Measured locking transient of the CDR circuit and the adaptive loop, (b) performance summary.

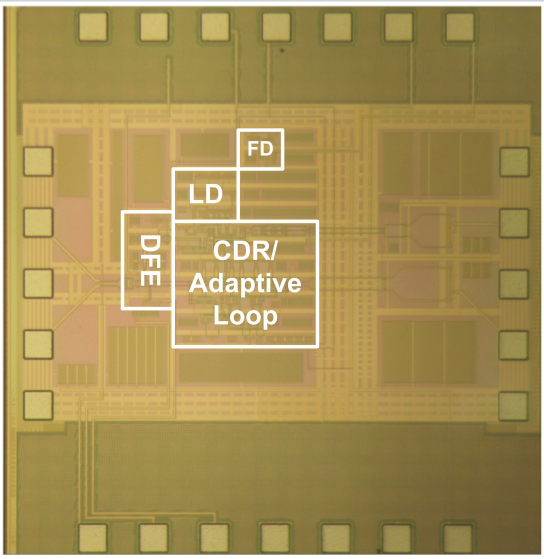


Figure 20.6.7: Die Photograph.

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