

# IBM90nm – FO4 Delay

ECEN689 High Speed I/O

Dr Samuel Palermo

Ref : Dr Silva [EE474 Lab manuel]

## Starting Cadence for the First Time

### -Course Directory : /mnt/lab\_files/ECEN689\_605

1. Make EE689 folder in your home director : mkdir ECEN689
2. Go to the EE689 : cd ECEN689
3. Copy model(directory), cds.lib(file), and ncsu from course directory

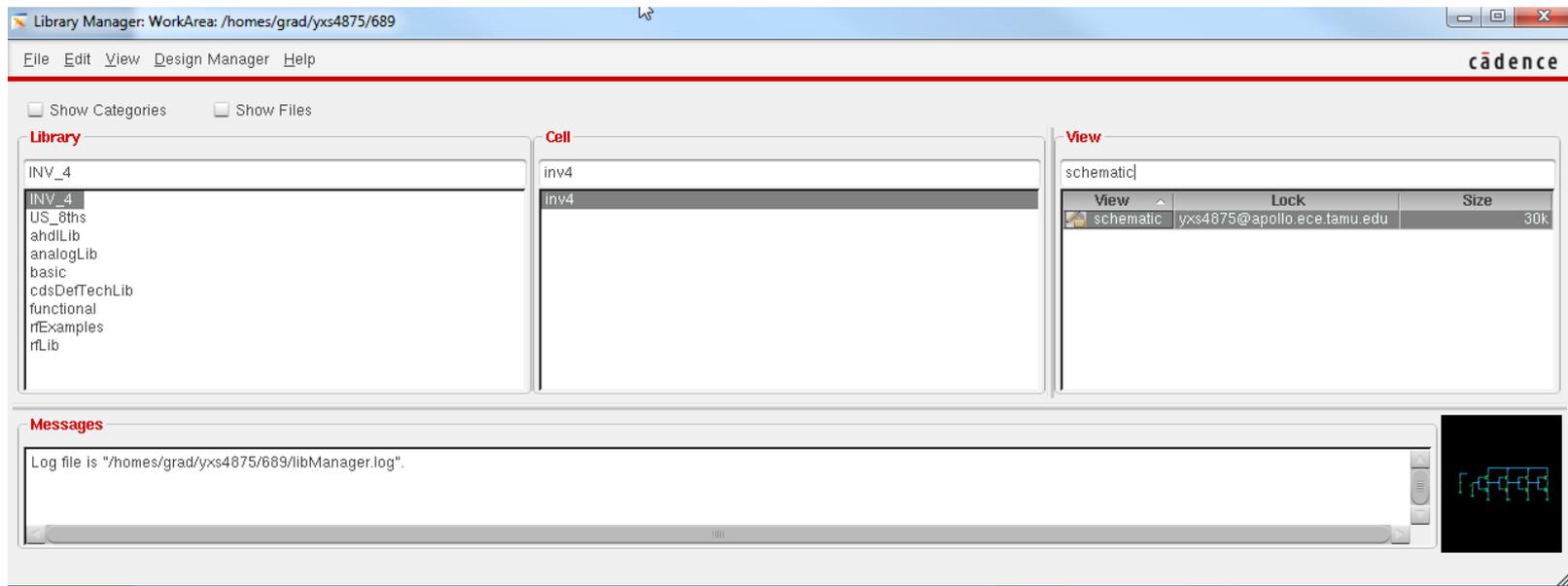
```
cp -rf /mnt/lab_files/ECEN689_605/model .  
cp -rf /mnt/lab_files/ECEN689_605/cds.lib .  
cp -rf /mnt/lab_files/ECEN689_605/ncsu .
```

4. Run cadence => ./ncsu

```
[rdliu918]@hera3 ~-> (21:00:14 01/24/21)  
:: cd ECEN720/  
  
[rdliu918]@hera3 ~/ECEN720> (21:01:36 01/24/21)  
:: cp -rf /mnt/lab_files/ECEN689_605/cds.lib .  
  
[rdliu918]@hera3 ~/ECEN720> (21:02:02 01/24/21)  
:: cp -rf /mnt/lab_files/ECEN689_605/ncsu .  
  
[rdliu918]@hera3 ~/ECEN720> (21:02:10 01/24/21)  
:: cp -rf /mnt/lab_files/ECEN689_605/model .  
  
[rdliu918]@hera3 ~/ECEN720> (21:02:17 01/24/21)  
:: ./ncsu  
[1] 35942  
  
[rdliu918]@hera3 ~/ECEN720> (21:02:22 01/24/21)  
:: █
```

# Creating a Library

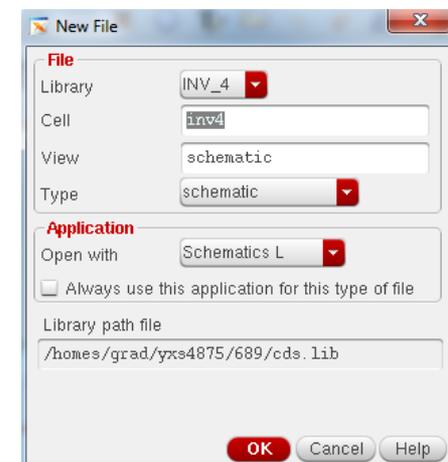
1. From the CIW select Tools → Library Manager to load the Library Manager



2. Do not Attach to an existing techfile due to using IBM90nm Model which is not support by cadence.

## Creating a Schematic

The first circuit we will design is a simple inverter. Select which library you want to put the cell into, in this case "INV4", and then File → New → Cell. Name your cell inverter. The tool you want to use here is Composer-Schematic



After selecting OK, the schematic window opens. We wish to add two transistors so that we can make an inverter. To do this we need to add an instance. You can do this by either clicking Add → Instance or by pressing “i” on the keyboard. A window titled “Component Browser” should pop up. Make sure that the library analogLib is selected. Select N\_Transistors and then nmos4. Go back to the schematic and select where you would like to add the NMOS transistor. Go back to the Component Browser and select P\_Transistors and then pmos4. Add this transistor to your schematic. Hit ESC to exit the Add Instance mode. Connect components together using wires. You can select Add → Wire or use the “w” hotkey. To change the properties of a device use Edit → Properties → Objects or use the “q” hotkey.

## MINIMUM W/L - 0.12um/0.10um

The screenshot displays the Virtuoso Analog Design Environment interface. The main window shows a schematic editor with an inverter circuit. The circuit includes a PMOS transistor (M1) and an NMOS transistor (M2) connected to a DVDD supply and ground. The PMOS transistor has a width of 2uM and a length of 100nM. The NMOS transistor has a width of 1uM and a length of 100nM. The circuit also includes a voltage source v1 (vdc) and a pulse source v0 (vpulse) connected to the gates of the transistors. The DVDD supply is connected to the drains of both transistors, and the gates are connected to each other and to the drain of the PMOS transistor.

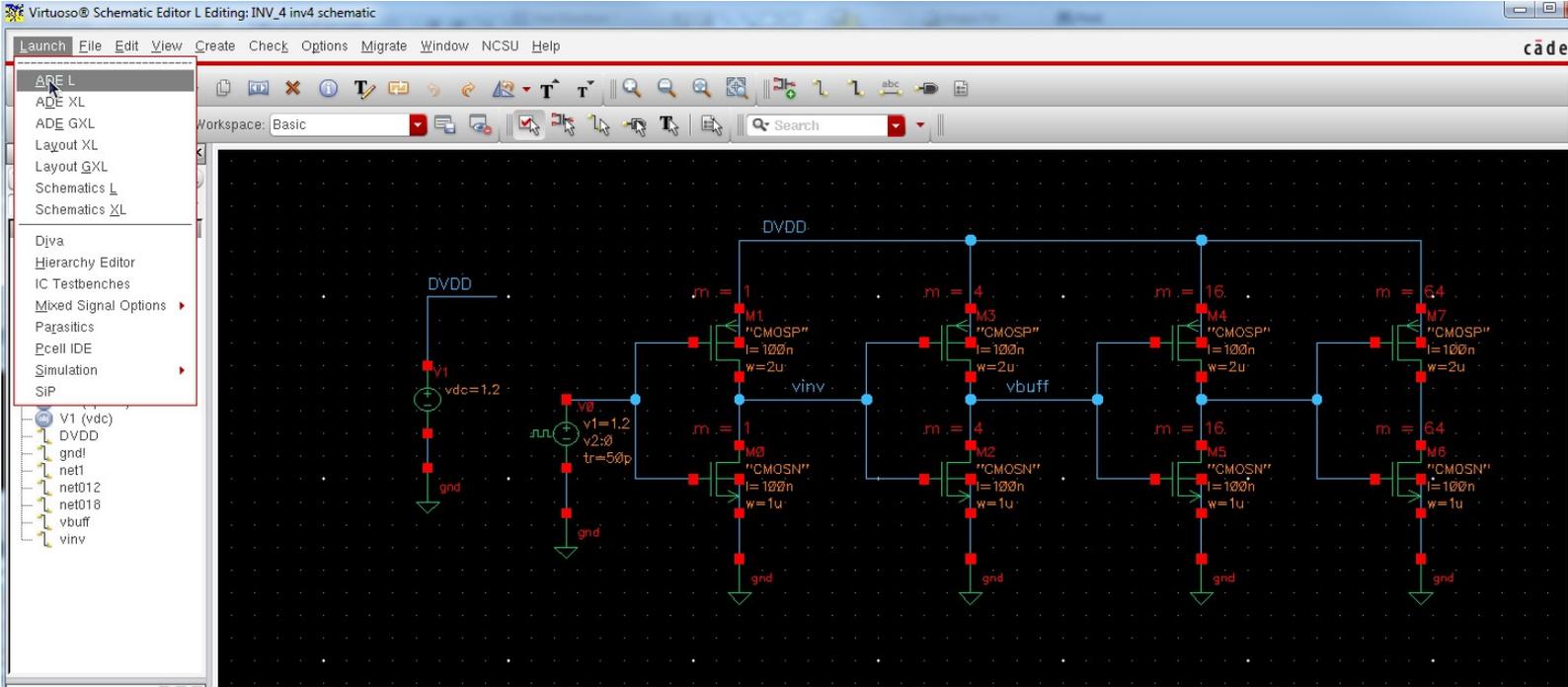
The 'Edit Object Properties' dialog box is open, showing the properties for the selected transistor instance (M1). The dialog box has the following fields and values:

View Name	Value	Display
View Name	symbol1	off
Instance Name	M1	off
CDF Parameter		
Model name	CMOSP	off
Width	2u M	off
Length	100n M	off
Source diffusion area		off
Drain diffusion area		off
Source diffusion periphery		off
Drain diffusion periphery		off
Drain diffusion res squares		off
Source diffusion res squares		off
Drain diffusion length		off
Source diffusion length		off
Multiplier	1	both

The Property Editor at the bottom left shows the following properties for the selected instance:

Instance	All
Model name	CMOSP
Width	2u M
Length	100n M
Source diff...	
Drain diff...	
Source diff...	

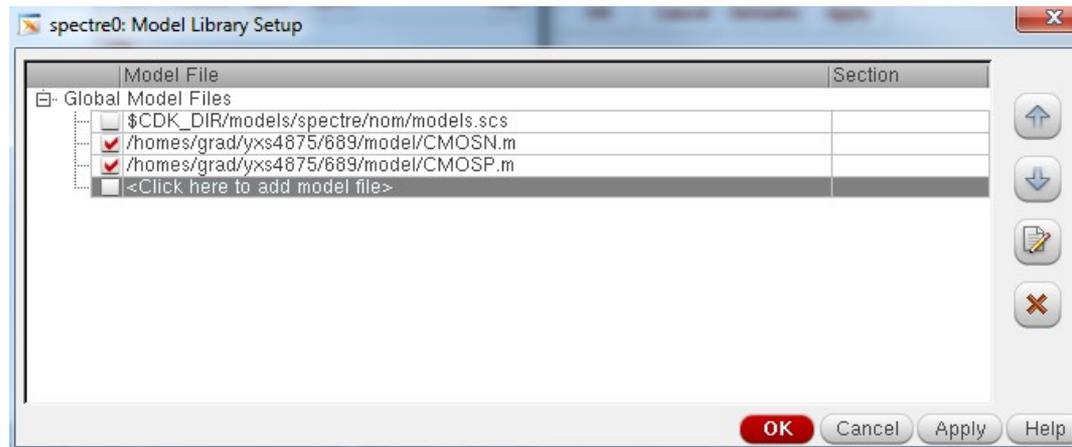
When finished, your schematic should resemble shown Figure to measure FO4 Delay.  
Select Design → Check and Save to save your schematic and make sure that there are no errors or warnings.



### Simulating the Schematic

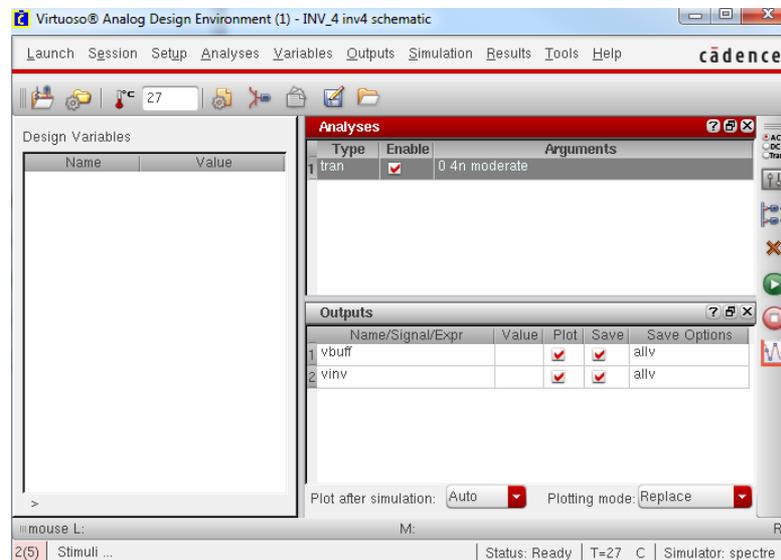
Start the simulator environment by selecting Launch → ADE L

Select Setup → Model path and add CMOSN.m and CMOSP.m



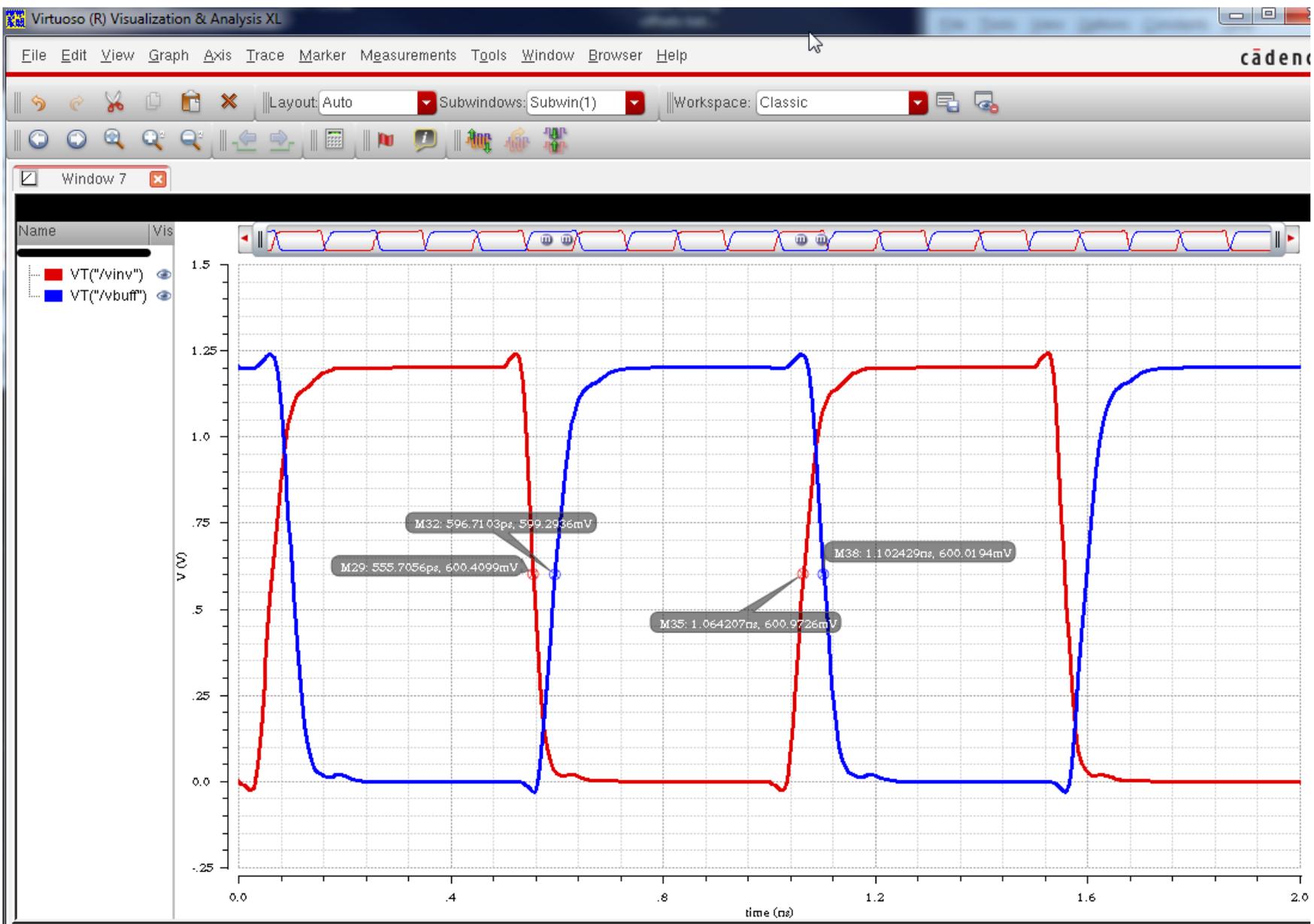
Next we need to configure the environment to run our first simulation. In the Analog Environment window select Analyses → Choose. Select “tran”

Select Simulation → Run or click on the green light in the bottom right corner. Once the simulation has completed, we can plot any outputs that we wish. To do this we use the calculator. To access the calculator, select Tools → Calculator in the Analog Environment.



# Simulation Result

FO4 delay for IBM90nm => 40ps



# How to use PRBS generator in Cadence

PRBS generator can be found in ahdlLib. It is called rand\_bit\_stream. Please specify a PRBS generator as shown in Figure 1. Please set seed to 128 for 7 bit PRBS.

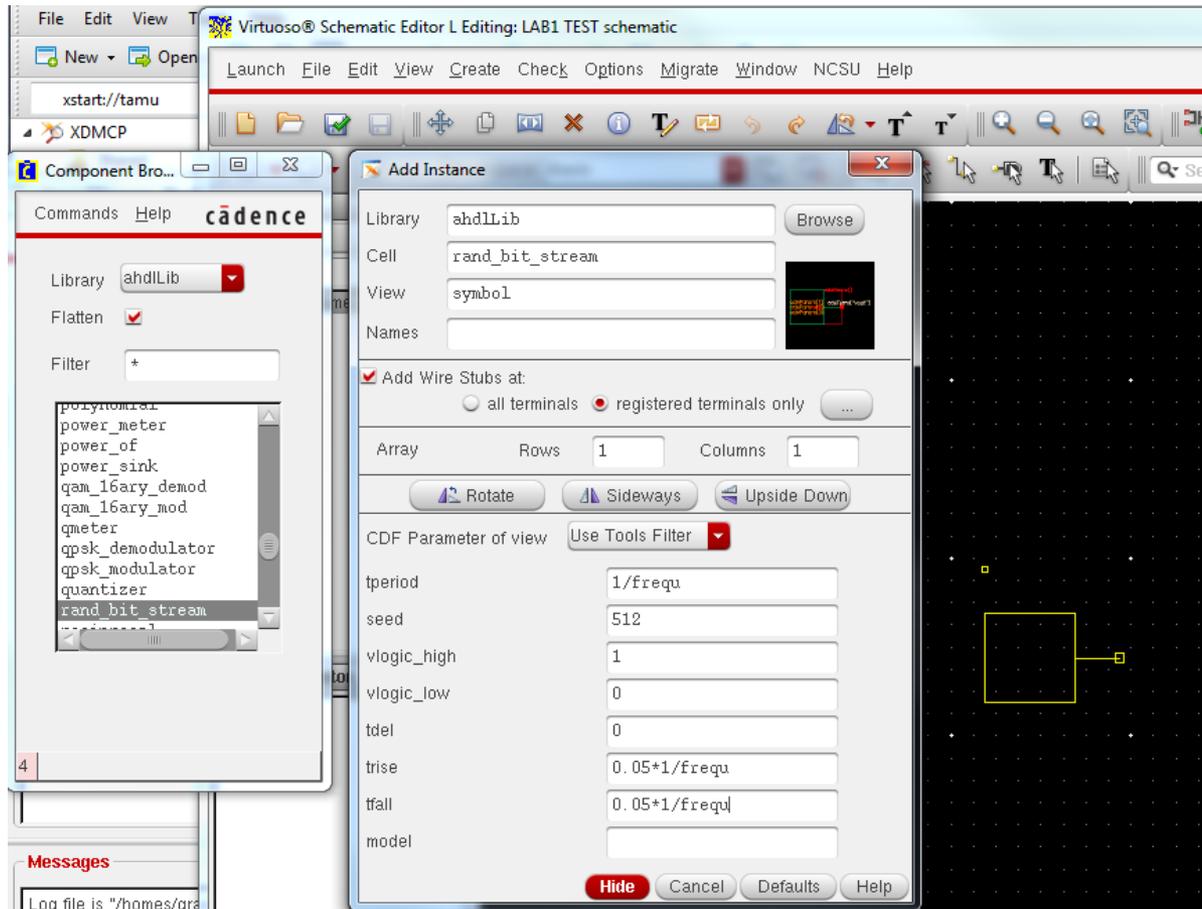
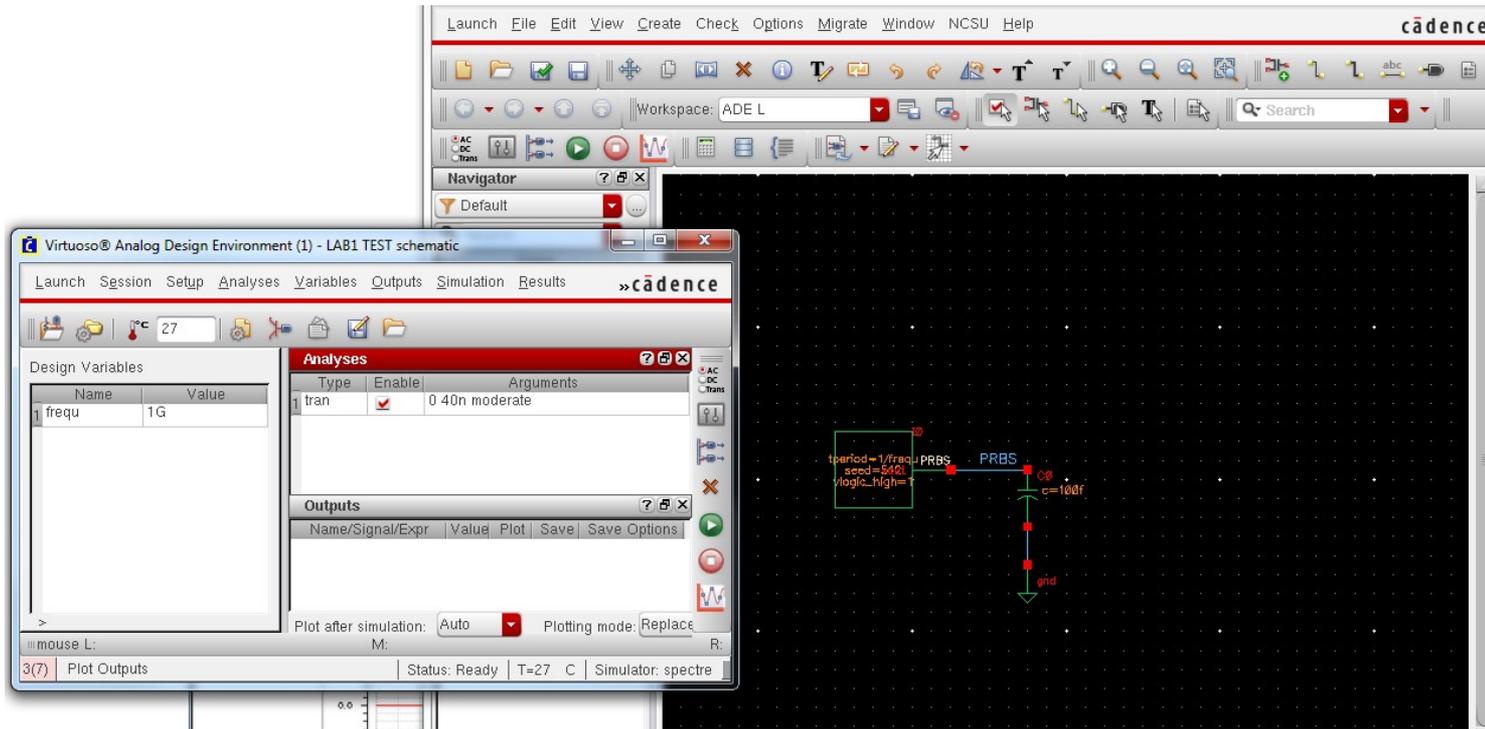


Figure 1 PRBS Generator Property

# Cadence Setup



# Simulation Result

