

IBM90nm – FO4 Delay

ECEN689 High Speed I/O

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Ref : Dr Silva [EE474 Lab manuel]

Note: There is a typo in the paths below.
It could be **/home**/faculty/.....
i.e. "home" not "homes"

Starting Cadence for the First Time

-Course Directory : /homes/faculty/shared/ECEN689_605

1. Make EE689 folder in your home director : `mkdir ECEN689`
2. Go to the EE689 : `cd ECEN689`
3. Copy model(directory), cds.lib(file), and ncsu from course directory

```
cp -rf /homes/faculty/shared/ECEN689_605/model .
```

```
cp -rf /homes/faculty/shared/ECEN689_605/cds.lib .
```

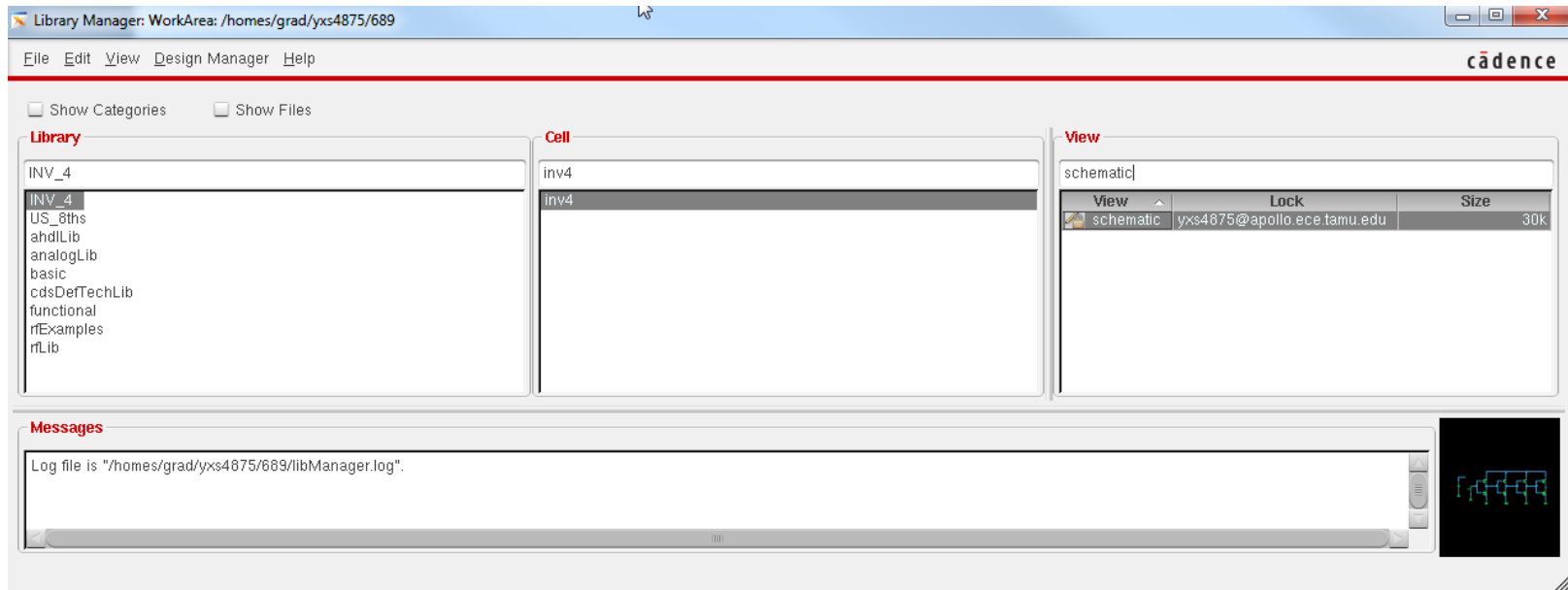
```
cp -rf /homes/faculty/shared/ECEN689_605/ncsu .
```

4. Run cadence => `./ncsu`

```
[yxs4875@apollo ~]$ cd ECEN689/  
[yxs4875@apollo ~/ECEN689]$ ll  
total 0  
[yxs4875@apollo ~/ECEN689]$ cp -rf /homes/faculty/shared/ECEN689_605/model .  
[yxs4875@apollo ~/ECEN689]$ cp -rf /homes/faculty/shared/ECEN689_605/cds.lib .  
[yxs4875@apollo ~/ECEN689]$ cp -rf /homes/faculty/shared/ECEN689_605/ncsu .  
[yxs4875@apollo ~/ECEN689]$ ll  
total 12  
-rwxr-xr-x 1 yxs4875 grad 62 Jan 27 12:41 cds.lib  
drwxr-xr-x 2 yxs4875 grad 4096 Jan 27 12:41 model  
-rwxr-xr-x 1 yxs4875 grad 261 Jan 27 12:41 ncsu  
[yxs4875@apollo ~/ECEN689]$ ./ncsu  
[1] 21064
```

Creating a Library

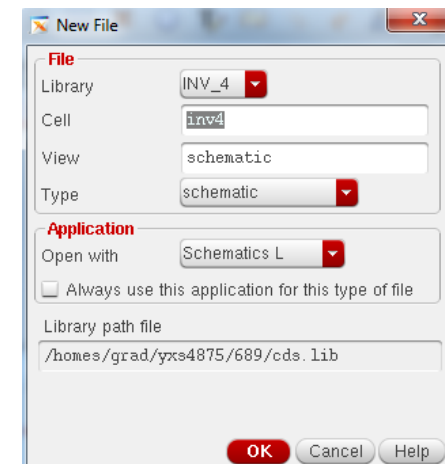
1. From the CIW select Tools → Library Manager to load the Library Manager



2. Do not Attach to an existing techfile due to using IBM90nm Model which is not support by cadence.

Creating a Schematic

The first circuit we will design is a simple inverter. Select which library you want to put the cell into, in this case "INV4", and then File → New → Cell. Name your cell inverter. The tool you want to use here is Composer-Schematic



After selecting OK, the schematic window opens. We wish to add two transistors so that we can make an inverter. To do this we need to add an instance. You can do this by either clicking Add → Instance or by pressing “i” on the keyboard. A window titled “Component Browser” should pop up. Make sure that the library analogLib is selected. Select N_Transistors and then nmos4. Go back to the schematic and select where you would like to add the NMOS transistor. Go back to the Component Browser and select P_transistors and then pmos4. Add this transistor to your schematic. Hit ESC to exit the Add Instance mode. Connect components together using wires. You can select Add → Wire or use the “w” hotkey. To change the properties of a device use Edit → Properties → Objects or use the “q” hotkey.

MINIMUM W/L - 0.12um/0.10um

The screenshot displays the Analog Design Environment (ADE) interface. The main window shows a schematic of an inverter circuit. The circuit includes a PMOS transistor (M1) and an NMOS transistor (M2) connected to a common drain node. The PMOS transistor is connected to DVDD, and the NMOS transistor is connected to ground. The input node is labeled v1 and the output node is labeled v2. The circuit is powered by DVDD and ground (gnd). The schematic also shows a voltage source V1 (vdc) and a pulse source V0 (vpulse).

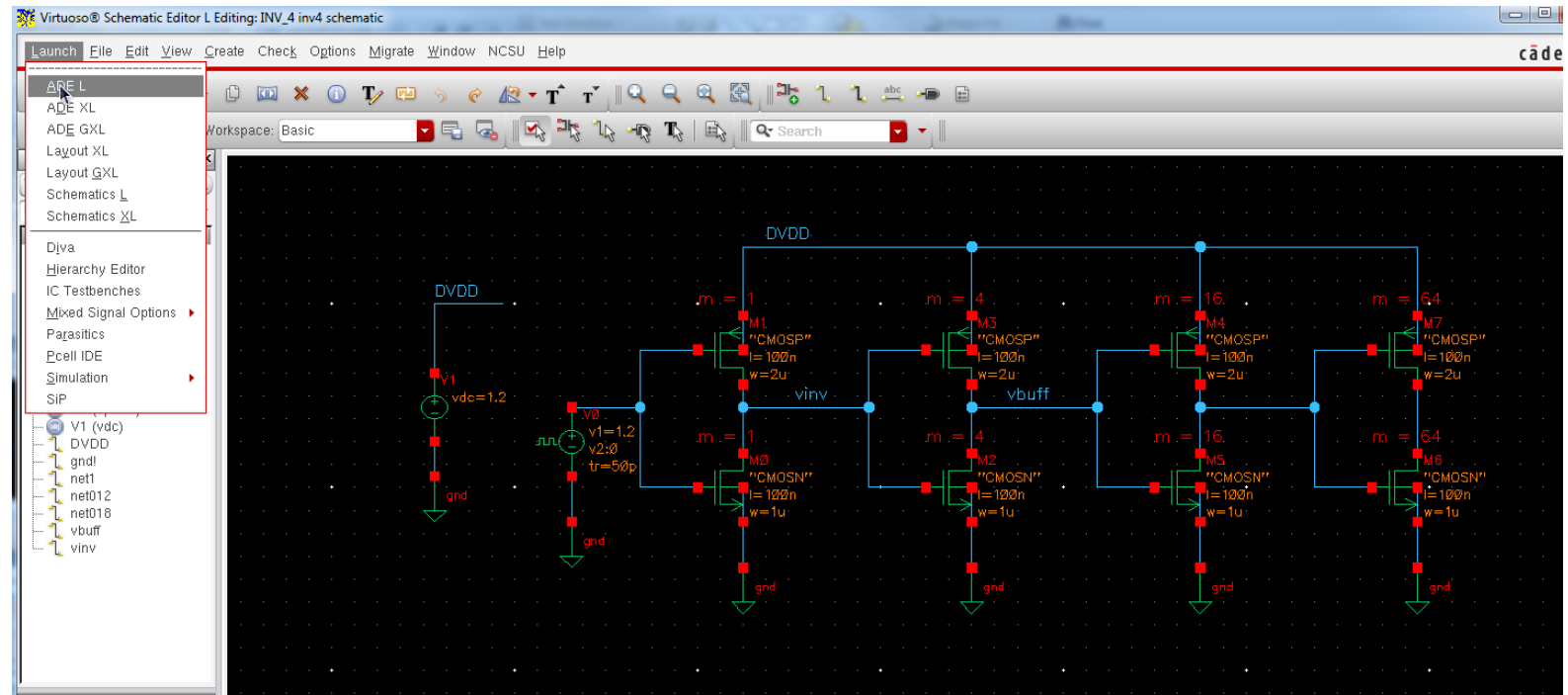
The **Edit Object Properties** dialog is open, showing the properties for a CMOS transistor. The dialog includes the following fields:

- View Name: syabo1
- Instance Name: M1
- CDF Parameter: Model name, Width, Length, Source diffusion area, Drain diffusion area, Source diffusion periphery, Drain diffusion periphery, Drain diffusion res squares, Source diffusion res squares, Drain diffusion length, Source diffusion length, Multiplier.
- Value: CMOSP, 2u M, 100n M, (empty), (empty), (empty), (empty), (empty), (empty), (empty), (empty), (empty), 1.
- Display: (empty), (empty), (empty), (empty), (empty), (empty), (empty), (empty), (empty), (empty), (empty), (empty).

The **Property Editor** at the bottom left shows the properties for the selected instance:

- Model name: CMOSP
- Width: 2u M
- Length: 100n M
- Source diff...: (empty)
- Drain diffus...: (empty)
- Source diff...: (empty)

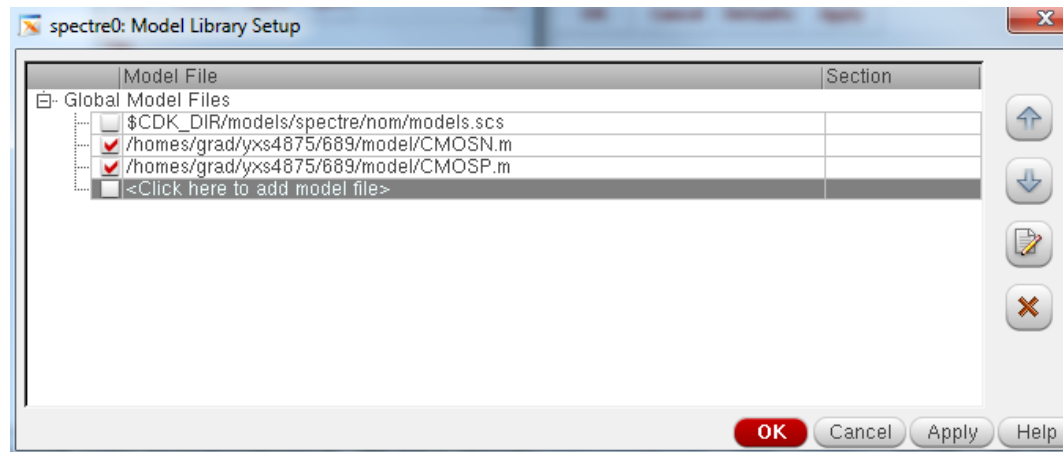
When finished, your schematic should resemble shown Figure to measure FO4 Delay.
Select Design → Check and Save to save your schematic and make sure that there are no errors or warnings.



Simulating the Schematic

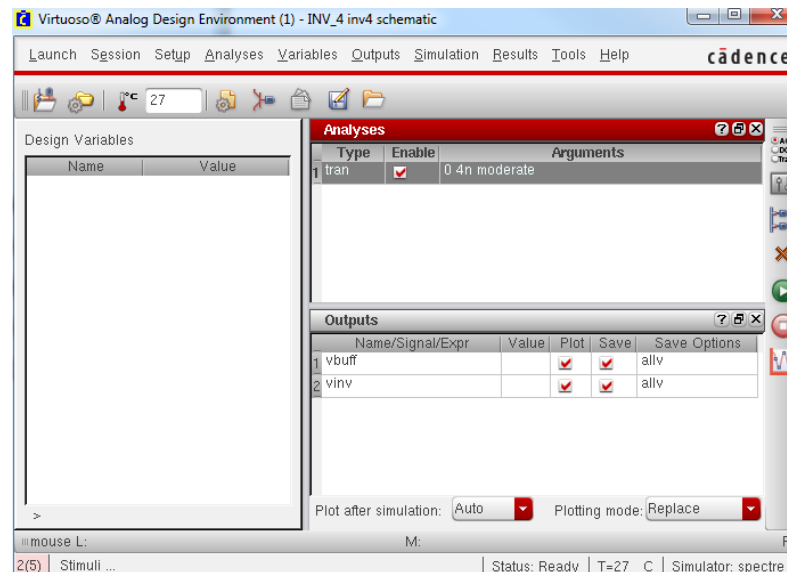
Start the simulator environment by selecting Launch → ADE L

Select Setup → Model path and add CMOSN.m and CMOSP.m



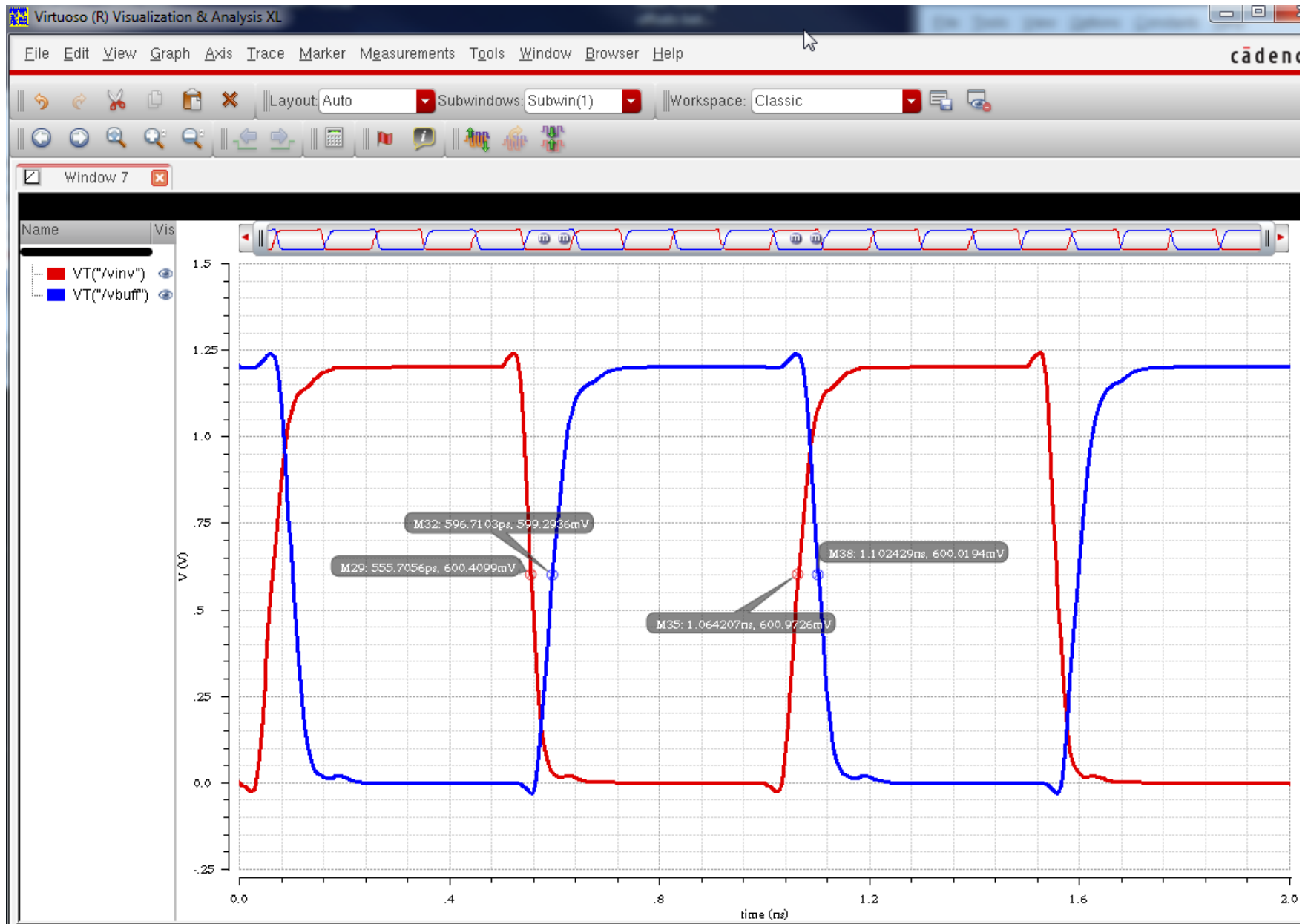
Next we need to configure the environment to run our first simulation. In the Analog Environment window select Analyses → Choose. Select “tran”

Select Simulation → Run or click on the green light in the bottom right corner. Once the simulation has completed, we can plot any outputs that we wish. To do this we use the calculator. To access the calculator, select Tools → Calculator in the Analog Environment.



Simulation Result

FO4 delay for IBM90nm => 40ps



How to use PRBS generator in Cadence

PRBS generator can be found in ahdlLib. It is called rand_bit_stream. Please specify a PRBS generator as shown in Figure 1. Please set seed to 128 for 7 bit PRBS.

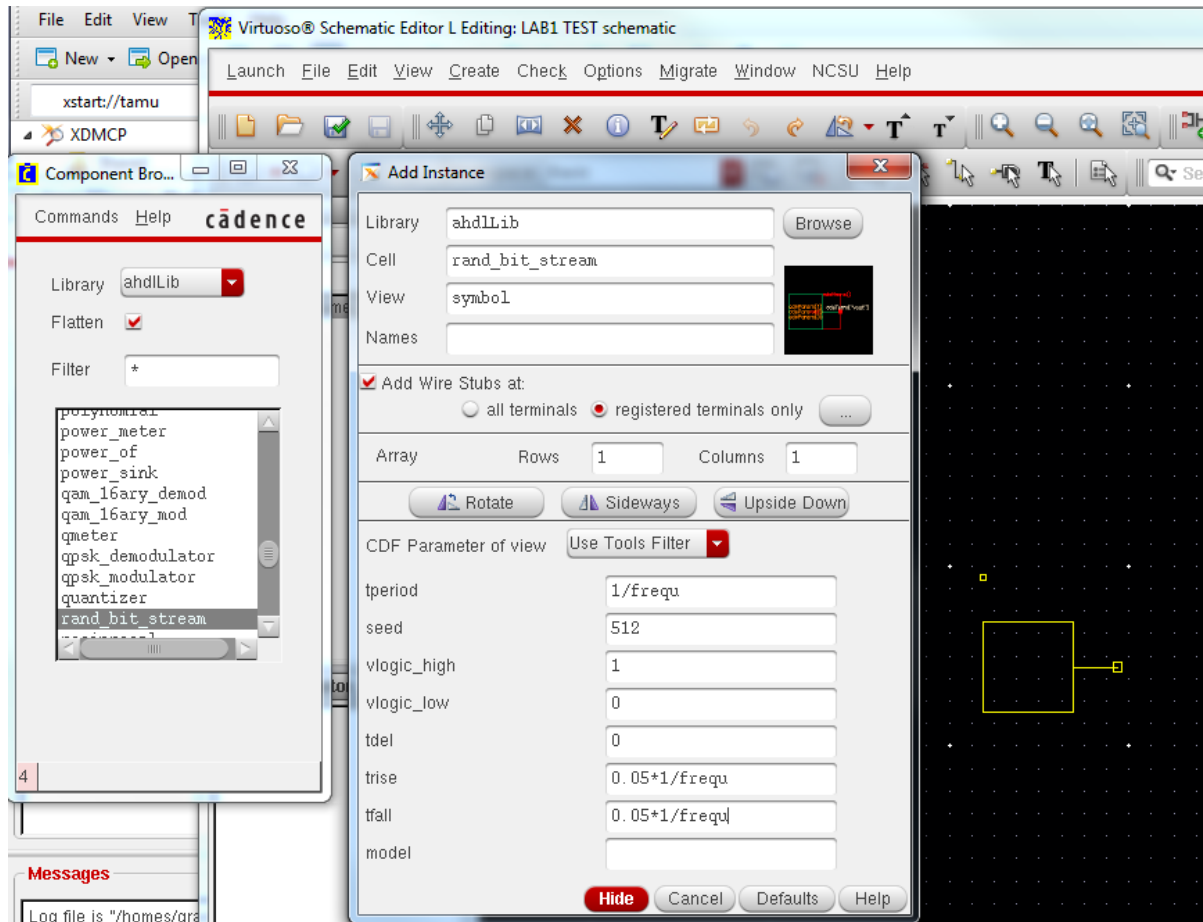
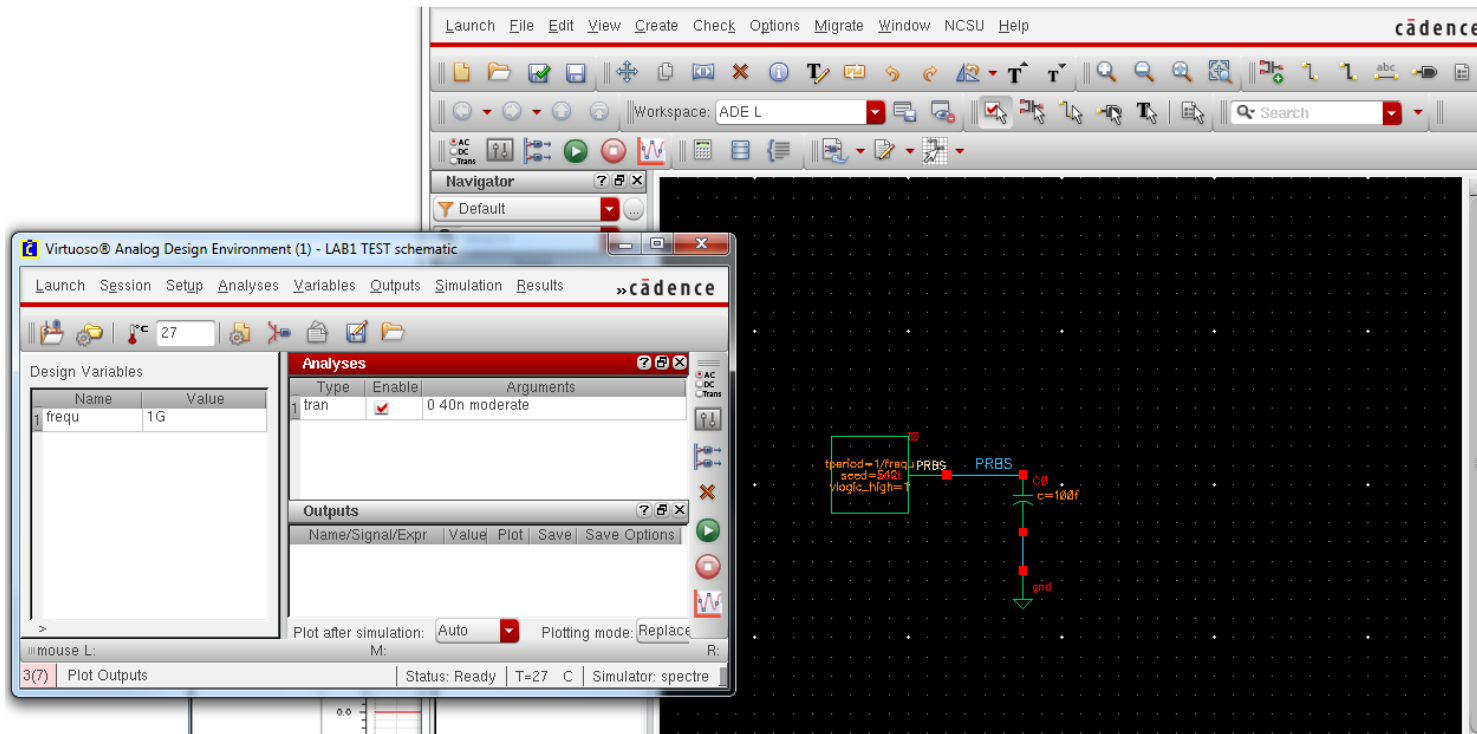


Figure 1 PRBS Generator Property

Cadence Setup



Simulation Result

