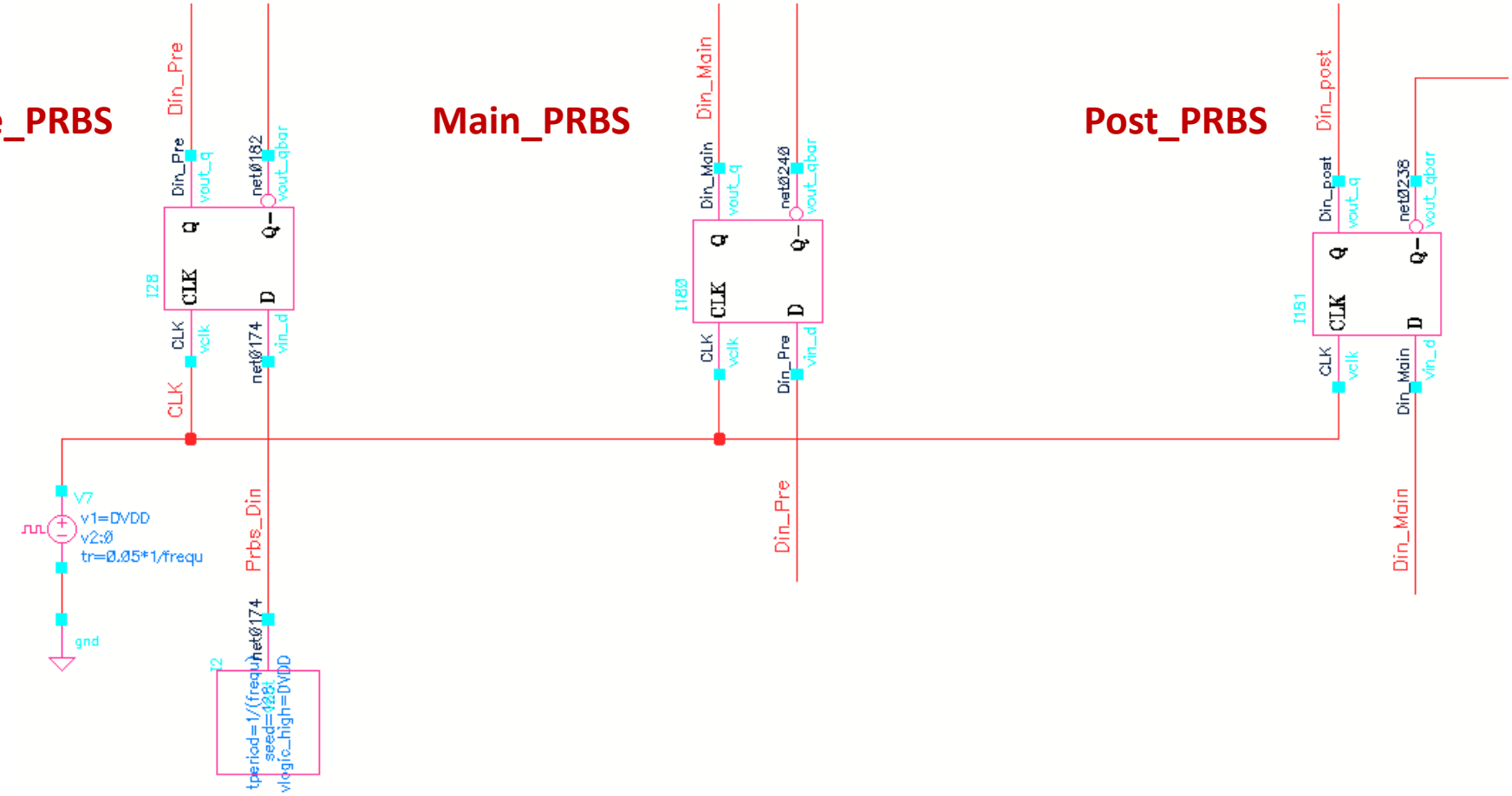
HW 6 - Problem 1 Clarifications

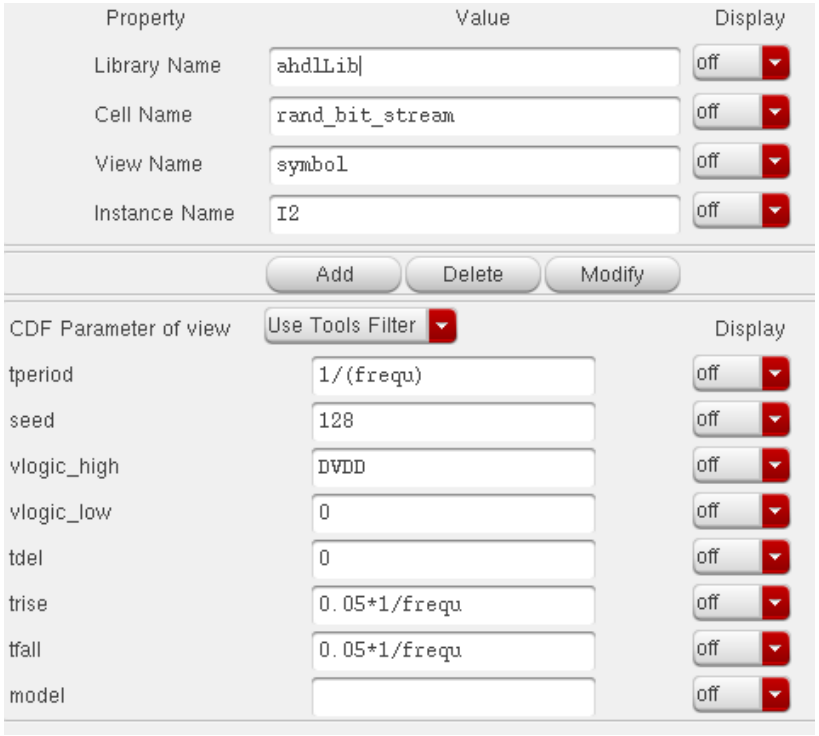
1. PRBS Generation For TX FIR Equalization

Full Data Rate – CLK 10GHz and Data 10Gbps

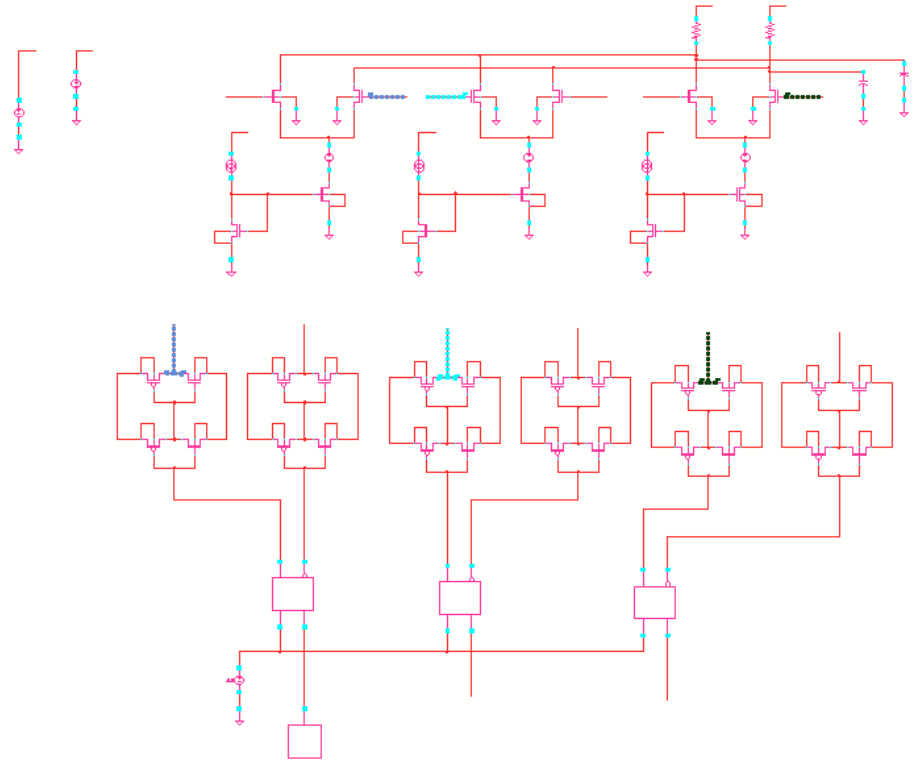


2. Setting for Ideal conponents

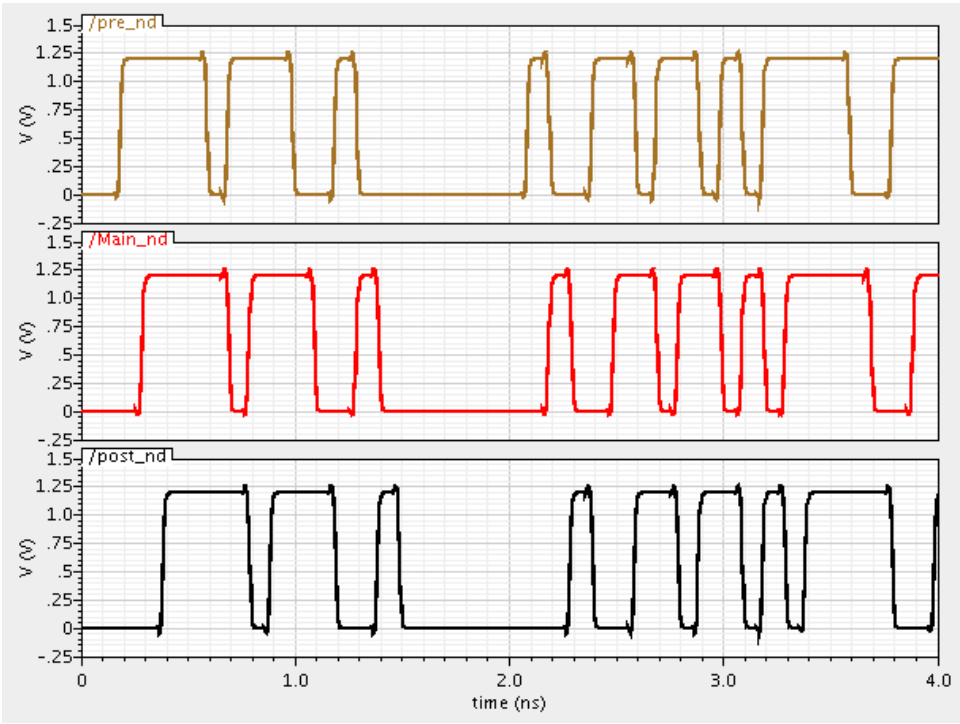
We can find the rand_bit_stream and d_ff in ahdlLib to generate PRBS and 1UI delay PRBS. For setting, Tperiod is your 1UI time, and more detail we can see figures.



3. EX) 3-Tap TX FIR Equalization



Input Data – Pre_nd, Main_nd and Post_nd (1UI Delay)



TX FIR output EYE – (-0.1, 0.8, -0.1) – This setting has to be changed based on your channel pulse response