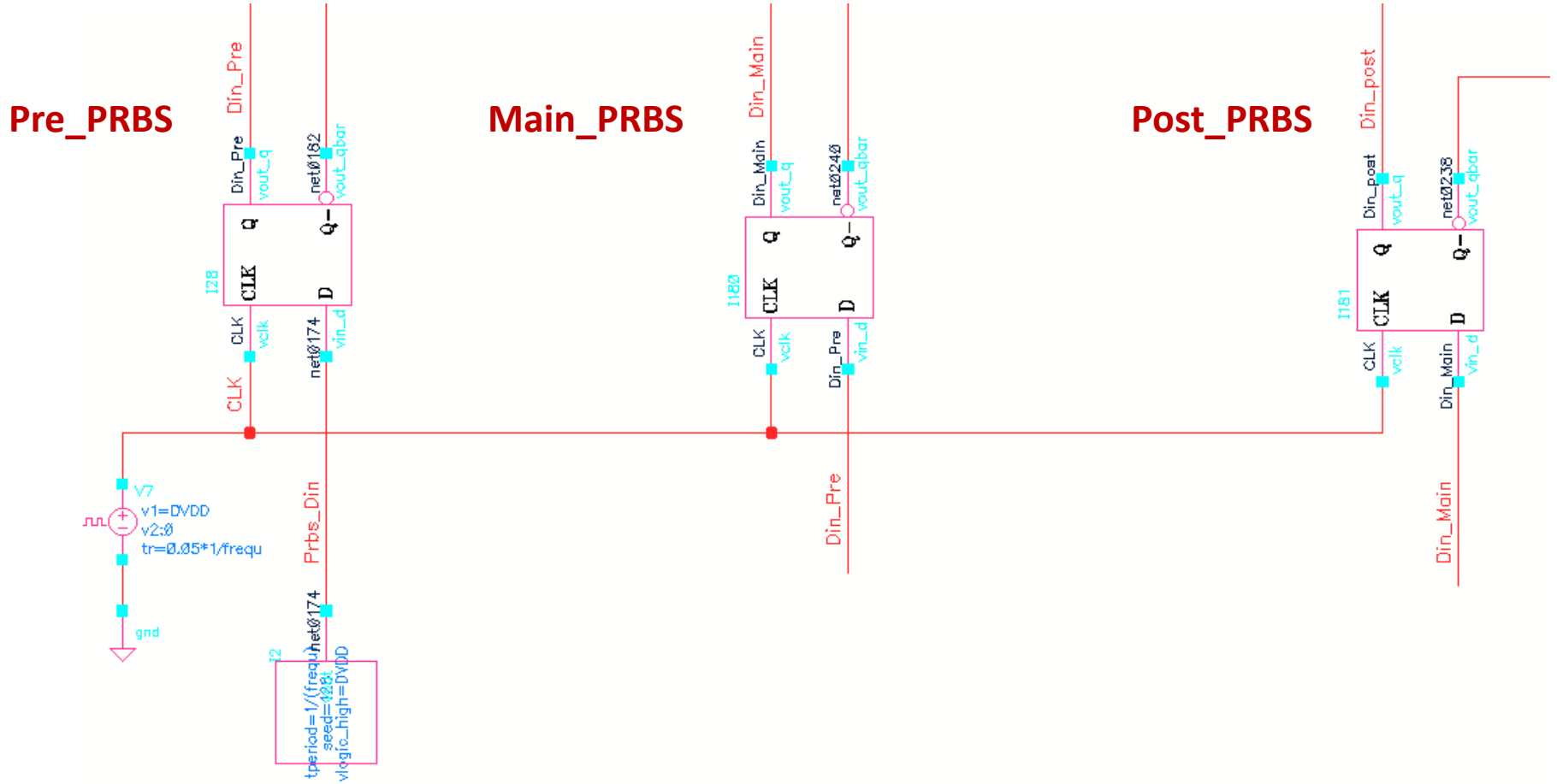


HW 6 - Problem 1 Clarifications

1. PRBS Generation For TX FIR Equalization

Full Data Rate – CLK 10GHz and Data 10Gbps



2. Setting for Ideal components

We can find the rand_bit_stream and d_ff in ahdlLib to generate PRBS and 1UI delay PRBS. For setting, Tperiod is your 1UI time, and more detail we can see figures.

Property	Value	Display
Library Name	ahdlLib	off
Cell Name	d_ff	off
View Name	symbol	off
Instance Name	I28	off

Add Delete Modify

CDF Parameter of view Use Tools Filter

Property	Value	Display
model		off
vlogic_high	DVDD	off
vlogic_low	0	off
vtrans_clk	DVDD/2	off
vtrans	DVDD/2	off
tde1	de1	off
trise	$0.05 * 1 / \text{frequ}$	off
tfall	$0.05 * 1 / \text{frequ}$	off

Property	Value	Display
Library Name	ahdlLib	off
Cell Name	rand_bit_stream	off
View Name	symbol	off
Instance Name	I2	off

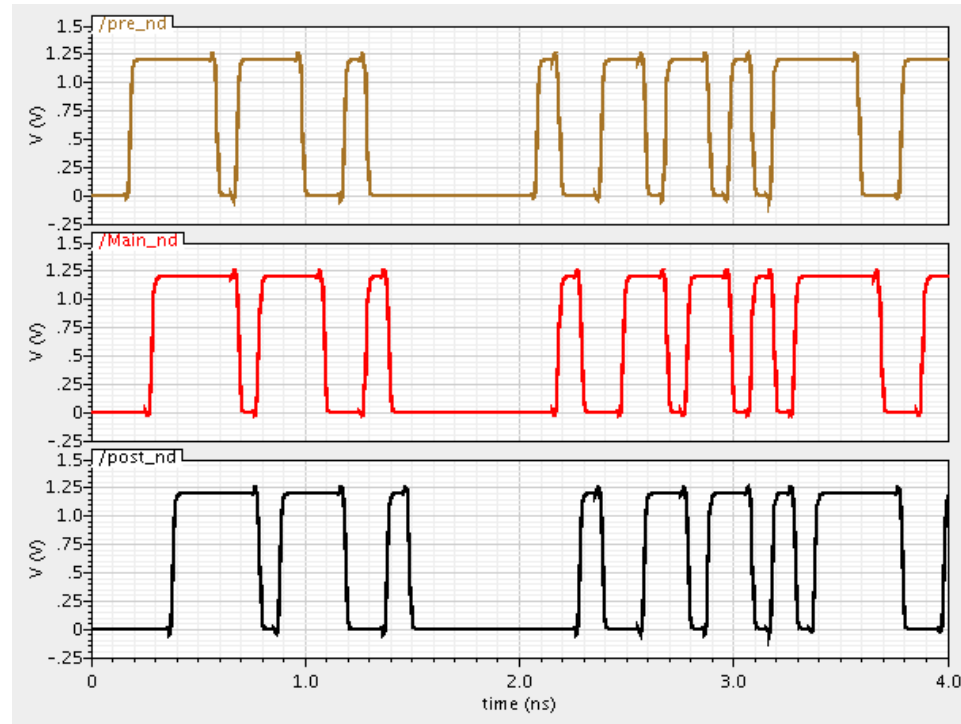
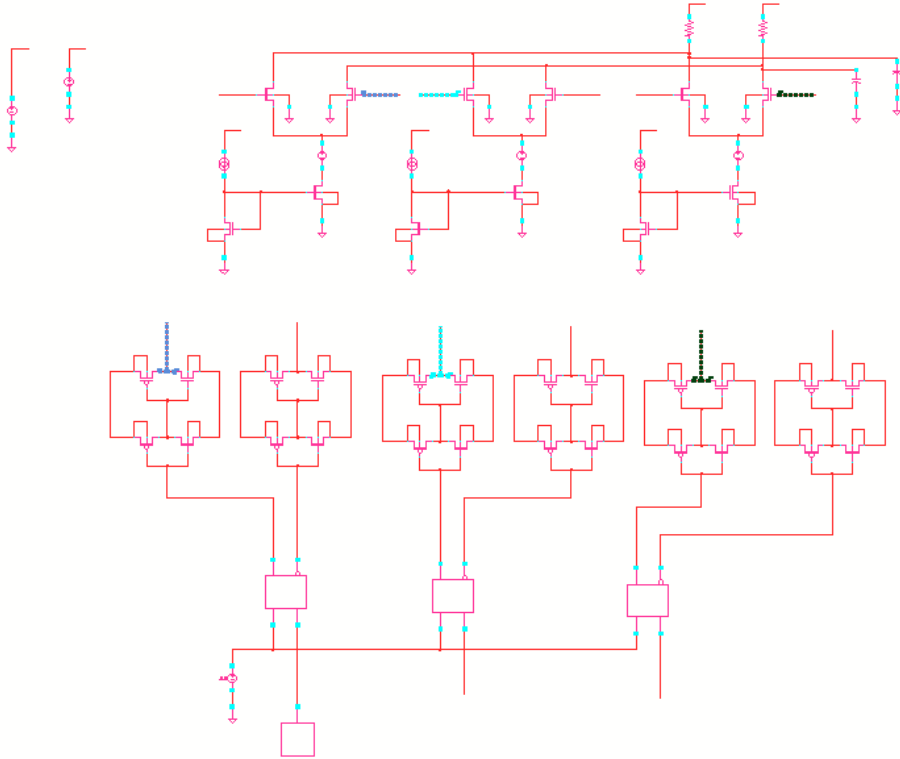
Add Delete Modify

CDF Parameter of view Use Tools Filter

Property	Value	Display
tperiod	$1 / \text{frequ}$	off
seed	128	off
vlogic_high	DVDD	off
vlogic_low	0	off
tde1	0	off
trise	$0.05 * 1 / \text{frequ}$	off
tfall	$0.05 * 1 / \text{frequ}$	off
model		off

3. EX) 3-Tap TX FIR Equalization

Input Data – Pre_nd, Main_nd and Post_nd (1UI Delay)



TX FIR output EYE – (-0.1, 0.8, -0.1) – This setting has to be changed based on your channel pulse response

