4 bit Parallel PRBS Generation





Data 1[n-1] = D5 [n] Data2 [n-1] = XNOR (Data1[n], Data3[n]) Data3 [n-1] = XOR (Data2[n],Data4[n]) Data4 [n-1] = XOR (Data3[n], Data[5]) D5 [n-1] = XOR (Data4[n], XNOR (Data1[n+1], Data3[n+1])) D5 internally used for 4 bit Parallel PRBS generation.

- 1. To generate 2.5Gbps data, 2.5GHz Clock has to be connect to the clock of DFF
- 2. Ideal Logic components (DFF, XNOR, and XOR gate) have in ahdlLib, which we are getting for random generation component

Edit Object Properties					
Apply To Only cur	rent 🔍 instance 🔽				
Show 🔄 system 🗹 user 🗹 CDF			Browse Reset Instance Labels Display		
Browse	Reset Instance Labels Display		Property	Value	Display
Property	Value	Display	Library Name	ahdlLib	off 🔽
Library Name	ahdlLib	off 🔽	Coll Nome	fore and the	off
Cell Name	d_ff	off 🔽	Cell Name	xnor_gate	
View Name	symbol	off 🔽	View Name	symbol	off 🔽
Instance Name	I15	off 🔽	Instance Name	I42q	off 🔽

4 bit Parallel PRBS Detection



*2.5GHz Clock has to be connect DFF

Simulation Result

