- Parallel PRBS generation and detection circuit could be used in the project to detect the data transmission integrity in order to monitor the functionality of the designed transceiver.

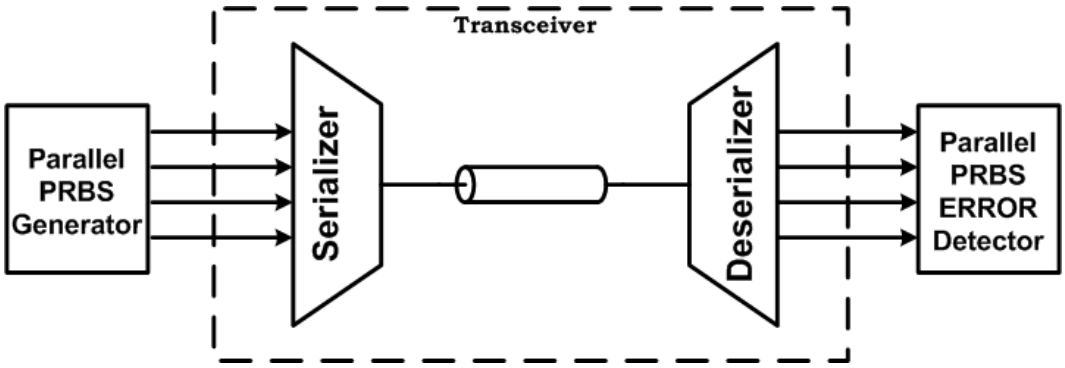


Figure 1 Schematic of parallel PRBS generator and error detector using in Serdes

- The schematic of $2^7$-1 4 bit parallel PRBS generator is shown in Figure 2. AHDL logic models are used to build this circuit.

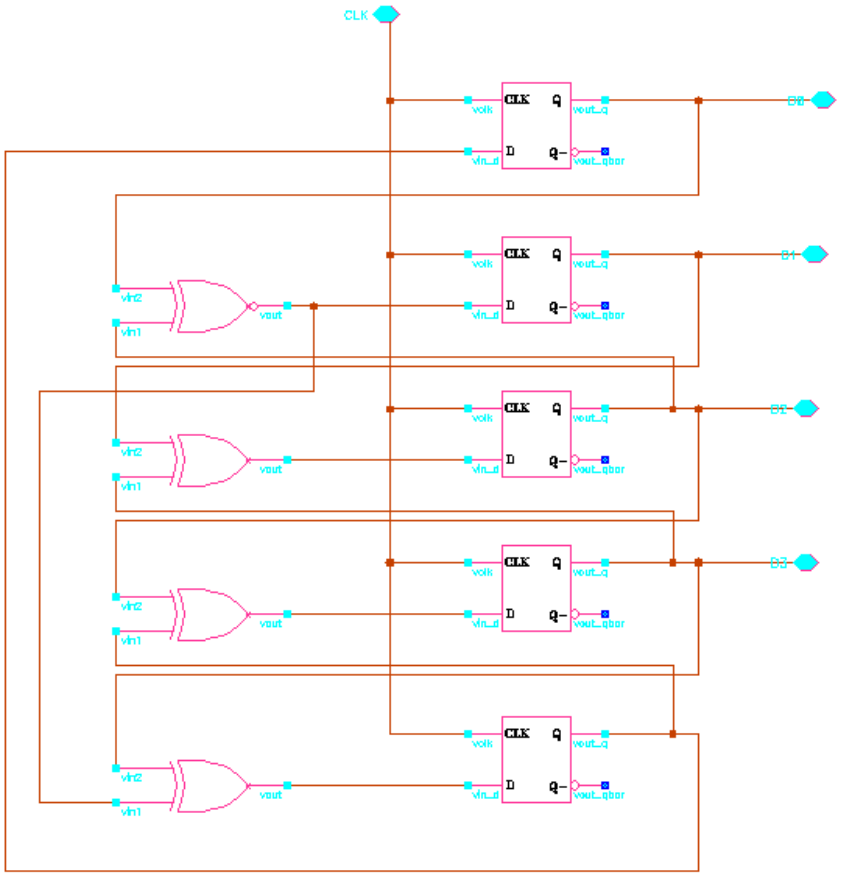


Figure 2 schematic of $2^7$-1 4 bit parallel PRBS circuit

- The schematic of $2^7$-1 4 bit parallel PRBS detector is shown in Figure 3. AHDL logic models are used to build this circuit.

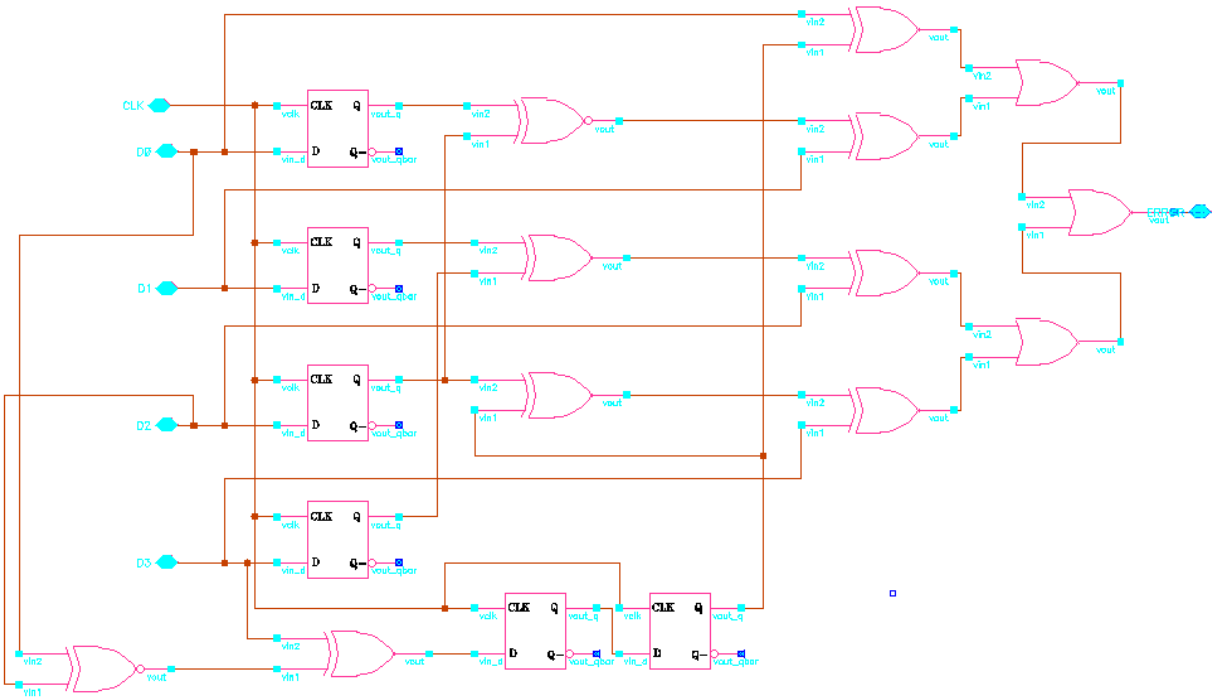


Figure 3 The schematic of $2^7$-1 4 bit parallel PRBS detector

- The schematic of a parallel PRBS testing circuit at 5Gb/s is shown in Figure 4. With perfect signal transmitting channel, the error output shows ZERO voltage as shown in Figure 5.

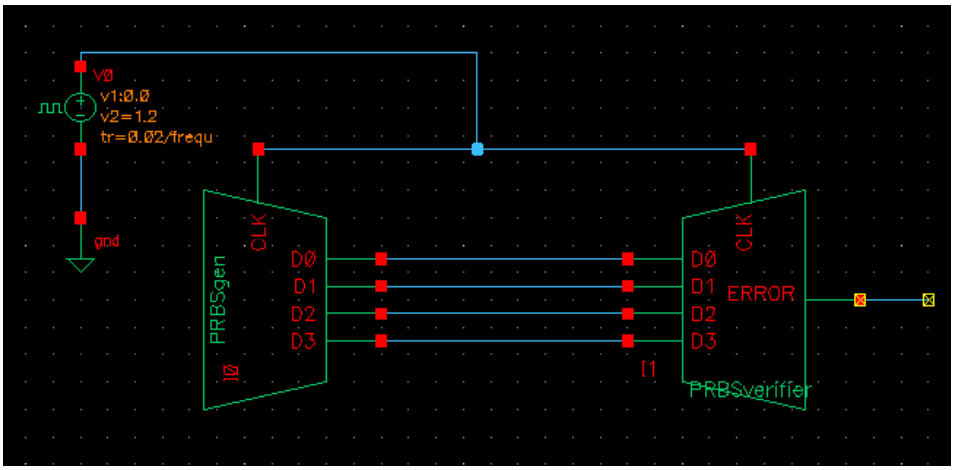


Figure 4 Schematic of a parallel PRBS testing circuit

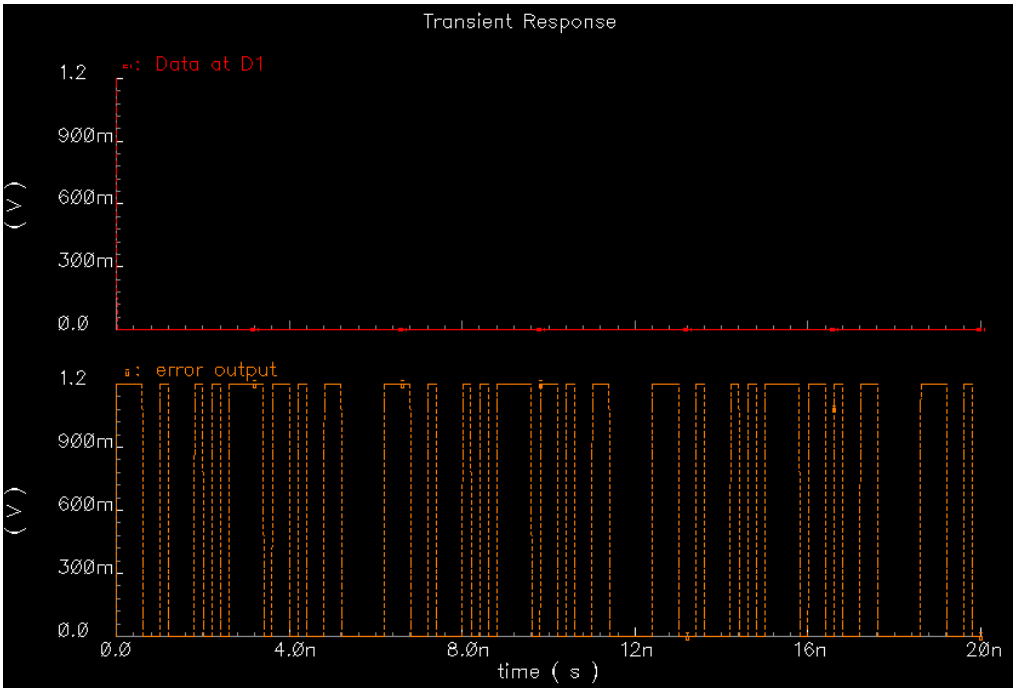


Figure 5 Simulation results of uncorrupted data and error free output

- The schematic of a parallel PRBS testing circuit at 5Gb/s is shown in  with corrupted data at D1. With corrupted signal transmitting “channel”, the error output shows NON-ZERO voltage.

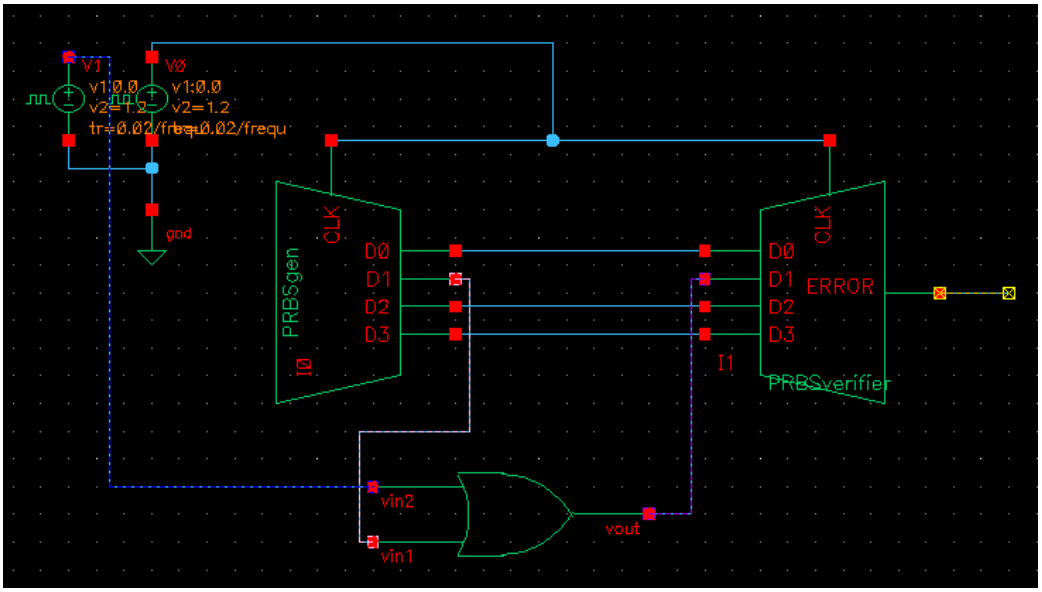


**Figure 6 Schematic of a parallel PRBS testing circuit with corrupted data channel**

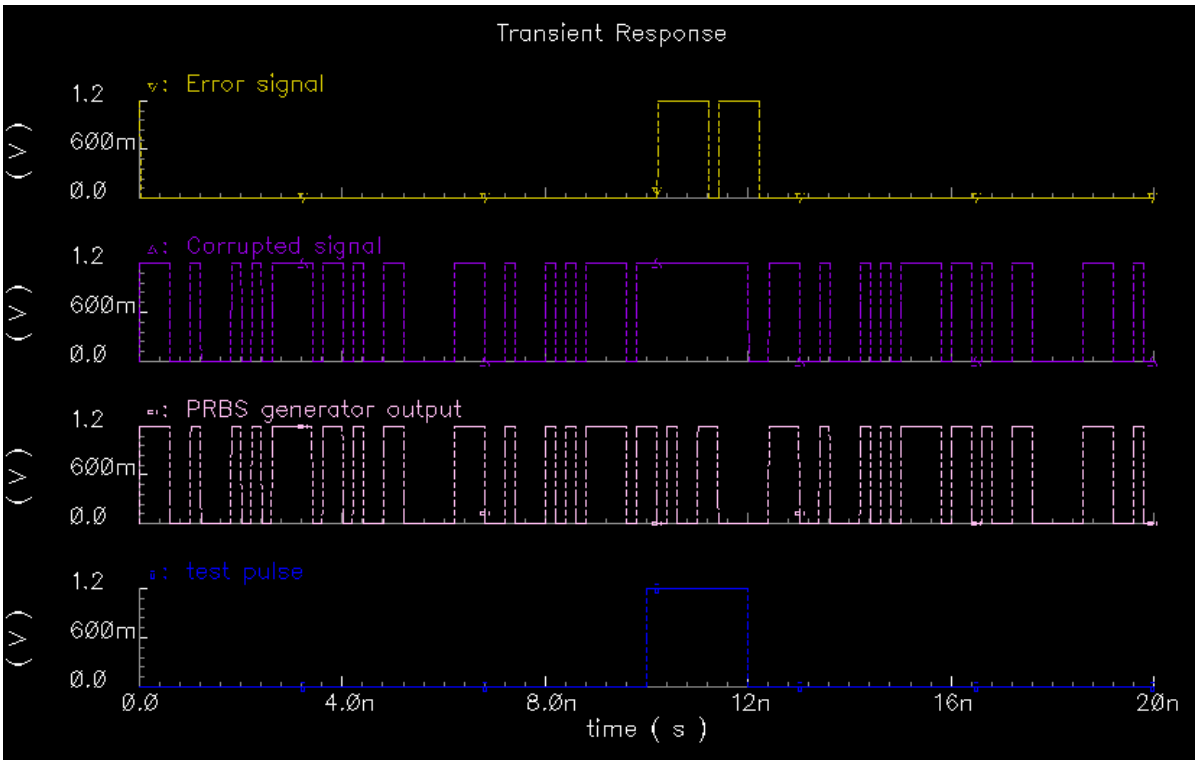


**Figure 7 Simulated corrupted data channel using PRBS generator and detector**

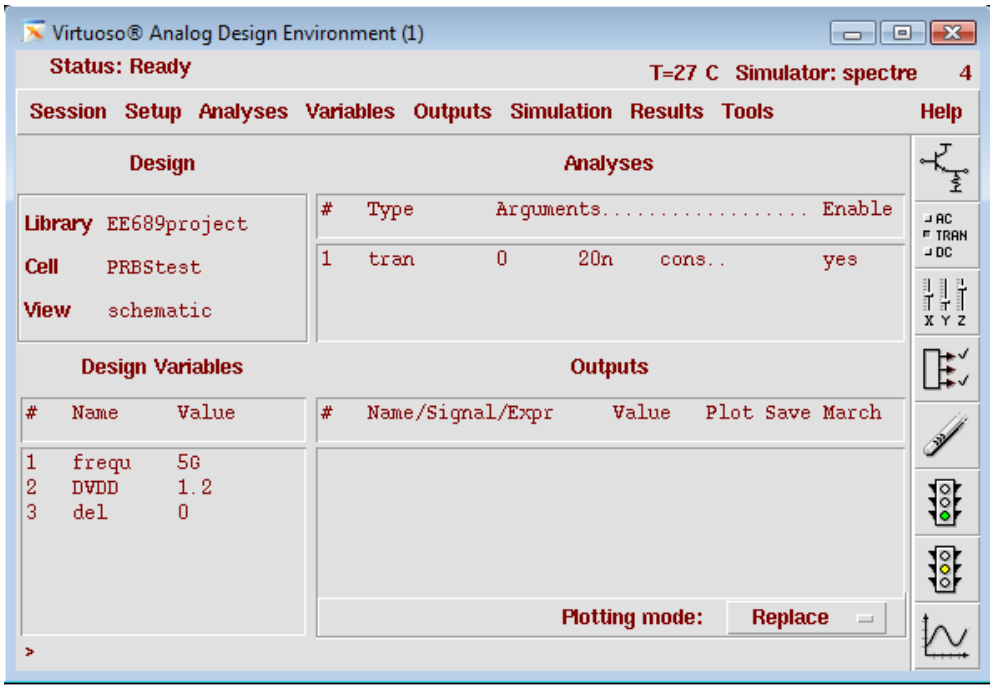


**Figure 8 Analog Design Environment setup**