A Comparator With Reduced Delay Time in 65-nm CMOS for Supply Voltages Down to 0.65 V

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***Abstract*—A comparator in a low-power 65-nm complementary metal–oxide–semiconductor process (only standard transistors with threshold voltage $V_t \approx 0.4$ V were used) is presented, where the circuit of a conventional latch-type comparator consisting of two cross-coupled inverters is modified for fast operation, even with 0.6 GHz at a low supply voltage of 0.65 V. The advantages of a high-impedance input, rail-to-rail output swing, robustness against the influence of mismatch, and no static power consumption are kept. To achieve a bit error rate of 10^{-9} at 1.2-V supply, an amplitude at the input of 16.5 mV at 4 GHz has to be applied. If the supply voltage is lowered, 12.1 mV at 0.6 GHz/0.65 V is necessary. The power consumption of the comparator is 2.88 mW at 5 GHz (1.2 V) and 128 μW at 0.6 GHz (0.65 V). Simulations show an offset standard deviation of about 6.1 mV at 0.65-V supply. With an on-chip measurement circuit, the delay time of the comparator of, e.g., 104 ps for 15-mV input amplitude at 1.2-V supply, is obtained.**

***Index Terms*—Comparator, complementary metal–oxide–semiconductor (CMOS) analog circuits, low supply voltage, modified latch, ultradeep submicrometer (UDSM) CMOS.**

I. Introduction

ANALOG circuit design in ultradeep submicrometer (UDSM) CMOS technologies suffers from low supply voltages, thus having a small voltage headroom left, which commonly decreases the dc performance at a given power consumption [1]. In contrast to this, the ac performance tends to become better in UDSM CMOS technologies due to lower parasitic capacitances. Another problem is the increasing gate tunnel current when the gate area is increased (supposing optimal g_m/I_D ratio) to, e.g., reduce the input-referred offset. Lowering the influence of mismatch by increasing the gate area is limited by the gate–leakage mismatch. It is now a challenge to develop new circuit structures that either avoid a stack of too many transistors between the supply rails, so that the technology-given better ac performance does not degrade, or keep the advantages of standard circuits, e.g., robustness against the influence of noise and mismatch, or lower power consumption. An important circuit that is used for the transition from the analog to the digital domain is the comparator. Commonly, a comparator compares two analog input voltages and delivers a logical value at the output, which indicates the polarity of the input-voltage difference. Especially clocked regenerative comparators are fundamental circuit blocks, which are mostly based on cross-coupled inverters (latch) to force a fast decision due to positive feedback [2]. This type of comparator is typically used in Flash analog-digital converters (ADCs) because of their high decision speed. In ADCs, additional circuitry is added to the comparator, e.g., a preamplifier for enhancing the resolution [3]–[5] or an offset compensation block [6]. The applications of comparators are not only restricted to Flash ADCs. A comparator based on a current-mode latch was implemented in a 40-GBit/s demultiplexer in 1.2-V/0.11-μm CMOS technology. There, a 10-GHz clocked three-stage comparator with a bandwidth modulation technique was used to extract every fourth bit of a 40-GBit/s data stream [7]. In [8], a comparator was designed for an analog rank-order extractor, and in [9], a latch-type voltage sense amplifier for a static random-access memory is described.

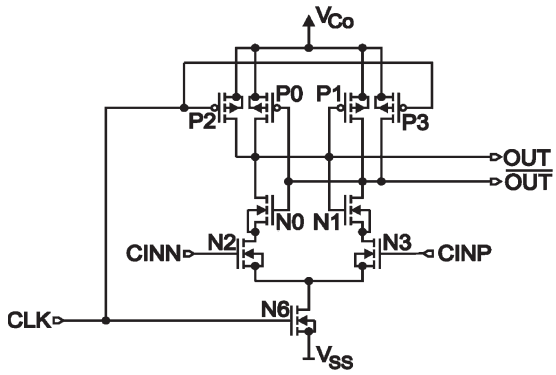

Fig. 1. Widely used conventional latch-type comparator.

A standard comparator circuit, which is widely used in circuit design, with high-impedance input, rail-to-rail output swing, and no static power consumption is shown in Fig. 1 [6], [9], [10]. Before the comparison, the comparator is reset in the reset phase (CLK $= V_{SS}$, and N6 is off), where transistors P2 and P3 pull both output nodes OUT and $\overline{\text{OUT}}$ to V_{Co} to define a start condition and to have a valid logical level during reset. The input voltages to be compared are applied to nodes CINP and CINN. In the comparison phase (CLK $= V_{\text{Co}}$, transistors P2 and P3 are off, and N6 is on), for the case where CINP $>$ CINN, the whole latch [cross-coupled inverters (N0, P0) and (N1, P1)] will initiate regeneration when $\overline{\text{OUT}}$ has been discharged to $V_{\text{Co}} - V_{\text{tp}}$ by N3 before OUT (discharged by N2) reaches this voltage level and P0 has turned on before P1. At this point of time, OUT $-$ $\overline{\text{OUT}}$ is the amplified input voltage difference

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CINP-CINN, which is initially applied to the latch for regeneration [6]. OUT is pulled to $V_{\rm Co}$, and $\overline{\rm OUT}$ is pulled to V_{SS}. In the other case where CINP $<$ CINN, the circuit works vice versa: P1 is turned on before P0, and the latch pulls OUT to V_{SS} and $\overline{\rm OUT}$ to $V_{\rm Co}$. In principle, this circuit has the advantage of good robustness against noise and mismatch, because, among other reasons, it can also be designed with large input transistors N2 and N3, e.g., to minimize the offset, where the larger parasitic capacitances at their drains do not directly affect the switching speed, which primarily depends on the load capacitances at output nodes OUT and $\overline{\rm OUT}$. For example, when the latch regenerates OUT toward $V_{\rm Co}$, then transistor N0 is turned off, and node OUT is cut off from the parasitic capacitance at the drain of N2. Thus, the effective load capacitance of the latch is reduced in comparison to that of N2 and N3 directly connected to the output nodes. Another reason for the lower input-referred offset is the amplification of CINP-CINN for the initial voltage difference, which causes the latch to switch higher than in other structures (e.g., in [14]), where the input transistors and the latch are parallel (additional parallel load at the output nodes). Disadvantageous is the fact that, due to the many stacked transistors, a sufficient high supply voltage is needed for a proper delay time [11]. This may cause problems in low-voltage UDSM CMOS, where even a stand-alone latch (e.g., used in [11]), with its two cross-coupled inverters, suffers from higher delay time if the supply voltage is reduced or a low-power process with higher transistor threshold voltages is used. For example, in Fig. 1, after the reset phase, the initial condition of the comparison phase is OUT $= \overline{\rm OUT} = V_{\rm Co}$. Thus, at the beginning of the decision, only transistors N0 and N1 of the latch contribute somewhat to positive feedback until the voltage level of one output node has dropped enough to turn on transistor P0 or P1 to start complete regeneration. At a low supply voltage, this voltage drop only contributes a small gate–source voltage for transistors N0 and N1, where the gate–source voltage of P0 and P1 is also small; thus, the delay time of the latch becomes large due to lower transconductances.

This brief describes a proposed comparator design, where the latch of the conventional circuit in Fig. 1 has been replaced by a new latch for low-supply-voltage operation, where the advantages of a high-impedance input, a rail-to-rail output swing, no static power consumption, and the indirect influence of the parasitic capacitances of the input transistors (larger gate area for lower offset) to the output nodes and, therefore, to the switching speed have been kept. Furthermore, a structure with parallel-connected input transistors as in [14] is avoided to get a higher amplification of CINP-CINN for the initial voltage difference, which causes the latch to flip with a lower input-referred offset.

II. Circuit Description

The circuit of the proposed comparator is shown in Fig. 2. In contrast to the conventional latch used in Fig. 1, where only N0 and N1 are initially on, the latch of the proposed comparator is expanded into two paths between the supply rails (transistors N0, N1, P0, P1, P4, and P5), so that, at the beginning of the comparison phase, where both output nodes have the initial

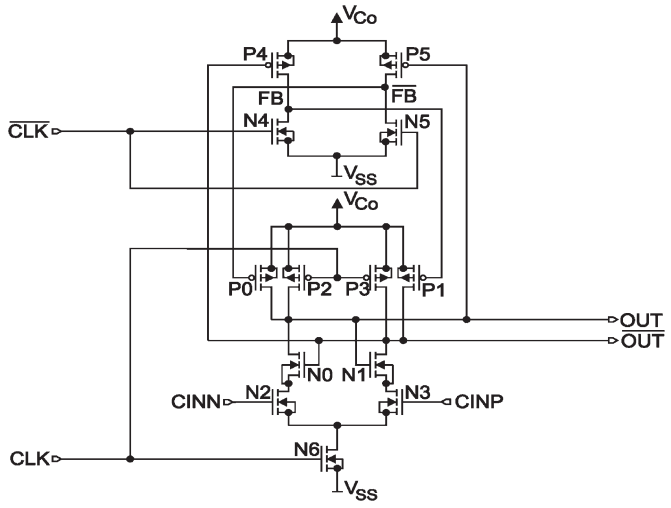

Fig. 2. Proposed comparator with a modified latch.

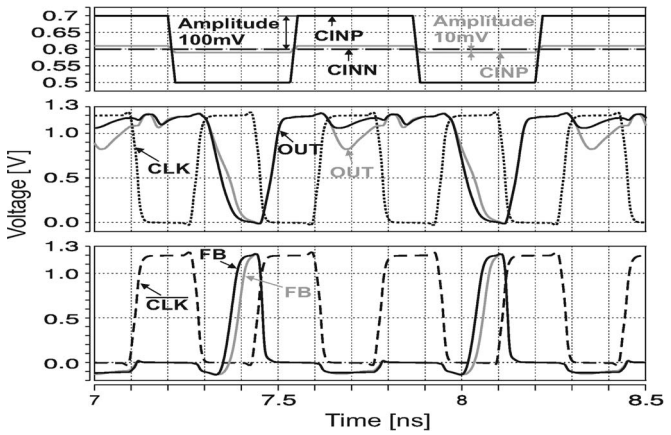

Fig. 3. Transient simulations of the proposed comparator with an input voltage difference of (gray case) 10 mV and (black case) 100 mV.

condition OUT $= \overline{\rm OUT} = V_{\rm Co}$ (initially, internal nodes FB $= \overline{\rm FB} = V_{SS}$), transistors N0 and N1 are turned on. However, transistors P0 and P1 are also turned on and build, with input transistors N2 and N3, an amplifier with a distinct working point, which, in contrast to that in Fig. 1, contributes enough gate–source voltage to transistors N0 and N1 at lower supply voltages. Complete positive feedback of the latch starts when one output node is discharged enough to turn on P4 or P5. Regeneration is done with N0, N1, P0, and P1, where P4 and P5 help with additional amplification. To get a rail-to-rail output swing and no static power consumption of the comparator, one of the initial load transistors P0 or P1 is switched off, when, during regeneration, $\overline{\rm FB}$ or FB, respectively, is charged to $V_{\rm Co}$. The other advantages of a high-impedance input and no direct influence of parasitic capacitances of N2 and N3 to the output nodes are kept. The corresponding transient simulations of Fig. 2 can be seen in Fig. 3. A clock period is divided into two phases: The reset phase (CLK $= V_{SS}$) is used to establish the initial condition OUT $= \overline{\rm OUT} = V_{\rm Co}$ for the following comparison phase. (CLK $= V_{\rm Co}$, $V_{\rm Co}$ is the positive supply voltage of the comparator.) During reset, transistor N6 is switched off, and transistors P2, P3, N4, and N5 are on. Consequently, the

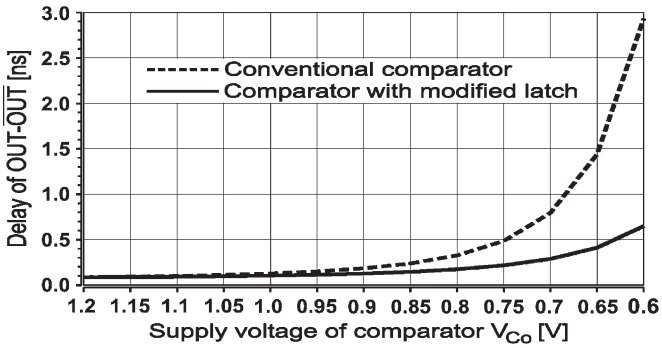

Fig. 4. Comparison of the decision time (50% clock edge to 50% of the final output voltage difference OUT $-$ $\overline{\text{OUT}} = V_{\text{Co}}$) of the conventional comparator with the proposed comparator, depending on the supply voltage V_{Co}.

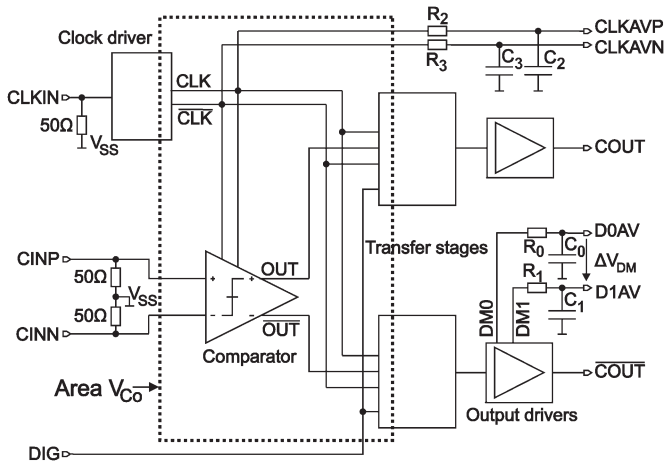

Fig. 5. Block diagram of the test chip with the comparator.

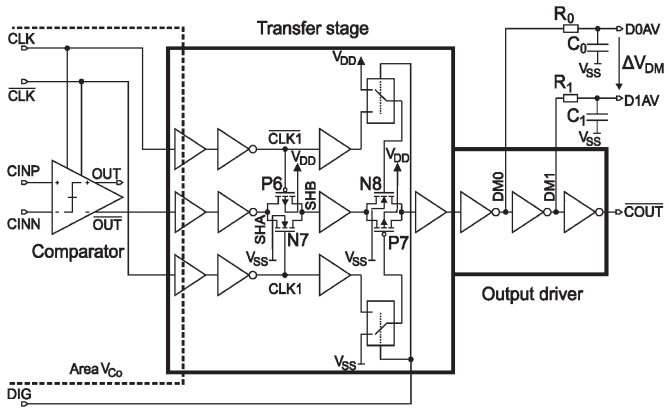

Fig. 6. Detailed block diagram of on-chip delay-time measurement implementation, which consists of the transfer stage at node $\overline{\text{OUT}}$ and the appropriate output driver with low-pass filters (R_0, C_0) and (R_1, C_1).

output nodes OUT and $\overline{\text{OUT}}$ are pulled toward V_{Co} by P2 and P3, which causes transistors P4 and P5 to be switched off. N4 and N5 pull both nodes FB and $\overline{\text{FB}}$ to V_{SS}. Hence, transistors P0 and P1 are turned on and help in pulling OUT and $\overline{\text{OUT}}$ to the final voltage level V_{Co}. Comparison of the voltage at input CINP with the voltage at CINN is started when CLK switches to voltage level V_{Co} (comparison phase). Hence, transistor N6 is turned on, and P2, P3, N4, and N5 are switched off. At the very beginning, transistors P4 and P5 are switched off, and transistors P0 and P1 work in the linear region and build the load for an amplifier with N2 and N3. Transistors N0 and N1 are initially on. (The comparison phase starts with OUT $= \overline{\text{OUT}} = V_{\text{Co}}$ and FB $= \overline{\text{FB}} = V_{SS}$.) If, for the input voltage, CINP $>$ CINN is assumed, transistor N3 pulls the voltage level at node $\overline{\text{OUT}}$ down faster than N2 does at node OUT. Hence, transistor P4 begins to conduct. In this initial time period, a small amount of positive feedback is also contributed by transistors N0 and N1. When P4 begins to conduct, node FB is charged toward V_{Co} (N4 and N5 are off), and complete positive feedback is started. Transistor P1 is turned off, and P0 keeps conducting, because node OUT is pulled to V_{Co}. Thus, P5 remains off, and $\overline{\text{FB}}$ remains near V_{SS}. (Sufficient input voltage difference CINP-CINN is assumed.) Finally, N1, P4, and P0 are switched on, and N0, P1, and P5 are turned off. Thus, OUT is at voltage level V_{Co}, $\overline{\text{OUT}}$ is at V_{SS}, and no static current can flow after the decision. In the other case where CINP $>$ CINN, OUT is pulled to V_{SS}, and $\overline{\text{OUT}}$ is pulled to V_{Co}, respectively.

A comparison of the decision times at different supply voltages of the proposed comparator in Fig. 2 with those of the conventional comparator in Fig. 1 is shown in Fig. 4. Each comparator was designed in a similar way, so that the decision time (50% clock edge to 50% of the final output voltage difference OUT $-$ $\overline{\text{OUT}} = V_{\text{Co}}$) is equal for $V_{\text{Co}} = 1.2$ V with the same transistors N0, N1, N2, N3, and N6. For example, at a supply voltage of $V_{\text{Co}} = 0.6$ V, the proposed comparator needs only 650 ps, instead of 2.95 ns, of the conventional comparator and is therefore capable of low-voltage operation. For test purposes, a test chip with the proposed comparator in 65-nm low-power CMOS technology with a nominal supply voltage of $V_{DD} = 1.2$ V was designed, whose block diagram is shown in Fig. 5. The dashed rectangle marks an area that is separately supplied with a voltage V_{Co} to be able to investigate the behavior of the comparator if V_{Co} is lowered. The area outside is supplied with nominal $V_{DD} = 1.2$ V to always have the functionality of the additional measurement circuitry for the characterization of the implemented comparator. With the help of the clock driver, a noninverted digital clock CLK and the appropriate inverted clock $\overline{CLK}$ are generated, where the logical voltage levels are V_{SS} and V_{Co}. To generate a clock signal, a sine wave in which the frequency is defined by the on-chip clock frequency and the duty cycle (adjusted to $\approx 50\%$) is defined by the dc bias voltage level is applied to pad CLKIN. The *RC* low-pass filters (R2, C2) and (R3, C3) are added to measure the mean voltage (duty cycle) of the internal clock lines CLK and $\overline{CLK}$ at pads CLKAVP and CLKAVN, respectively. All high-frequency inputs CLKIN, CINP, and CINN are terminated with on-chip 50-Ω resistors. The transfer stage (see Figs. 5 and 6) dynamically holds the decision of the comparator during its reset phase at node SHB. In the case where CLK1 and $\overline{\text{CLK1}}$ are also switched to transmission gates P7 and N8, respectively (case DIG $= 1.2$ V), P7 and N8 are turned off when P6 and N7 are on, and vice versa during a clock cycle. Therefore, at outputs COUT and $\overline{COUT}$, a single decision of the comparator lasts for a whole clock period, and the overall delay time between (CLK, $\overline{CLK}$) and (COUT, $\overline{COUT}$) is kept constant to simplify bit

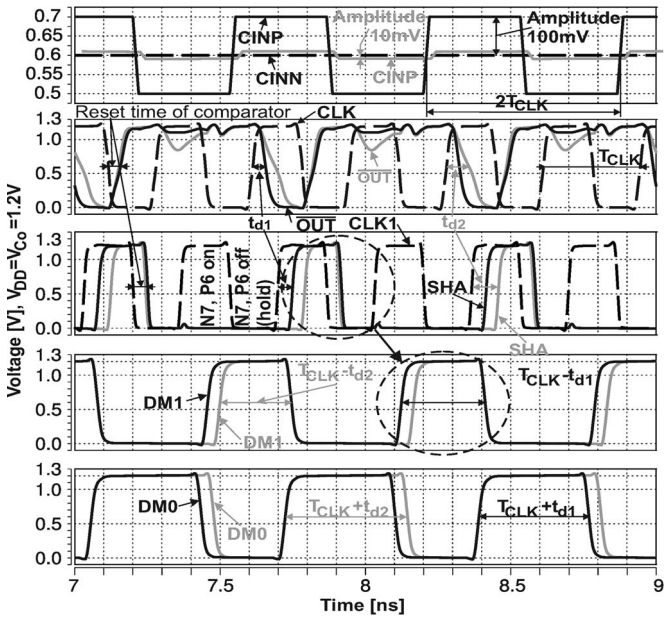

Fig. 7. Transient simulation to illustrate the measurement of the delay time of the comparator (see also Fig. 6, case DIG $= V_{SS}$, where P7 and N8 are always turned on). An amplitude at the input CINP of 100 mV (black case) causes a delay time t_{d1}, and a smaller amplitude of 10 mV (gray case) causes a larger delay time t_{d2}. The delay time is then determined by measuring the mean voltage of nodes DM0 and DM1 at D0AV and D1AV, respectively. $\Delta V_{\mathrm{DM}} =$ D0AV $-$ D1AV is proportional to t_d.

error rate (BER) measurements with a BER analyzer, because the delay time of the comparator varies, depending on, e.g., the amplitude or the common-mode voltage at the inputs. In the transfer stage (see also Fig. 6), adapters for the conversion of the logical voltage levels V_{SS} and V_{Co} to levels V_{SS} and V_{DD} are added at the input. Such an adapter consists of a chain of two inverters, where each inverter is separately supplied for step-wise increasing the supply voltage from V_{Co} to $V_{DD} = 1.2$ V. Each output driver of Fig. 5 consists of a chain of inverters and is able to drive off-chip 50-Ω measurement equipment. *RC* low-pass filters (R0, C0) and (R1, C1) have been added at the output driver for $\overline{COUT}$, with which, in addition to the transfer stage, the delay time t_d of the comparator at $\overline{\mathrm{OUT}}$ can be measured (see Fig. 6). Delay time measurements can be done in the case where DIG $= V_{SS}$ when only transmission gate (P6, N7) holds the decision of the comparator during reset and transmission gate (P7, N8) is switched to be always turned on. The delay time is defined here as the time duration, which begins at the time point when the voltage level has reached 50% of V_{Co} at the rising edge of CLK and ends at the time point when $\overline{\mathrm{OUT}}$ has fallen to the switching threshold of the following inverter ($\approx 50\%$ of V_{Co}). The transient simulations for Fig. 6 to illustrate delay-time measurements are shown in Fig. 7. For measuring the delay time, a rectangular signal with a period of two times the clock period, which is superimposed by a bias voltage for offset compensation, is applied to CINP, as shown in Fig. 7. CINN is biased with a reference voltage, e.g., an amplitude at the input CINP of 100 mV (black case) causes a delay time t_{d1}, and a smaller amplitude of 10 mV (gray case) causes a larger delay time t_{d2} at $\overline{\mathrm{OUT}}$. Signal $\overline{\mathrm{OUT}}$ is led to a chain of inverters, which are able to drive the parasitic capacitances of

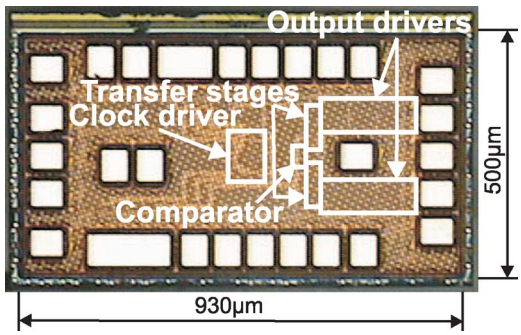

Fig. 8. Micrograph of the test chip with the comparator.

transmission gate (P6, N7). To compensate the additional delay time, which is caused by the inverter chain, signal CLK and $\overline{\mathrm{CLK}}$ are each led via an equal inverter chain as well. Thus, the time difference between turning on (P6, N7) by CLK1 and the rising edge at node SHA is the delay time t_d of the comparator. The reset time of the comparator is not considered due to the fact that it is replaced by $T_{\mathrm{CLK}}/2$ because transmission gate (P6, N7) holds the decision of the comparator at node SHB during reset $T_{\mathrm{CLK}}/2$ long. Transistors P7 and N8 are always on. Thus, the duty cycle at nodes DM0 and DM1 in the output driver comprises information on the comparator's delay time. To obtain this delay time t_d, the mean voltages of DM0 and DM1 are measured at D0AV and D1AV, and then, the following is used:

$$t_d = \frac{\mathrm{D0AV} - \mathrm{D1AV}}{V_{DD}} T_{\mathrm{CLK}} = \frac{\Delta V_{\mathrm{DM}}}{V_{DD}} T_{\mathrm{CLK}}. \qquad (1)$$

A Monte Carlo simulation with 50 runs for the delay-time measurement system consisting of the transfer stage and output driver, as shown in Fig. 6, has been done, where, instead of the output signal of the comparator, a signal with a known delay time has been introduced to the transfer stage. As a result, an offset error of 6 ps and a standard deviation of $\sigma < 4$ ps of the simulated delay time measurement result were obtained. It should be mentioned that the measurement technique is independent of the duty cycle of the signal CLK.

An analytical calculation of the delay time of the comparator itself can be done in a similar way as in [9]: The threshold voltage of P4 $(=$ P5$)$, for the first part (discharging time of the output nodes), and the additional contribution of the transconductances of (P4, P5) and the parasitic capacitances of the internal nodes FB and $\overline{\mathrm{FB}}$ to positive feedback, for the second part (regeneration time of the latch), have to be considered.

III. Measurement Results

A chip with an area of 930×500 μm^2 was fabricated in low-power 65-nm CMOS technology (see Fig. 8). Thereof 28.4×49.1 μm^2 is dedicated to the comparator.

The influence of noise to the decision of the comparator and, thus, the sensitivity can be characterized with the help of statistical measurements by measuring the BER with an appropriate pattern generator and receiver. A reference voltage (at CINN) and a pseudorandom bit sequence $2^{31} - 1$ (at CINP) were applied, which was superimposed to a bias voltage of

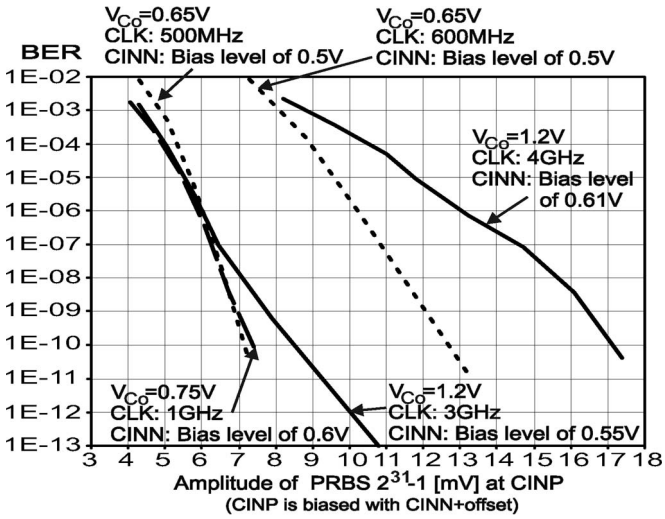

Fig. 9. BER measurements.

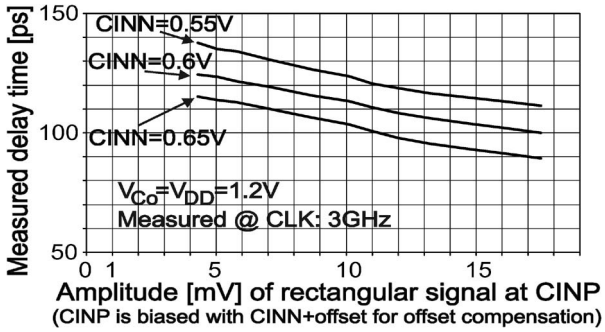

Fig. 10. With the help of the on-chip measurement implementation, determined mean delay time of the comparator (with ten test chip samples measured, $\sigma \approx 7$ ps).

CINN + offset to compensate the offset of the comparator. The amplitude of a bit sequence is defined here, i.e., the bits switch, at CINP $+/-$ amplitude, around voltage level CINN + offset, whereas, at CINN, the reference voltage is applied. The BER measurement results of a typical test chip are shown in Fig. 9. To achieve BER $= 10^{-9}$ at 1.2-V supply, an amplitude of 7.8 mV at 3 GHz, 16.5 mV at 4 GHz, and 145 mV at 5 GHz had to be applied. If $V_{\rm Co}$ was lowered, 7 mV at 1 GHz/0.75 V, 6.9 mV at 0.5 GHz/0.65 V, and 12.1 mV at 0.6 GHz/0.65 V were measured.

The determined mean delay time of the comparator (ten chip samples), which was measured with the on-chip measurement implementation previously described, is shown in Fig. 10. For an amplitude of, e.g., 15 mV, at the input of the comparator, the mean delay times ($\sigma \approx 7$ ps) were 93 ps at CINN $= 0.65$ V, 104 ps at CINN $= 0.6$ V, and 115 ps at CINN $= 0.55$ V at $V_{\rm Co} = 1.2$ V.

The power consumption of the comparator was 2.88 mW at 5 GHz (1.2 V), 295 μW at 1 GHz (0.75 V), and 128 μW at 0.6 GHz (0.65 V). To investigate the influence of mismatch, Monte Carlo simulations were done. For a run of 50 samples, the standard deviations of the offset were simulated to be 1.9 mV at CINN $= 0.6$ V ($V_{\rm Co} = 1.2$ V), 4 mV at CINN $= 0.55$ V ($V_{\rm Co} = 0.75$ V), and 6.1 mV at CINN $= 0.5$ V ($V_{\rm Co} = 0.65$ V).

IV. Conclusion

A comparator with a modified latch for low-supply-voltage operation has been fabricated in low-power 65-nm CMOS (threshold voltage ≈ 0.4 V) and characterized with the help of an on-chip delay-time measurement circuit. Compared to [9], [11]–[13], the proposed comparator has shown a good tradeoff between sensitivity, offset, and speed, with the big advantage of working even at a supply voltage of 0.65 V with a clock rate of 0.6 GHz, power consumption of 128 μW, sensitivity of 12.1 mV, and simulated $\sigma = 6.1$ mV of the offset. On the contrary, in [12], transistors with a threshold voltage of ≈ 0.29 V were used, and the comparator worked with 0.6 GHz at 0.5-V supply voltage with 60.5-mV sensitivity and a simulated standard deviation of the offset $\sigma = 57$ mV but 18-μW power consumption. Compared to [14], the offset $\sigma = 22$ mV is reduced to 1.9 mV at 1.2 V. By placing the input transistors below the modified latch, the delay time is shortened to 650 ps, compared with 900 ps in [14] at 0.6-V supply.

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