ECEN 720 High-Speed Links: Circuits and Systems

Lab4 –Receiver Circuits

Objective

To learn fundamentals of receiver circuits.

Introduction

Receivers are used to recover the data stream transmitted by transmitters. The voltage and time domain resolution and offset are the key performance specs for receiver circuits. In this lab, the receiver building blocks will be studied and practiced. Their performance metrics are going to be characterized.

Receiver Parameters

The receiver performance is measured in both time and voltage domain. How small voltage a receiver can measure is the sensitivity. The receiver voltage offset is a similar concept as a comparator input offset voltage, which is caused by the device mismatch and circuit structure. In time domain, the shortest pulse width the receiver can detect is called the aperture time. It limits the maximum data rate of the link system. The time offset becomes the timing skew and jitter between the receiver and some reference timing marker (CDR). These four parameters are illustrated in Figure 1.

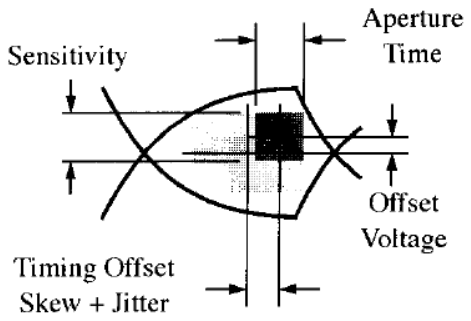


Figure 1 Eye Diagram Showing Time and Voltage Offset and Resolution [Dally]

Basic Receiver Block Diagram

Pre-amplifier is often used in the receiver side to improve signal gain and reduce input referred offset and noise. It must provide gain at high frequency bandwidth so that it does not attenuate high frequency data. It can also operate as a common mode shifter to correct the common mode

mismatch between TX and RX. Offset correction can be also implemented in the pre-amplifier. The comparator/sampler can be implemented with static amplifiers or clocked regenerative amplifiers. If the power consumption is a concern, clocked regenerative amplifier is preferred.

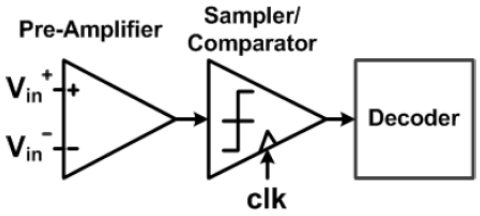
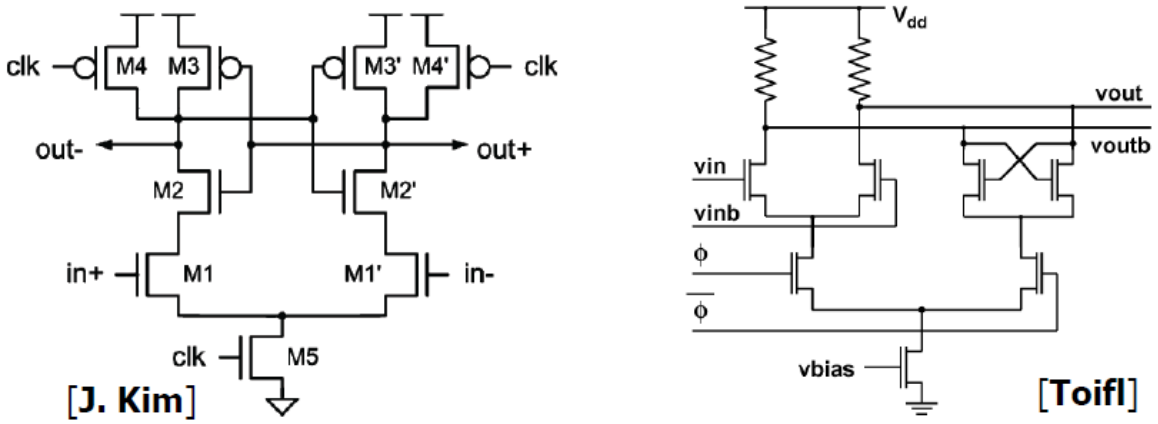


Figure 2 Basic Receiver Block Diagram

Clocked Comparators

Clocked comparators can sample the input signals at clock edges and resolve the differential output. They are also called regenerative amplifiers, sense-amplifiers, or latches. Two clocked comparators are shown in Figure 3. A flip-flop can be made by cascading a strong-arm latch and a SR latch as shown in Figure 4. It can also be formed by cascading two CML latches.



(a) (b)

Figure 3 Clocked Comparators (a) Strong-Arm Latch (b) CML Latch

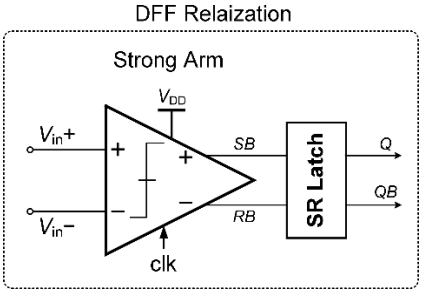


Figure 4 Flip-Flop Made of a Strong-Arm Comparator and an SR Latch

Clocked Comparator Linear Time-Variant (LTV) Model and ISF

A comparator can be viewed as a noisy nonlinear filter followed by an ideal sampler and slicer (comparator) as shown in Figure 5 [2]. The small-signal comparator response can be modeled using an impulse sensitivity function (ISF) of

$$\Gamma(\tau) = h(t,\tau) \tag{1}$$

The comparator ISF is a subset of a time-varying impulse response $h(t,\tau)$ for a linear time-variant (LTV) system, which can be expressed as

$$y(t) = \int_{-\infty}^{\infty} h(t,\tau)x(\tau)d\tau \tag{2}$$

where $h(t,\tau)$ is the system response at t to a unit impulse arriving at τ, and for a linear time-invariant (LTI) system $h(t,\tau) = h(t-\tau)$ using convolution. Output voltage of a comparator can be expressed as

$$V_o(t_{obs}) = \int_{-\infty}^{\infty} V_i(\tau)\Gamma(\tau)d\tau \tag{3}$$

and the comparator decision can be calculated as

$$D_K = sgn(V_K) = sgn\big(V_o(t_{obs} + KT)\big) = sgn\left(\int_{-\infty}^{\infty} V_i(\tau)\Gamma(\tau)d\tau\right) \tag{4}$$

Please refer to [2] for more details.

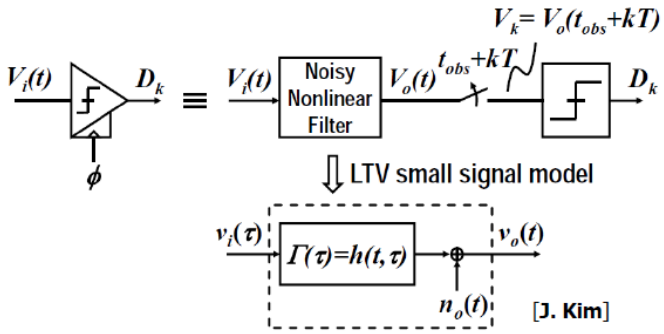


Figure 5 Clocked Comparator LTV Model

Characterizing Comparator ISF using Cadence

The method for characterization of a comparator's ISF can be found in [2]. The simulation setup is shown in Figure 6. A small step signal is applied to the comparator at time τ with a small offset voltage. The offset voltage is generated through a simple servo loop, which makes the comparator metastable. The $V_{metastable}$ is measured for various time τ to obtain the step sensitivity

function SSF(τ). Cadence simulation setup is shown in Figure 7. Both input step and clock signals are set to be the same frequency and with time τ delay. At the metastable condition, the flip-flop generates equal number of 1's and 0's. The percentage of 1's and 0's controls the average current flow direction of the voltage controlled current source (VCCS) which generates an offset voltage on the shunt capacitor. The simulation can be done by sweeping the time τ and measure the offset voltage. ISF can be eventually generated from those simulation results [2]. Please refer to the Appendix at the end of this document for more details on how to extract the ISF response in Cadence.

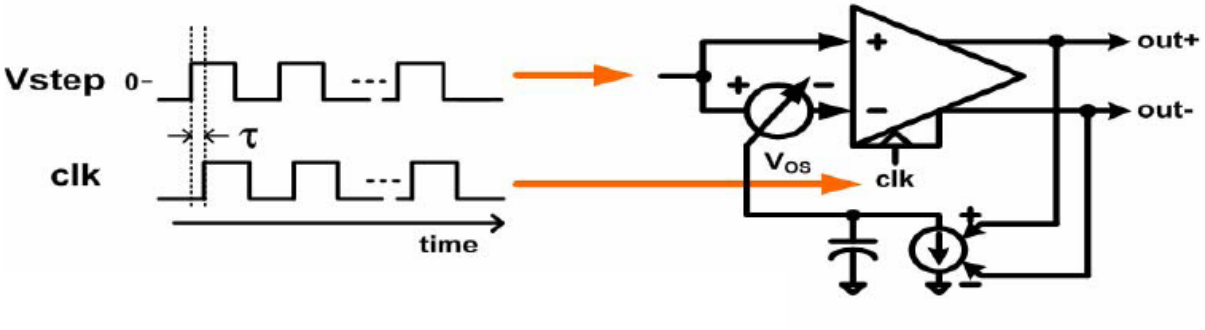


Figure 6 Characterization of Comparator ISF [Jeeradit, VLSI 2008]

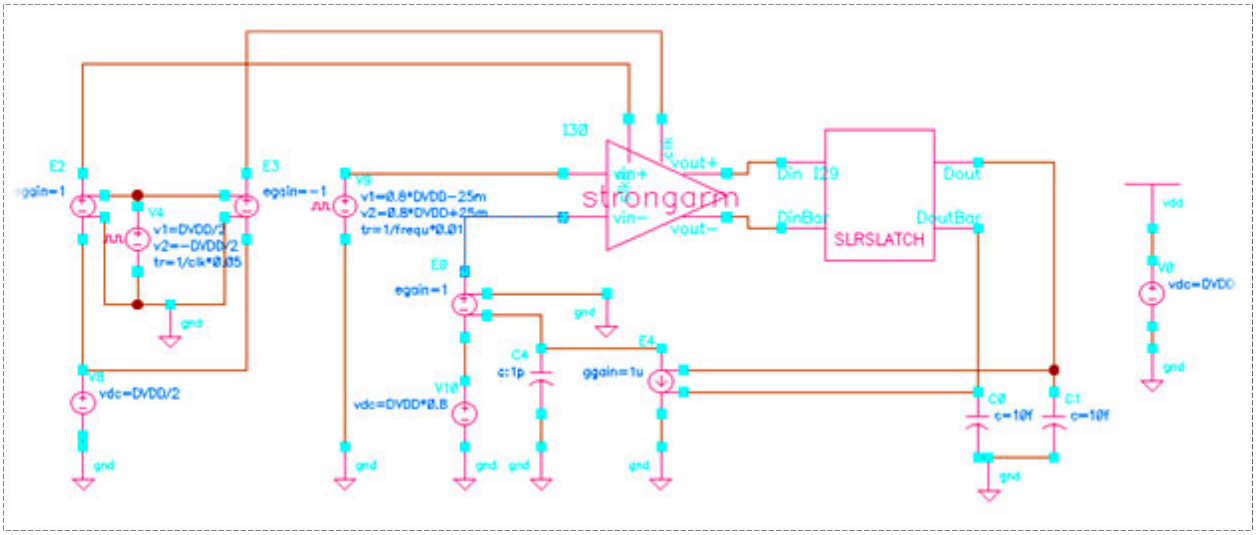


Figure 7 Comparator ISF Setup in Cadence

Pre-Lab

1. Generally, circuits are designed to handle a minimum variation range of ±3σ, where σ is the standard deviation of the variable under study. What is the yield rate for ±σ, ±2σ, ±3σ, and ±4σ assuming a Gaussian distribution?

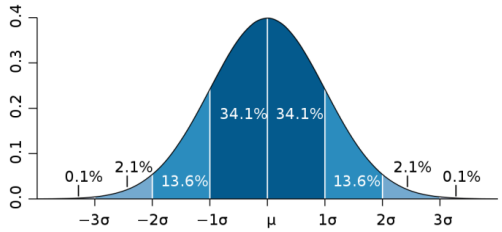


Figure 8 Gaussian distribution

2. A receiver is characterized by its input sensitivity which represents the voltage resolution, and by the set-up and hold times (t_S and t_H) which represent the timing resolution as illustrated with the light rectangle in Figure 1. The center of the dark rectangle is shifted by the offset time and offset voltage from the center of the light rectangle. Input sensitivity consists of input voltage offset, input referred noise, and minimum latch resolution voltage. A Strong-Arm latch input static voltage offset is 10mV, minimum latch resolution from hysteresis is bounded to 2mV, and 2mV sigma of input referred noise. The aperture time and the combined set-up and hold time (t_S+t_H) of the latch are 10ps and 20ps, respectively. Also assume that the receiver sampling clock has a 10ps timing offset and 1ps sigma of random jitter. The target BER is 10^{-12} (Hint: how many standard deviations does this imply?)

   On the 6Gb/s NRZ eye diagram obtained in Lab 2 over B12 backplane channel (either from MATLAB or CADENCE), draw the window that the incoming signal needs to avoid such that the receiver will reliably translate the voltage waveform received from the channel into logic 1's or 0's under worst-case combinations of offsets and resolution.

3. Demultiplexer (DeMUX) is often used to deserialize a stream of high speed data. It can be implemented after the receiver circuit to generate lower speed data. Please design a 1:4 binary-tree DeMUX that deserializes 6Gb/s data into 1.5Gb/s data. Figure 9 is an example of 1:2 De-MUX, please refer to [3] as a reference. You may use behavioral models to implement the building blocks in the DeMUX. Plot the simulation results that verify the operation of DeMUX.

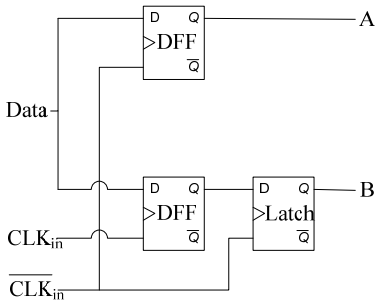


Figure 9 1:2 Data De-MUX [3]

Questions

1. **High-Speed Comparator Design.** This problem involves the design of four different high-speed comparators to meet the following specifications:
   a. clk → Dout delay ≤ 150ps with a 10mV static differential input voltage ($D_{in+}-D_{in-}$) at a common mode voltage of 80% VDD. Measure delay from when the clock is at 50% VDD to Dout+ is at 50% VDD for an output rising transition. Please refer to Figure 18 in the Appendix.
   b. Clock frequency = 3GHz. Use at least one inverter-based buffer to clock your circuit for realistic clock waveforms.
   c. Load capacitance on Dout+ and Dout- is 10fF.
   d. Input referred offset $\sigma \leq 10$mV. Here you can optimistically assume that the input referred offset is just due to the input differential pair Vt (threshold voltage) mismatch and use the mismatch equation given in the notes, i.e., no need to run Monte Carlo simulations (although if you have access to a PDK that includes accurate statistical models of the CMOS devices you are encouraged to use Monte Carlo analysis).
   e. Optimize the design for power consumption, i.e., don't overdesign the comparator for a super small delay. Try to minimize total capacitance while still meeting the ≤ 150ps delay and $\sigma_{offset} \leq 10$mV offset specifications.

   <u>Design the comparators based on the following four architectures:</u>
   a. **Conventional Strong-Arm Latch**. For an example schematic, refer to Figure 3(a). Feel free to change the pre-charge transistors configuration.

   b. **CML Latch**. For an example schematic, refer to Figure 3(b).

   c. **Schinkel Low-Voltage Latch**. For an example schematic, refer to Figure 2 in [6].

   d. **Goll Low-Voltage Latch**. For an example schematic, refer to Figure 2 in [7].

   <u>The comparators should realize a flip-flop function.</u>
   a. As shown in Figure 10, for the Strong-Arm type latches (1, 3, and 4) follow it with the optimized SR-latch shown in Figure 11. For more details on the optimized SR-latch, refer to [8].
   Note: for architecture (3) you will need to modify this optimized SR-latch – as the sense-amp pre-charges to GND (vs. VDD in 1 & 4).
   b. To realize a CML flip-flop with architecture (2), simply cascade two CML latches to realize a master-slave flip-flop.

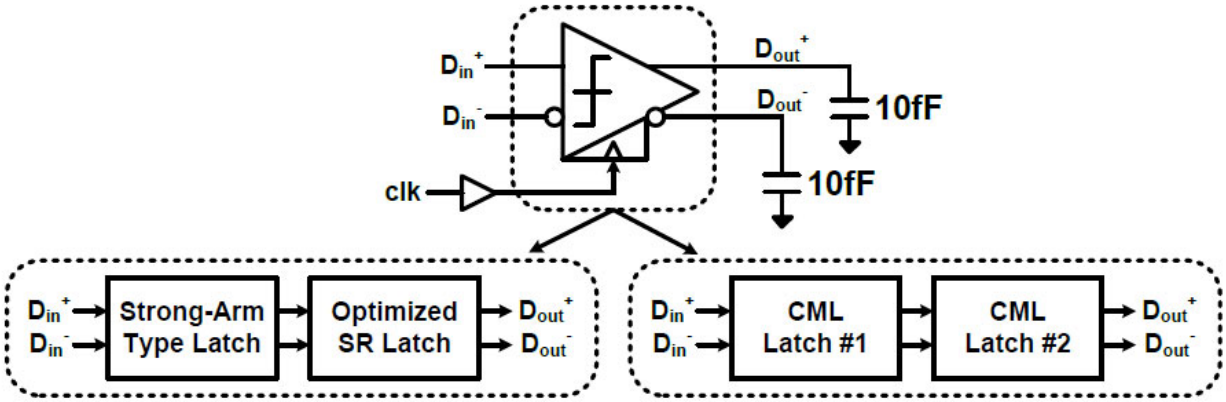


Figure 10 High-Speed Comparator with a Flip-Flop Configuration

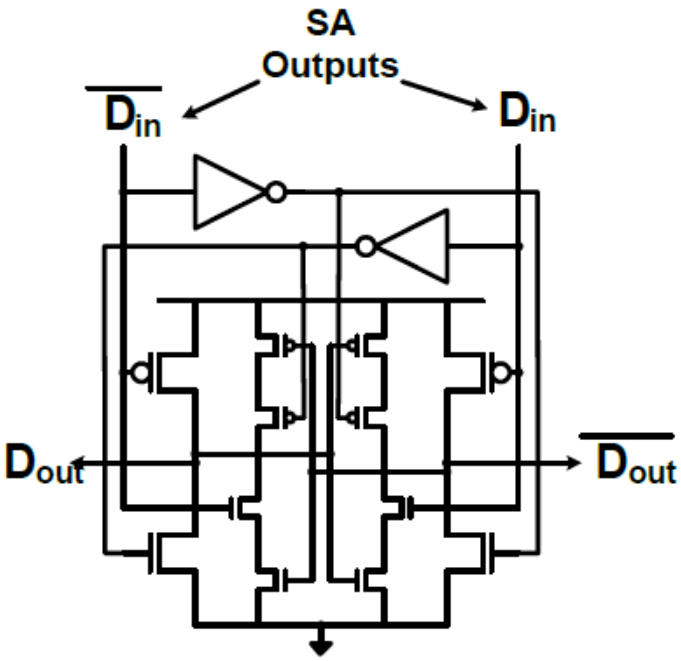


Figure 11 Optimized SR Latch [8]

2. **High-Speed Comparator Characterization.** Please simulate all four comparators and produce the following using 500MHz (or less if necessary) clock signal:

   a. **Plot comparator delay vs. VDD** for VDD varying from 50% of nominal VDD to 100% VDD. For this keep the input common mode equal to 80% of the supply, i.e., sweep the input common-mode along with the supply. Also scale the clock input signal level with VDD.
   b. **Plot comparator power vs. VDD** in a similar manner.
   c. **Generate the comparator Impulse Sensitivity Function (ISF) at the nominal VDD, 80%VDD, and 60%VDD (3 curves)**. Again, track the input common-mode with VDD (for more details refer to [2]). For the ISF-based characterization use an input differential step of 50mV, i.e., VCM±25mV for the differential input signals. **Report the comparator aperture time**, by measuring the 10%-90% "rise-time" based on the simulation results. Please refer to [9] for the aperture time measurement.
   d. Compare the design of these four latches (you can refer to [2]).

3. **Link Verification.** The designed comparator can be considered as a basic receiver. Build a 6Gb/s link system by using the transmitter designed either in voltage mode or current mode and the comparator which you've chosen for the best performance. Please refer to Figure 12 for the full test circuit. Use 50Ω transmission line with 1ns delay. Add 200fF parasitic caps at the output of your transmitter and input of the receiver. Feel free to choose the best termination and coupling schemes.
   a. Show the circuit schematic including coupling and termination.
   b. Explain your choice of coupling and termination schemes.
   c. Please show simulation results and eye diagrams that verify the link functionality and performance.

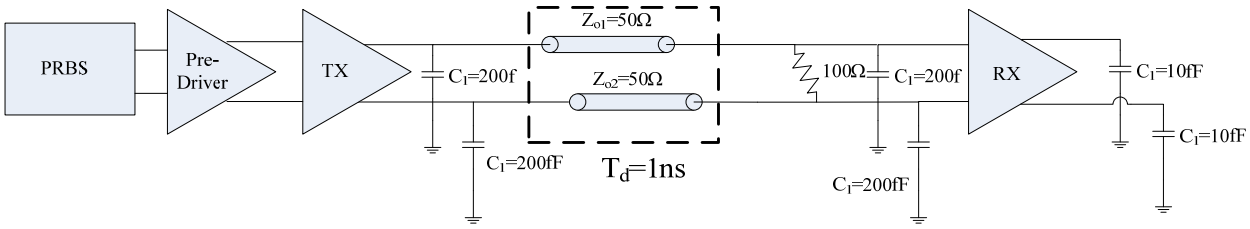


Figure 12 Basic Link System using DC Coupling

References

[1] *Digital Systems Engineering*, W. Dally and J. Poulton, Cambridge University Press, 1998.

[2] M. Jeeradit , J. Kim , B. S. Leibowitz , P. Nikaeen , V. Wang , B. Garlepp, and C. Werner, "Characterizing sampling aperture of clocked comparators," *Dig. Tech. Papers, IEEE Symp. VLSI Circuits*, pp. 68-69, June 2008.

[3] J. Cao, M. Green, A. Momtaz, K. Vakilian, D. Chung, K.-C. Jen, M. Caresosa, X. Wang, W.-G. Tan, Y. Cai, I. Fujimori, and A. Hairapetian, "OC-192 transmitter and receiver in standard 0.18-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 37, pp. 1768–1780, Dec. 2002.

[4] J. Kim *et al*., "Simulation and analysis of random decision errors in clocked comparators," *IEEE Transactions on Circuits and Systems-I*, vol. 56, no. 8, Aug. 2009, pp. 1844-1857.

[5] T. Toifl *et al*., "A 22-Gb/s PAM-4 receiver in 90-nm CMOS SOI technology," *IEEE J. Solid-State Circuits*, vol. 41, no. 4, Apr. 2006, pp. 954-965.

[6] D. Schinkel *et al*., "A double-tail latch-type voltage sense amplifier with 18ps setup+hold time," *IEEE International Solid-State Circuits Conference*, Feb. 2007.

[7] B. Goll and H. Zimmermann, "A comparator with reduced delay time in 65-nm CMOS for supply voltages down to 0.65V," *IEEE Transactions on Circuits and Systems-II*, vol. 56, no. 11, Nov. 2009, pp. 810-814.

[8] B. Nikolic *et al*., "Improved sense-amplifier-based flip-flop: design and measurements," *IEEE Journal of Solid-State Circuits*, vol. 35, no. 6, June 2000, pp. 876-884.

[9] H. O. Johansson and C. Svensson, "Time resolution of NMOS sampling switches used on low-swing signals," *IEEE J. Solid-State Circuits*, vol. 33, pp. 237 - 245, 1998.

Appendix

ISF Simulation Steps:

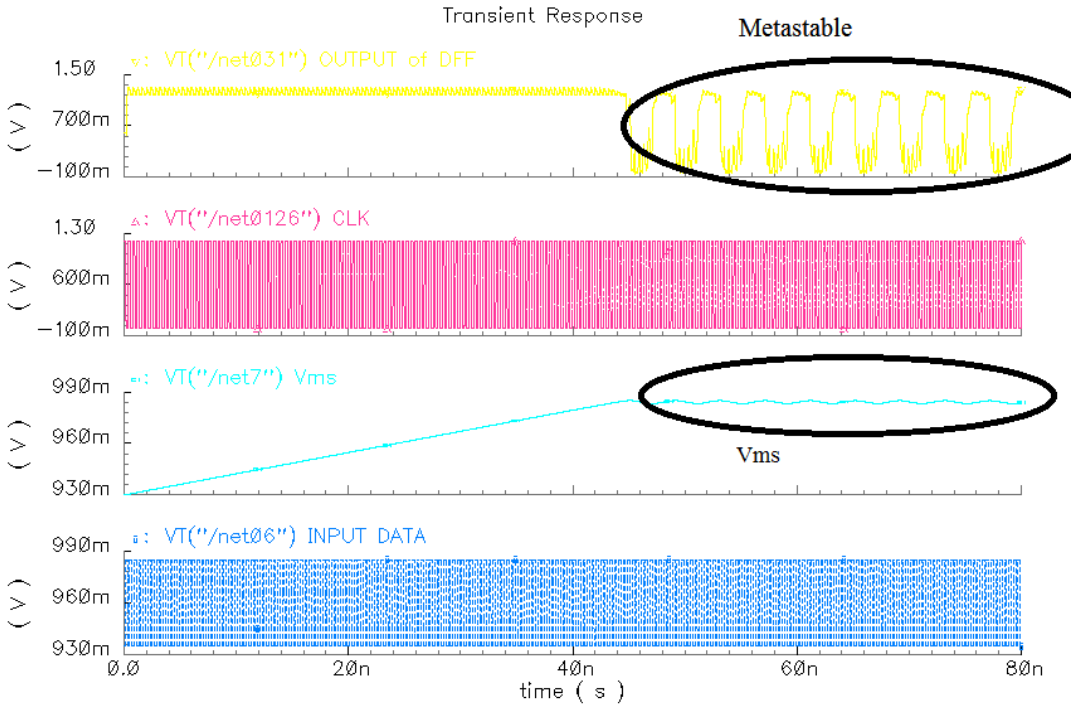


Figure 13 Transient Simulation of ISF Test Circuit at delay time τ

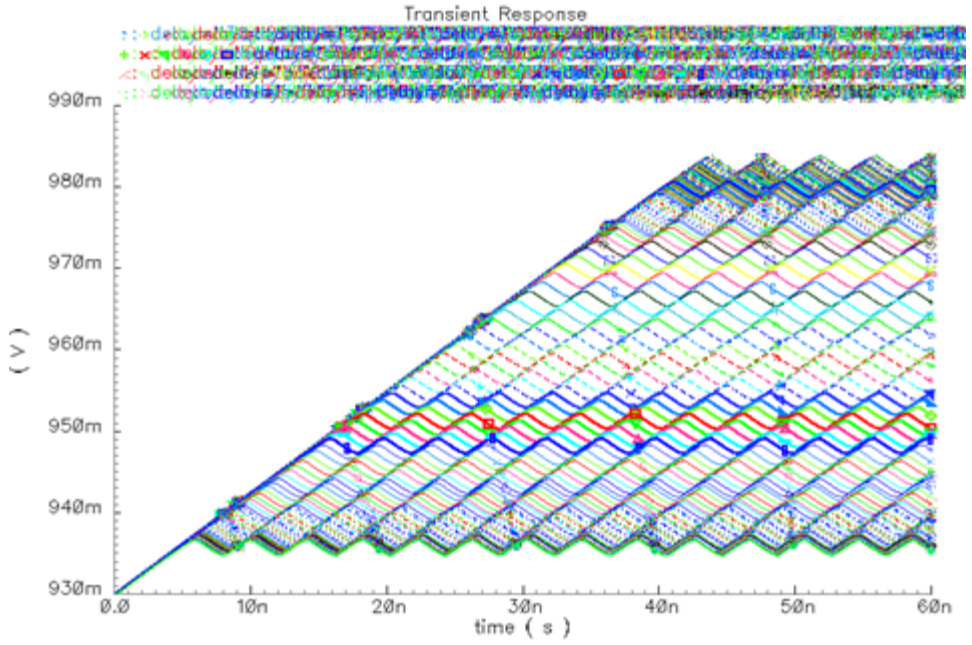


Figure 14 Direct Plot of V_{ms} at Each Time τ After Parametric Sweep

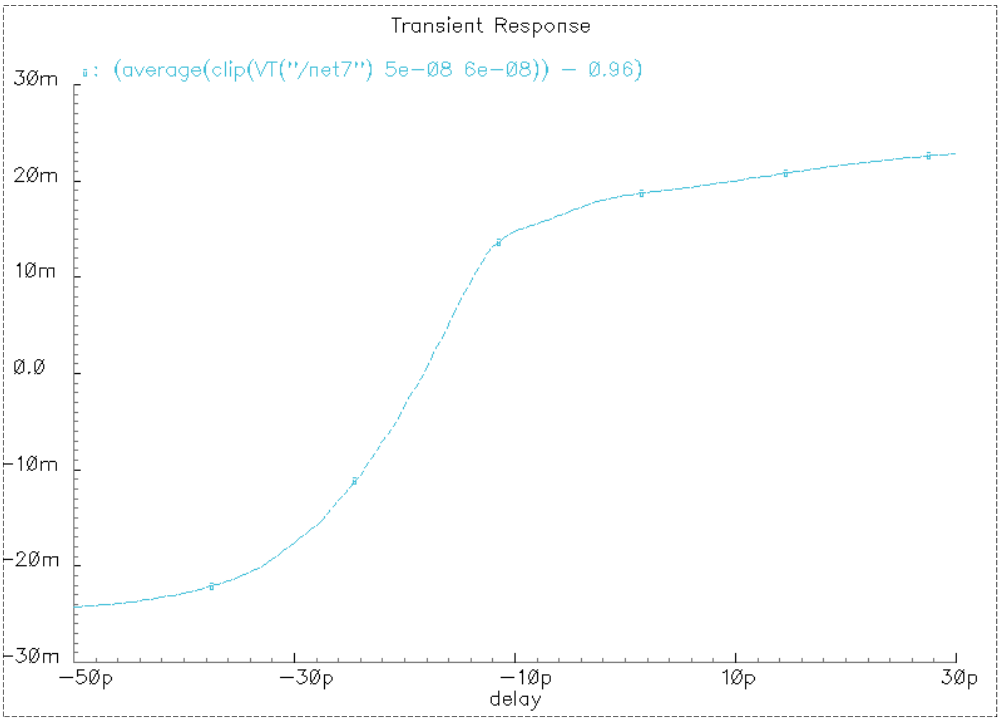


Figure 15 V_{ms} vs. Time τ with V_H=24.3mV and V_L=-24.3mV Through Measuring The Average Voltage of V_{ms} After Settling

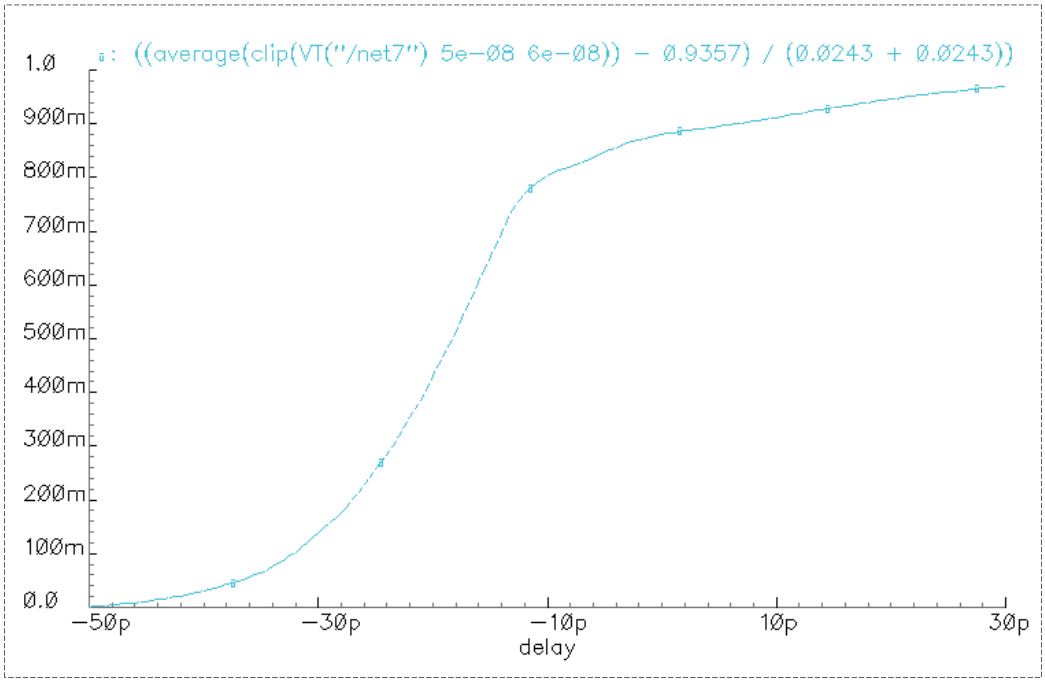


Figure 16 Generating SSF from Figure 15

Finally, the ISF can be plotted through taking the derivative of Figure 16 as shown in Figure 17.

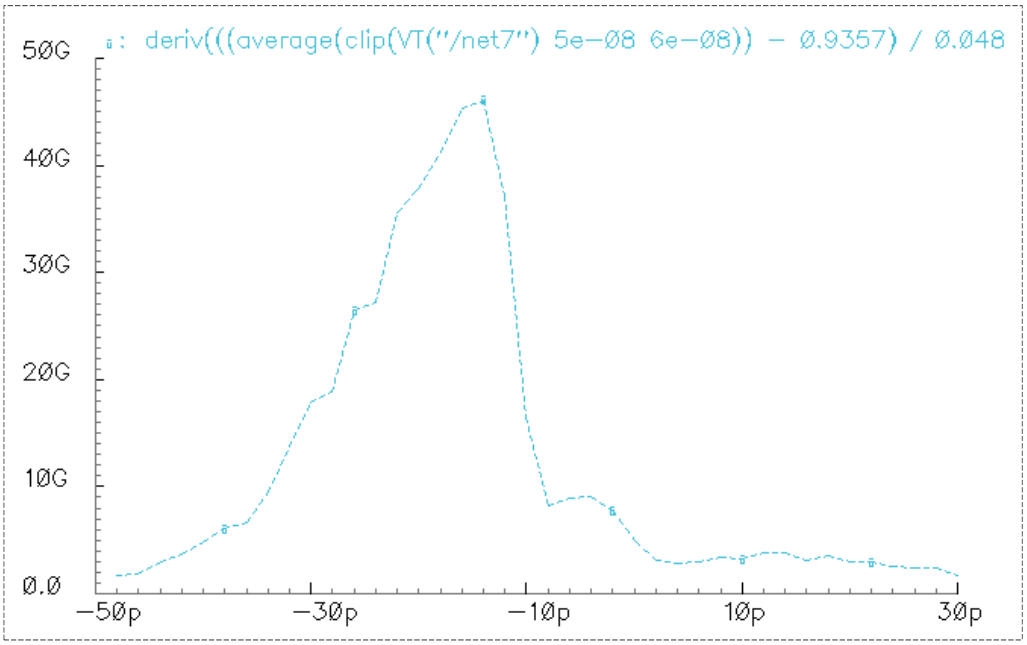


Figure 17 ISF for StrongArm (SA) Latch at 1.2V

CLK-to-Dout Delay Measurement:

To perform a reasonable CLK to Dout delay measurement, at some point the polarity of ($D_{in+}-D_{in-}$) has to be changed.

For example, as shown in Figure 18, before t = 0.75ns $D_{in+}-D_{in-}=-10mV$, while after this time $D_{in+}-D_{in-}=+10mV$.

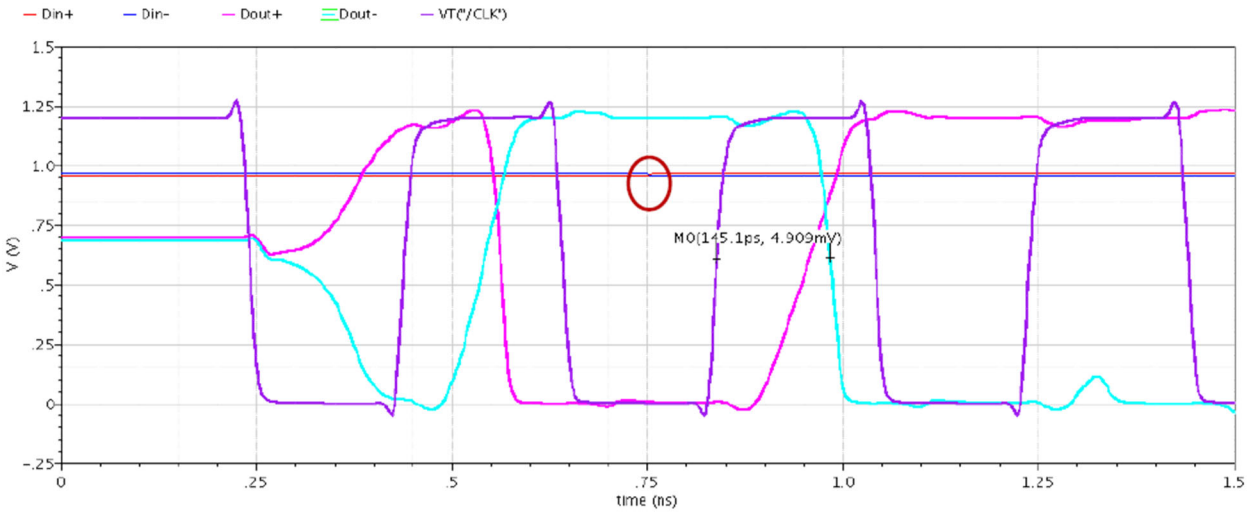


Figure 18 Clk-to-Dout Delay Measurement (I)

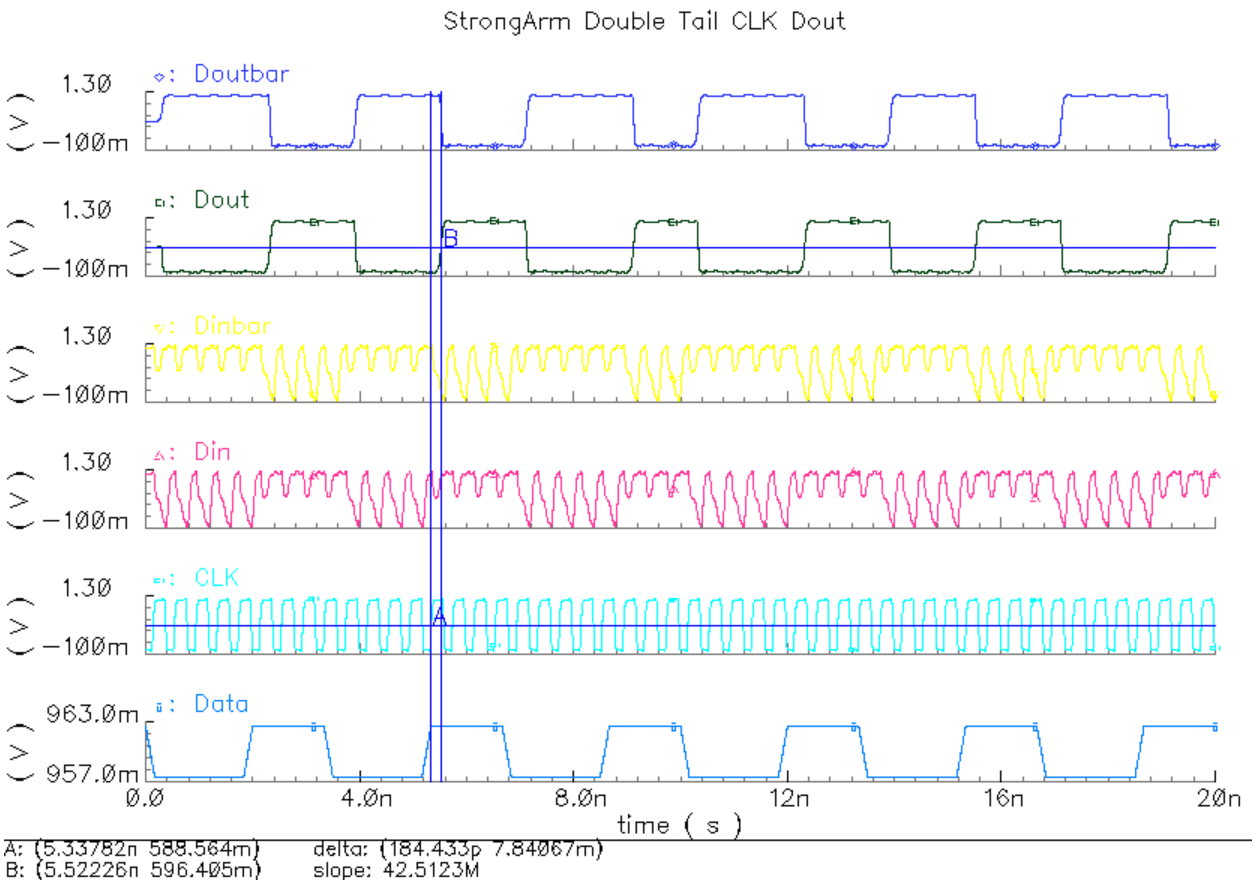


Figure 19 Clk-to-Dout Delay Measurement (II)