

ECEN 720 High-Speed Links: Circuits and Systems

Lab1 - Transmission Lines

Objective

To learn about transmission lines and time-domain reflectometer (TDR).

Introduction

Wires are used to transmit clocks and data signals. In base-band chip design, the wires are often treated as lumped parasitic loads. In high speed data communication chip design, the wires are often treated as transmission lines. Proper transmission line terminations are required to eliminate any reflections. In this lab, the characteristics and usage of basic transmission line model and its termination will be practiced. A time-domain reflectometer (TDR) consists of a step generator and an oscilloscope to measure the step response of the transmission line on the source side. The basic theory behind TDR will be explored during this lab.

Distributed System using Partial Differential Equation

The transmission line can be described as series resistance and inductance and parallel capacitance and conductance. An infinitesimal section of the wire is shown in Figure 1. Assuming V is a function of position and time, it can be described as

$$-\frac{\partial V}{\partial x} = RI + L \frac{\partial I}{\partial t} \quad (1)$$

$$-\frac{\partial I}{\partial x} = GV + C \frac{\partial V}{\partial t} \quad (2)$$

By differentiating the first equation with respect to x and substituting the second one into the first one gives

$$\frac{\partial^2 V}{\partial x^2} = RGV + (RC + LG) \frac{\partial V}{\partial t} + LC \frac{\partial^2 V}{\partial t^2} \quad (3)$$

If the conductance is set to zero, the equation can be written as follows

$$\frac{\partial^2 V}{\partial x^2} = RC \frac{\partial V}{\partial t} + LC \frac{\partial^2 V}{\partial t^2} \quad (4)$$

For high resistance T-lines such as long on-chip wires, the inductance can be ignored in equation (4). It then becomes the diffusion equation. The signal diffuses (low pass) down the line. The

signal edges are dispersed with distance. For T-lines with negligible resistance such as PCB traces, the resistance can be ignored in (4). It then becomes the wave equation.

Impedance of an Infinite Line

The impedance of the infinitesimal T-line model can be written as the following

$$Z_o = Rdx + Lsdx + \frac{1}{Csdx + Gdx + 1/Z_o} \quad (5)$$

Since dx is infinitesimal, the equation can be written as

$$Z_o = \left(\frac{R + Ls}{G + Cs} \right)^{1/2} \quad (6)$$

The impedance is complex and frequency dependent. Only if $R=G=0$, the impedance becomes real and frequency independent as the following

$$Z_o = \left(\frac{L}{C} \right)^{1/2} \quad (7)$$

which is independent of the T-line's length.

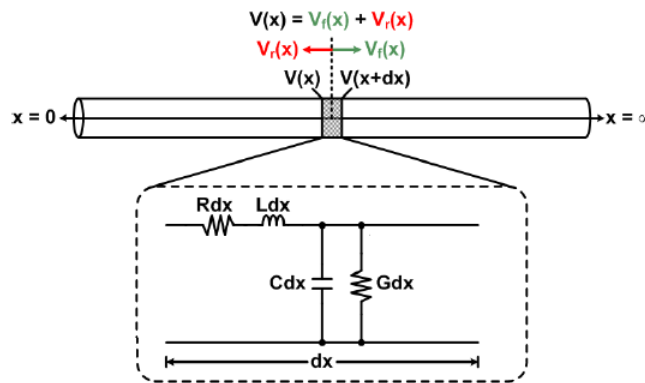


Figure 1 Infinitesimal Model of a T-Line

Reflections and Telegrapher's Equation

The Thevenin-equivalent model of a terminated transmission is given in Figure 2. The total current flowing through the termination Z_T is expressed as

$$I_T = \frac{2V_T}{Z_o + Z_T} \quad (8)$$

This current can be considered as the sum of forwarding current I_f and reflected current I_r . It can be written as

$$I_T = I_f - I_r \quad (9)$$

$$I_r = \frac{V_i}{Z_o} - \frac{2V_i}{Z_T + Z_o} \quad (10)$$

$$I_r = \frac{V_i}{Z_o} \left(\frac{Z_T - Z_o}{Z_T + Z_o} \right) \quad (11)$$

$$I_r = I_i \left(\frac{Z_T - Z_o}{Z_T + Z_o} \right) \quad (12)$$

With above derivation, the Telegrapher's equation can be written as

$$k_r = \frac{I_r}{I_f} = \frac{V_r}{V_f} = \frac{Z_T - Z_o}{Z_T + Z_o} \quad (13)$$

which relates the incident and reflected wave in both magnitude and phase.

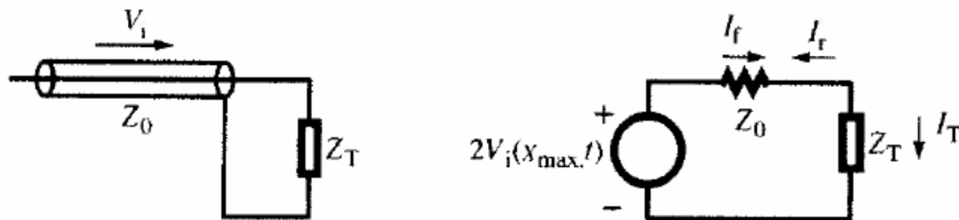


Figure 2 Terminating a Transmission Line [Dally]

Example:

Assuming the delay time of a transmission line as shown in Figure 8 is 1ns and the input source is 1V step with 1ns delay, while $R_S=400\Omega$, $R_T=600\Omega$, and $Z_0=50\Omega$, what is the voltage at source terminal at time=1ns? Calculate the reflection coefficient and draw the lattice diagram. What is the final value?

The time zero (1ns) voltage can be calculated using voltage divider as shown in Figure 3. It is calculated as

$$V_i = 1V * \frac{Z_o}{R_S + Z_o} = 1V * \frac{50}{400 + 50} = 0.111V \quad (14)$$

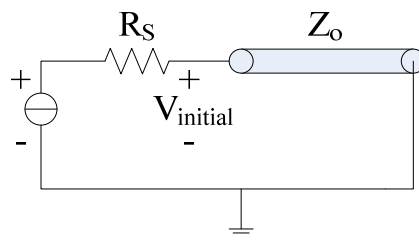


Figure 3 Initial Voltage Calculation

The reflection coefficient for the termination and source can be written as

$$K_{rT} = \frac{Z_T - Z_o}{Z_T + Z_o} = \frac{600 - 50}{600 + 50} = 0.846 \quad (15)$$

$$K_{rS} = \frac{Z_S - Z_o}{Z_S + Z_o} = \frac{400 - 50}{400 + 50} = 0.778 \quad (16)$$

At $t=2\text{ns}$ and on the load side, 0.111V incident wave is reflected back by the load termination impedance. The voltage at 2ns at the load is the sum of the incident wave and reflected wave. It is calculated by

$$V_{2ns} = 0.111 + 0.111 * K_{rT} = 0.205V \quad (17)$$

At $t=3\text{ns}$ and on the source side, the voltage is the initial 0.111V incident wave added by the reflected wave of $0.111 * K_{rT}$ and added by the voltage at $t=1\text{ns}$. It is shown as

$$V_{3ns} = 0.111 + 0.111 * K_{rT} + 0.111 * K_{rT} * K_{rS} \quad (18)$$

By following the above procedures, the lattice diagram can be created as shown in Figure 4.

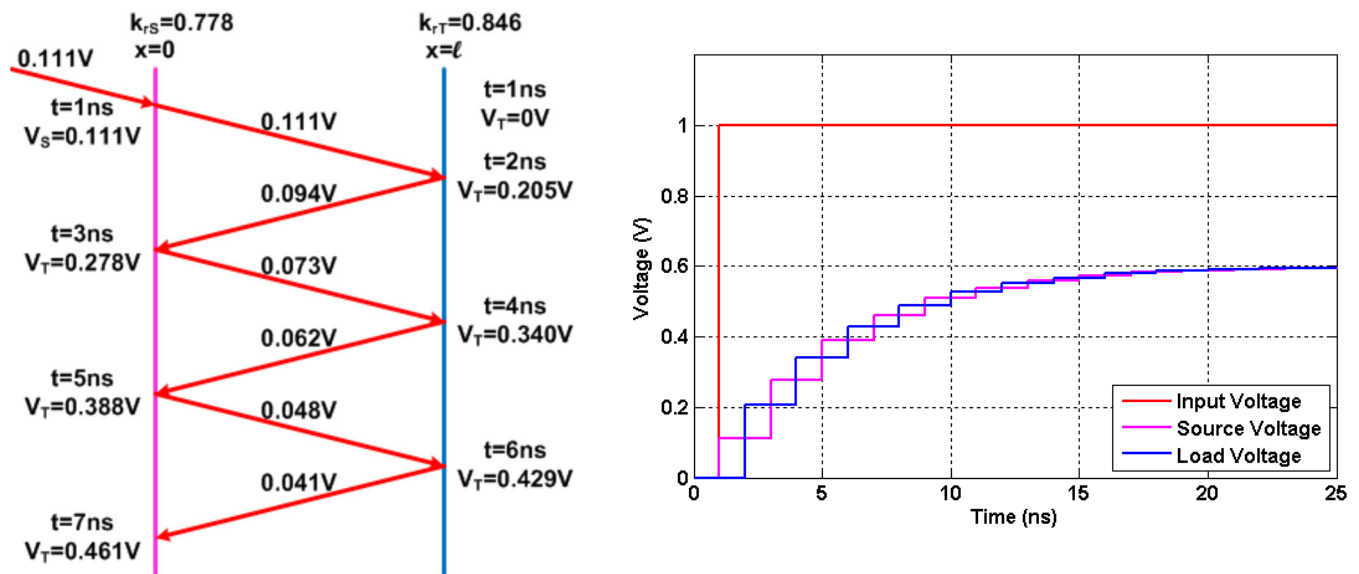


Figure 4 Lattice Diagram and Incident and Reflected Waves

The final value can be calculated using voltage divider again as shown in Figure 5. It is 0.6V .

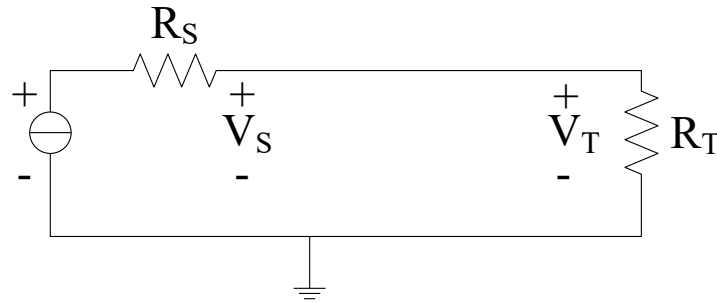


Figure 5 Final Value Equivalent Circuit

Lossy LRC Transmission Lines

In long LC transmission lines, losses cannot be neglected. The traveling wave is attenuated and dispersed by the resistance and the conductance. The resistance varies with frequency due to the skin effect. The conductance of the line changes with frequency due to the dielectric absorption.

Ignoring the frequency dependent skin effect and dielectric absorption, the amplitude of the traveling wave along the line is expressed as

$$\frac{|V_i(x)|}{|V_i(0)|} = \exp \left[- \left(\frac{R}{2Z_o} + \frac{GZ_o}{2} \right) x \right] \quad (19)$$

where x is the distance.

Time-Domain Reflectometer

Time-Domain Reflectometer is the most popular measuring instrument for characterizing a transmission line's discontinuities, through observing the step response at the source in time domain. A TDR block diagram is shown in Figure 6. In this figure, the voltage at $t=10\text{ns}$ is caused by the transmission line Z_o discontinuity and the reflected wave superimposes at the source. At $t=20\text{ns}$, the reflected wave reaches the source from the shorted load termination and causes the voltage drop.

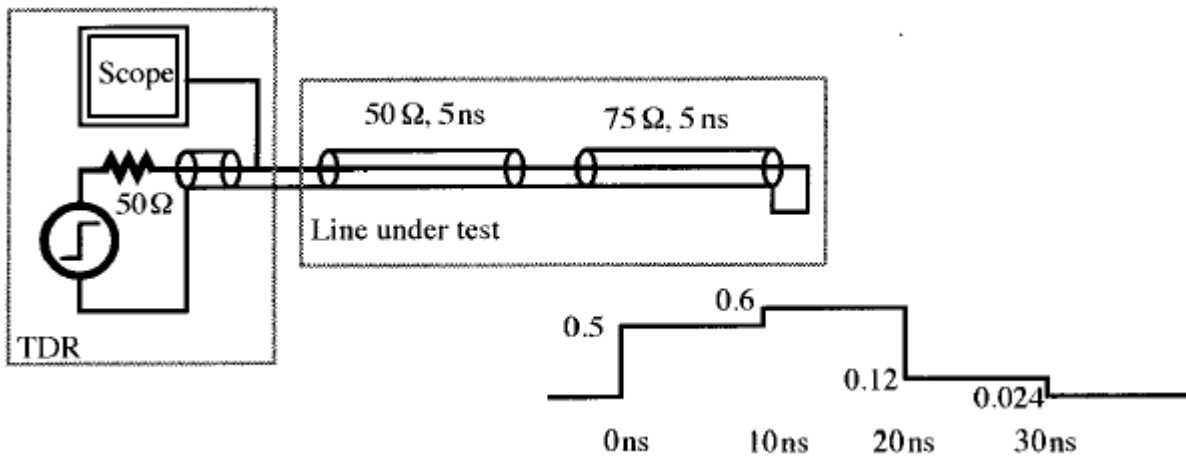


Figure 6 Time Domain Reflectometer [Dally]

Lumped capacitive and inductive discontinuities can also be detected through TDR as shown in Figure 7. A capacitor shows low impedance characteristic at high frequency, but an inductor shows high impedance characteristic. Suppose an ideal step signal is injected into an unknown transmission line, a capacitive discontinuity appears to be under-terminated looking at the source. A sudden voltage drop is observed by TDR. An inductive discontinuity appears to be over-terminated with opposite effect.

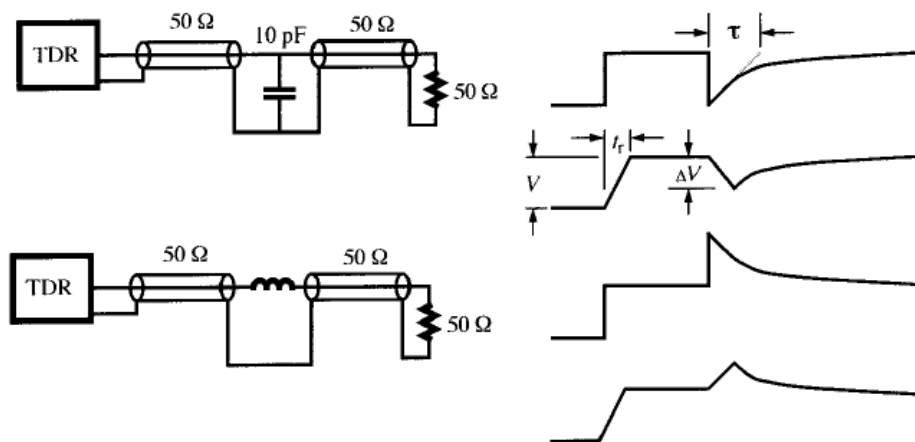


Figure 7 Impedance Discontinuities due to Lumped Capacitance and Inductance [Dally]

Not only the discontinuities, but also the positions and values can be calculated through TDR. The decay time constants (τ) of the capacitive and inductive discontinuities are expressed as

$$\tau_c = Z_o C / 2 \quad (20)$$

$$\tau_L = L / (2Z_o) \quad (21)$$

With finite step rise time, the peak magnitude of the discontinuity is

$$\frac{\Delta V}{V} = \left(\frac{\tau}{t_{rise}} \right) \left[1 - \exp\left(-\frac{t_{rise}}{\tau}\right) \right] \quad (22)$$

Pre-Lab:

1. Please work out the waveforms using Lattice Diagram for the terminated transmission line as shown in Figure 8. Assuming the delay time of the transmission line is 2ns and the input source is 1V step with 1ns delay. $R_S=100\Omega$, $R_T=30\Omega$, and $Z_0=50\Omega$

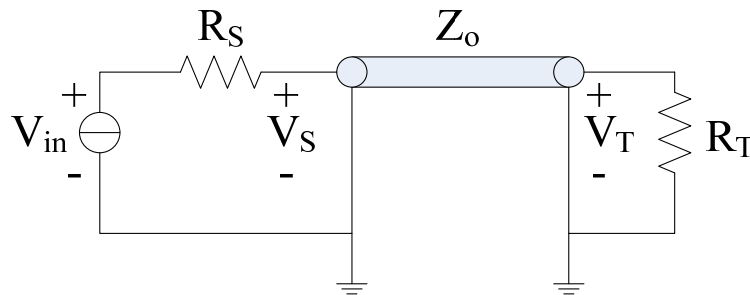


Figure 8 Transmission Line Termination Example

2. Please comment on the pros and cons of source termination and receiver termination schemes as shown in Figure 9.

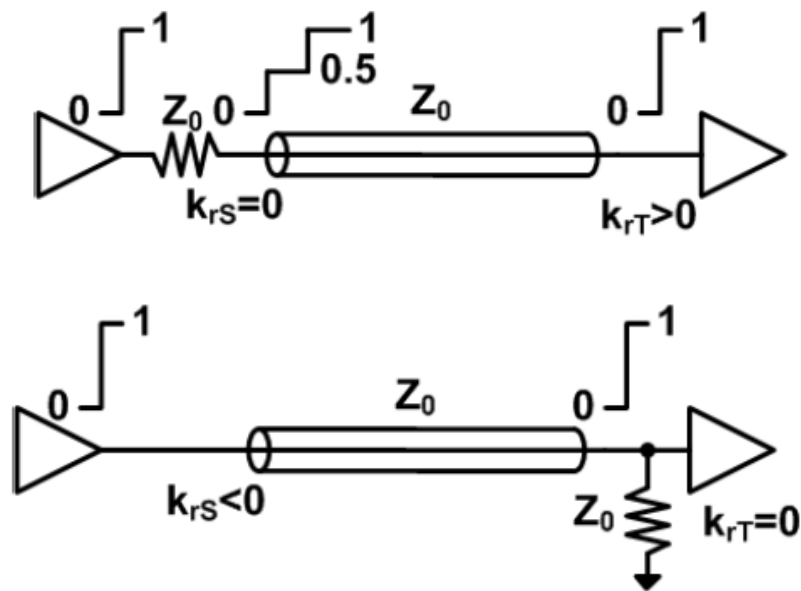


Figure 9 Source and Receiver Termination Schemes

Questions

1. LC Transmission Line Termination

Repeat the pre-lab question. Please work out the waveforms for the terminated transmission line circuit as shown in Figure 8. Please compare these three cases in terms of signal integrity. What is the final value in each case?

Case 1: $R_S=50\Omega$ $R_T=50\Omega$ $Z_0=50\Omega$

Case 2: $R_S=25\Omega$ $R_T=100\Omega$ $Z_0=50\Omega$

Case 3: $R_S=150\Omega$ $R_T=25\Omega$ $Z_0=50\Omega$

2. TDR is used to characterize interconnect for any impedance discontinuities.

- Please hand draw the TDR responses for the circuits shown in Figure 10 with an input step of 25ps rise time. Verify your results using Cadence. $Z_{01}=Z_{02}=R_T=50\Omega$. $T_{\text{delay}}=1\text{ns}$.
- TDR spatial resolution is set by the rise time of the step signal. Assuming a TDR generates a 1V step signal and measures its response using a 10-bit ADC. Please derive the minimum required step rising time versus TDR minimum lumped capacitance resolution curve.

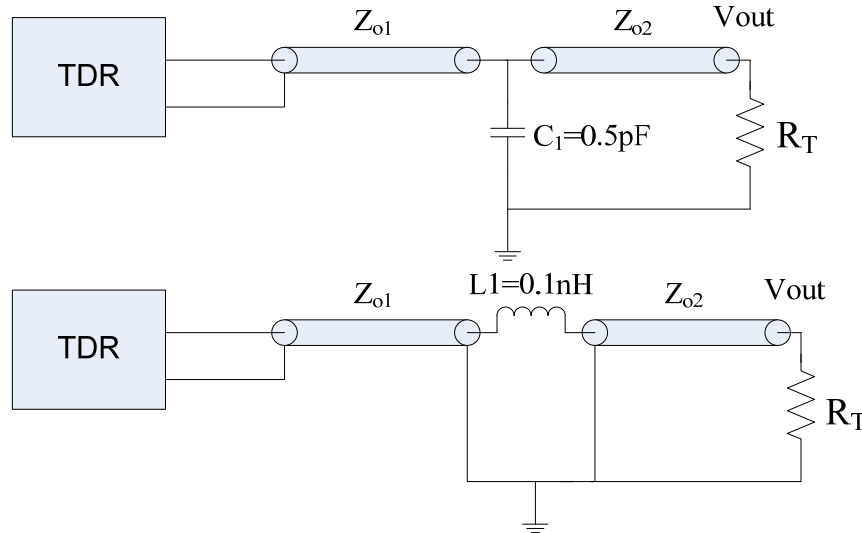


Figure 10 TDR Measurement on Lumped Discontinuities

- In a digital circuit, an open drain PMOS transistor functions as a buffer to drive a 50Ω testing probe as shown in Figure 11. The testing probe provides a 50Ω termination with respect to ground. The output pad and pin parasitic capacitance can be estimated to be 0.5pF each. Assuming 3mm bond wire, the bond wire parasitic resistance and inductance are $1\Omega/\text{mm}$ and $1\text{nH}/\text{mm}$. For 90nm technology, please use nominal 1.1V supply.

- Please measure the frequency response (impedance) of the PMOS transistor load and show and explain briefly the results.
- Design the open drain driver to output 300mVpp using 1.5GHz full swing square wave input signal (40ps rise time). Compare the output signal with the ideal case (no parasitic). Explain the effect of parasitic resistance, capacitance and inductance. What happens if 200MHz input signal is used? Does rising and falling times affect the output signal? Change the input to a 7-bit 2.5Gb/s PRBS (pseudo random bits) input data, comment on the output signal and its ripple.

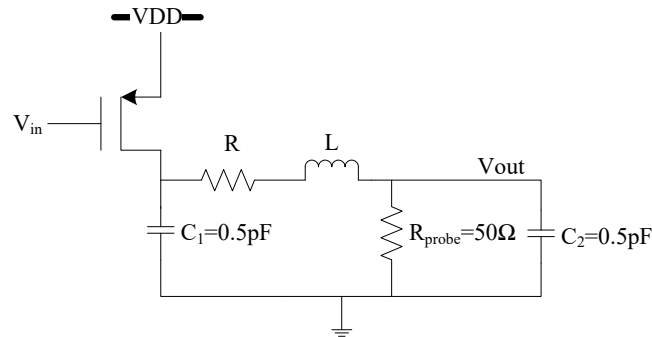


Figure 11 PMOS Open Drain Driver

- Suppose the same buffer is used to transmit the signal through two segments of PCB trace as shown in Figure 12. Z_{01} is 50 Ω and Z_{02} is 80 Ω . Please use only resistors to design the termination so that there are no reflections from a wave traveling from left to right. What kind of modification is needed to output a 300mVpp signal at V_{out} ?
- The signal at the output contains ripple (inter symbol interference (ISI)). What kind of problems it may introduce to the receiver stage?

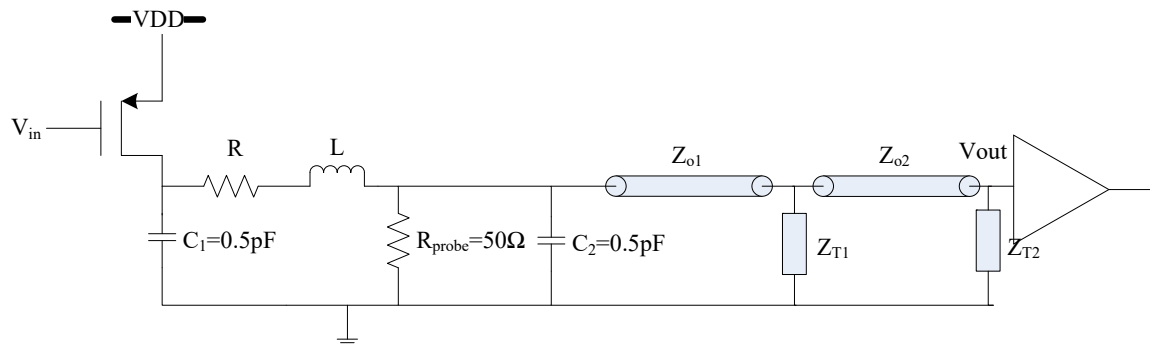


Figure 12 Transmission Line Matching Network

4. Please develop a model circuit composed of ideal transmission lines, inductors, resistors, and capacitors which generates the same response as Figure 13. The input rise time is 0.1ns. Please show your model circuits and Cadence simulation result.

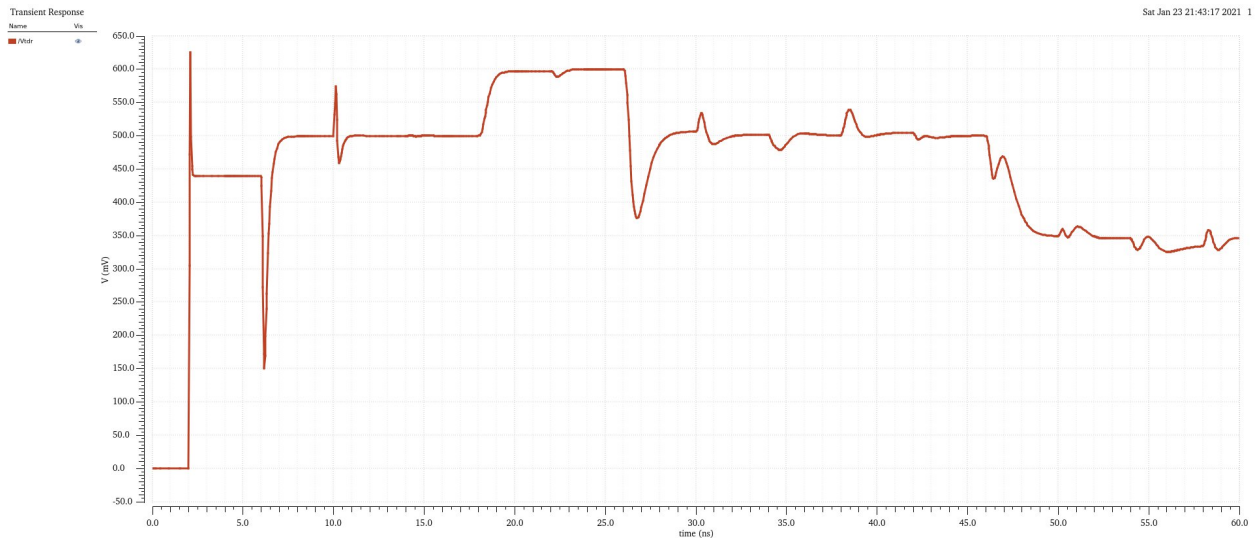


Figure 13 TDR Response

Please include your design procedure, simulation schematics and results in your lab report.

Appendix

Use Transmission line model in Cadence

Step 1: Find the T-line symbol in Library Manager as shown in Figure 14

Step2: Specify the tline delay and characteristic impedance as shown in Figure 15.

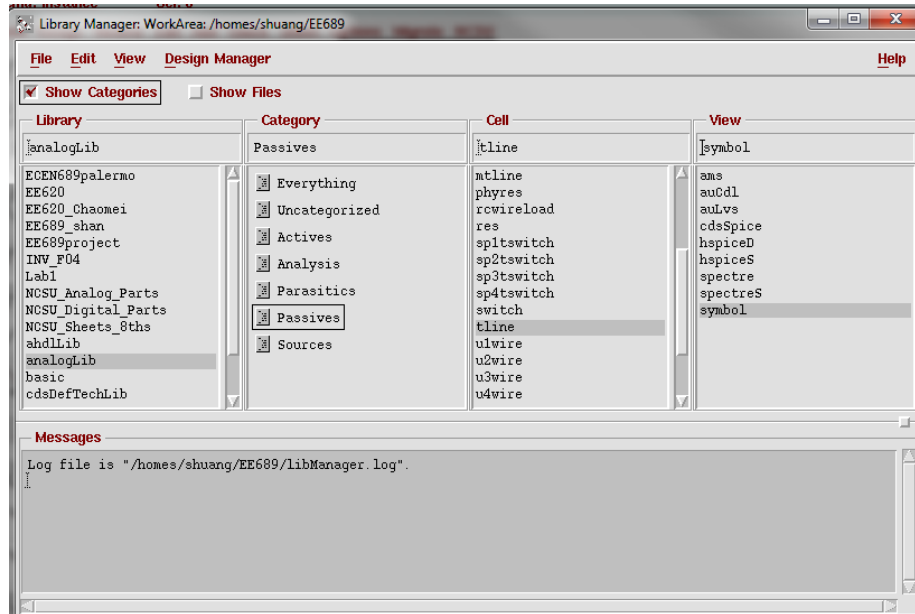


Figure 14 analogLib: transmission line model

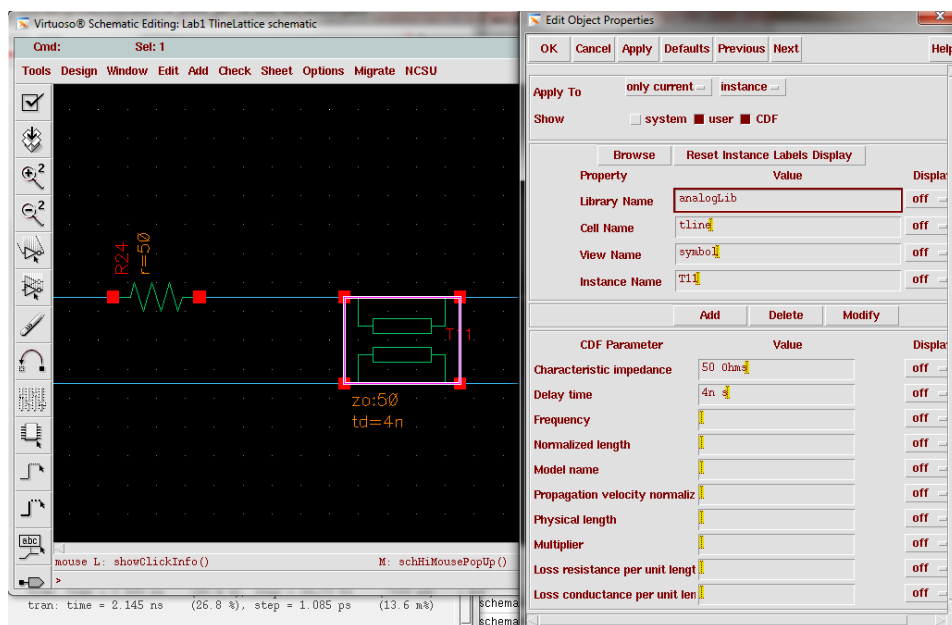


Figure 15 T-line Properties in analogLib

Reference

- [1] *Digital Systems Engineering*, W. Dally and J. Poulton, Cambridge University Press, 1998.