ECEN 689 High-Speed Links Circuits and Systems

Lab5 –Equalization Circuits

Objective

To learn fundamentals of high speed I/O link equalization techniques.

Introduction

An ideal cable could propagate all frequency components without any loss. In reality, all the electrical transmitting mediums have finite signaling bandwidth which limits the data rate of binary signaling. Fortunately, engineers have developed equalization schemes both at transmitter side and receiver side to compensate the loss of transmitting mediums and extend a channel's maximum data rate. In this lab, TX feed-forward equalization (FFE) will be studied, which acts as an FIR filter and pre-distorts transmitted pulse in order to invert channel distortion. At receiver side, RX FIR, continuous time linear equalizer (CTLE) and decision feedback equalizer (DFE) will be studied, which are implemented as part of receiver circuits and flatten the system response through conditioning the receiving signal. In addition to the link equalization, noise sources in high-speed link systems will be introduced in this lab. Figure 1 shows a high-speed electrical link using TX FFE equalization and RX CTLE+DFE equalization.

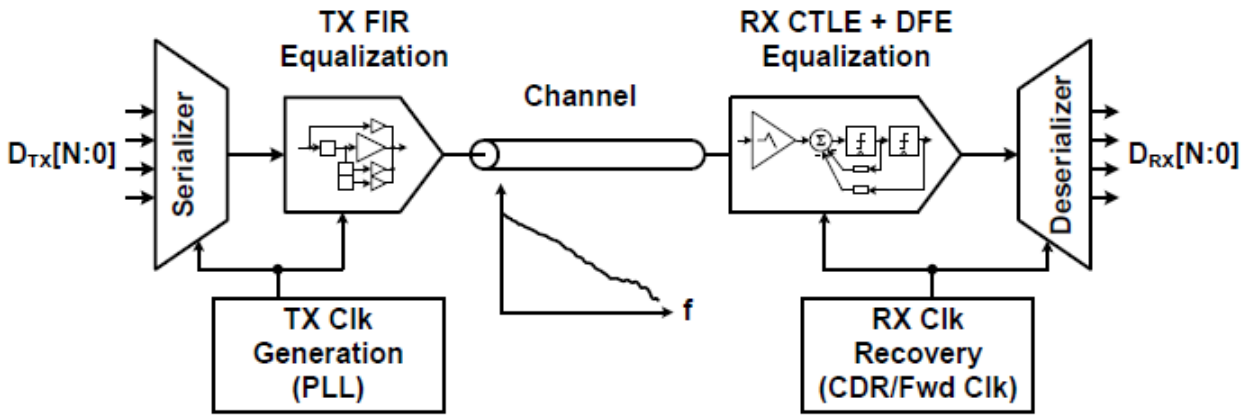


Figure 1 High-Speed Electrical Link with Equalization Schemes

TX Feed-Forward Equalization

Transmit equalization is the most common technique in high-speed links design. It is usually implemented through an FIR filter. It pre-distorts or shapes the data over several bit periods in order to invert the channel loss/distortion. The low frequency components get de-emphasized in

order to flatten the channel response. Without a FIR equalizer, the TX driver transmits 1 as a single pulse as the red curve shown in Figure 2(a). The pulse is dispersed by the channel loss/distortion. It is shown as the red curve in Figure 2(b) with pre-curse ISI and post-curse ISI. By using FFE, the pulse is shaped as the blue curve shown in Figure 2(a). The pulse is shaped based on the channel response. The pulses at time -1 and +1 are generated to cancel the channel pulse response's ISI. The equalized pulse is shown as the blue curve in Figure 2(b).

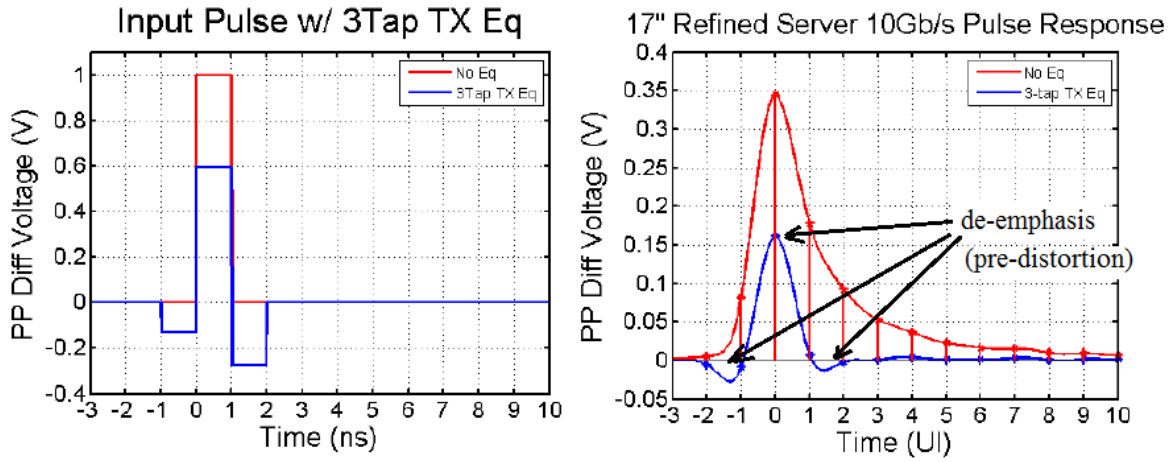


Figure 2 With (blue)/Without(red) FFE Equalizer (a) TX data pattern (b) Transmitted data pattern at RX side

TX FFE can be implemented as a FIR filter by using unit time delay elements (flip-flops) and current steering DAC circuit as shown in Figure 3(a). Compared with implementing a FIR filter at the receiver side, it is generally easier to build high-speed digital-to-analog converters versus receive-side analog-to-digital converters. However, the transmitter is limited by the peak transmitting power across the channel due to driver voltage headroom. Channel response flattening is realized through attenuating low-frequency signal content as shown in Figure 3(b).

Pros:

- High speed DAC is relatively easy to implement compared with receiver high speed ADC.
- TX FFE can cancel pre-cursor ISI.
- Due to the digital nature of the TX FFE, the noise is not amplified.
- 5-6 bit resolution can be achieved.

Cons:

- To flatten the channel response, low frequency content is attenuated due to the peak-power limitation.

- To tune the FIR taps, a feedback path from receiver side is required to detect channel response.

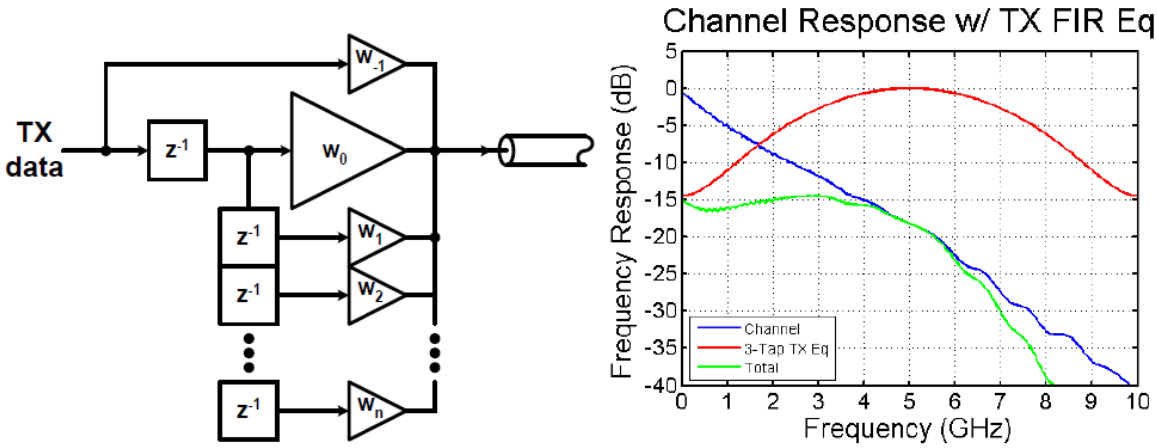


Figure 3 TX Equalization with an FIR Filter (a) FFE Equalizer (b) Channel Response

Example:

Given TX FIR z domain transfer function (1), find the low frequency response and Nyquist frequency response?

$$W(z) = -0.131 + 0.595z^{-1} - 0.274z^{-2} \tag{1}$$

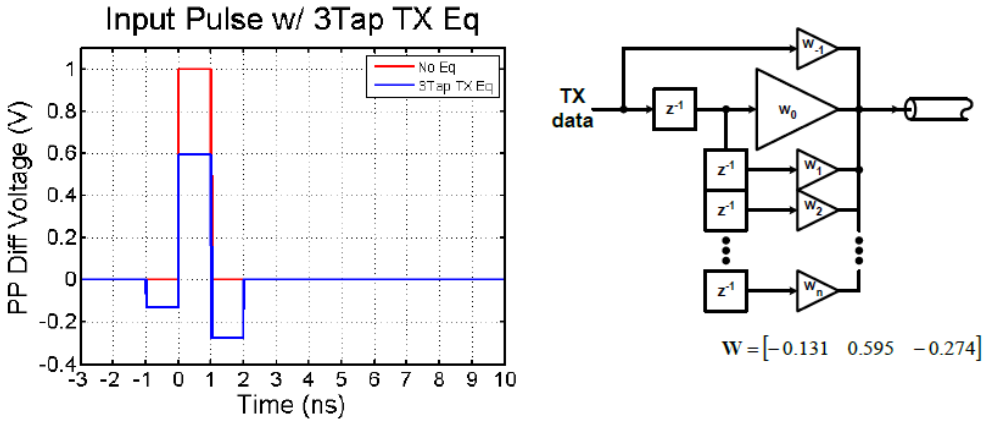


Figure 4 TX FFE Example

At the low frequency, we can assume that data pattern is infinite number of 1 as [….1 1 1 1 1 1….]. The z domain transfer function is [w_{-1} w_0 w_1] = [-0.131 0.595 -0.274]. The low frequency response can be expressed as

$$[\ldots.1\ 1\ 1\ 1\ 1\ 1\ \ldots.] * [-0.131\ 0.595\ -0.274] = [\ \ldots\ \ldots.0.190\ 0.190\ 0.190\ \ldots\ \ldots.] \tag{2}$$

Alternatively, at low frequency f=0 and in z domain, z=cos(0)+jsin(0)=1, the transfer function can be written as

$$W(1) = -0.131 + 0.595(1^{-1}) - 0.274(1^{-2}) = 0.190 = -14.4dB \quad (3)$$

At the Nyquist frequency, the data pattern is infinite number of -1 and 1 as [….-1 1 -1 1 -1 1….]. The Nyquist frequency response can be expressed as

$$[\ldots.-1\ 1-1\ 1-1\ 1\ldots.] * [-0.131\ 0.595\ -0.274] = [\ \ldots\ldots.1\ , -1,\ \ 1\ \ldots\ldots.] \quad (4)$$

Alternatively, at Nyquist frequency f=1/2T_s and in z domain, z=cos($2\pi fTs$)+jsin($2\pi fTs$)=1, the transfer function can be written as

$$W(1) = -0.131 + 0.595(-1^{-1}) - 0.274(-1^{-2}) = -1 = 0dB \quad (5)$$

Therefore the FIR attenuates DC at -14.4dB and passes Nyquist frequency at 0dB.

RX FIR Equalization

FIR equalization can be realized in receiver side as shown in Figure 5. Since the receiving signal contains the channel response information, the filter tap coefficients can be adaptively tuned to the specific channel which is the major advantage of receiver side equalization. However, the implementation of the analog delay elements is the major challenging in circuit level realization. The high-frequency noise content and crosstalk are also amplified along with the incoming signal. Noise amplification can be illustrated in Figure 6. RX FIR equalization can also be realized in digital domain. Due to the speed of the ADC, power consumption can be very high.

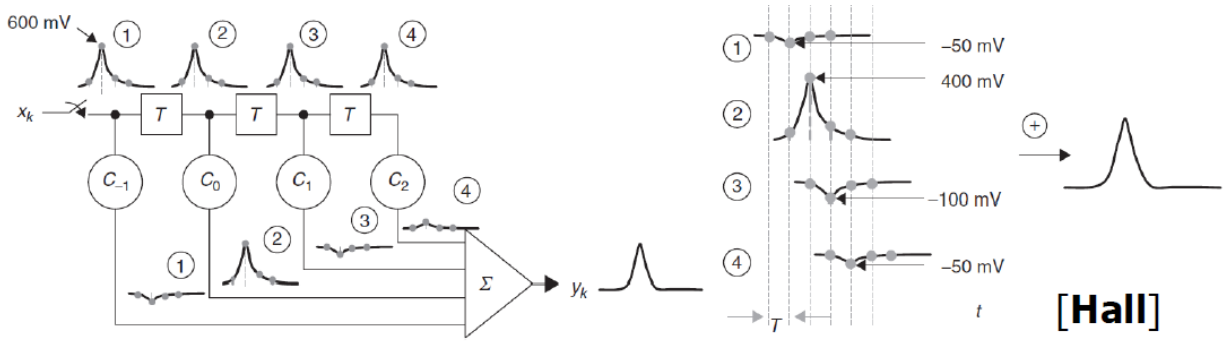


Figure 5 Receiver FIR Equalization

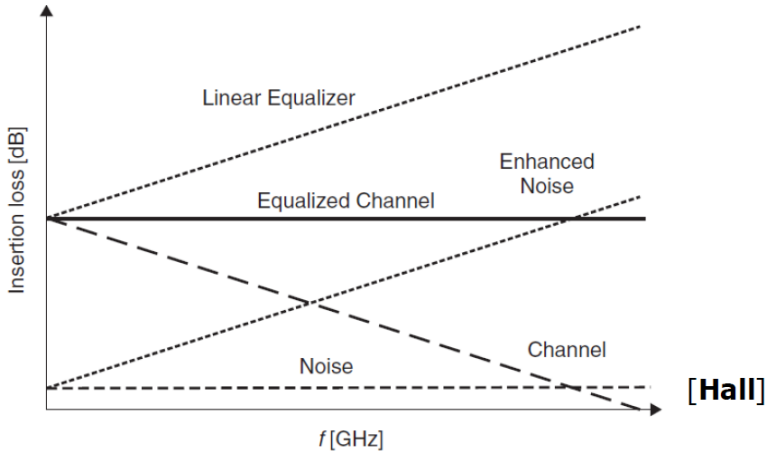


Figure 6 RX Equalization Noise Enhancement

Pros

- Amplify high frequency content rather than attenuate low frequency components.
- Cancel both pre-cursor and beyond filter span ISI.
- Filter tap can be adaptively tuned.

Cons

- Noise and crosstalk are amplified at the same time
- Analog delays are not easy to implement and tap precision is difficult to meet.

RX Continuous-Time Linear Equalizer (CTLE)

Both linear passive and active filter can realize high-pass transfer function to compensate for channel loss as shown in Figure 7. Both pre-cursor and long-tail ISI can be cancelled using the linear equalizer.

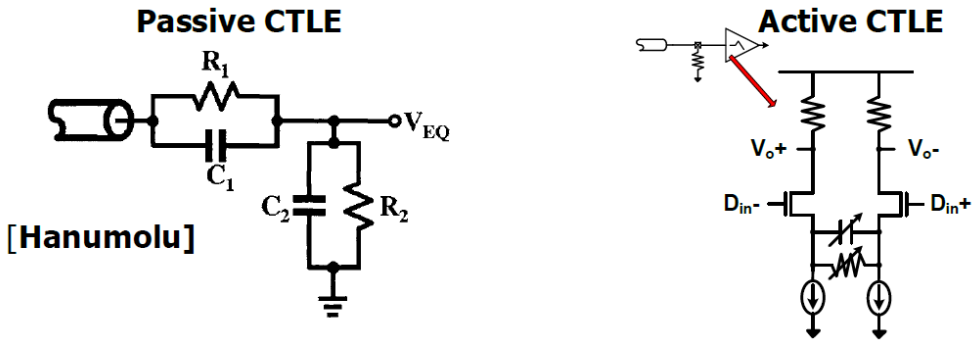


Figure 7 (a) Passive CTLE (b) Active CTLE

The passive CTLE is the combination of passive low pass filter and high pass filter. The transfer function of Passive CTLE shown in Figure 7 (a) can be written as

$$H(S) = \frac{R_2}{R_1 + R_2} \frac{1 + R_1 C_1 S}{1 + \frac{R_1 R_2}{R_1 + R_2}(C_1 + C_2)} \tag{6}$$

At DC, the capacitors can be ignored and the filter becomes a resistor divider circuit. DC gain is written as

$$DC\ gain = \frac{R_2}{R_1 + R_2} \tag{7}$$

At AC, the capacitors become low impedance elements. The AC gain is determined by capacitors. It is written as

$$AC\ gain = \frac{C_1}{C_1 + C_2} \tag{8}$$

For the passive filter, there is no gain at Nyquist frequency and the peaking is calculated as

$$peaking = \frac{AC\ gain}{DC\ gain} = \frac{\omega_p}{\omega_z} = \frac{R_2}{R_1 + R_2} \frac{C_1}{C_1 + C_2} \tag{9}$$

Active CTLE can be implemented through a differential pair with RC degeneration with gain at Nyquist frequency as shown in Figure 7(b). At the high frequency, degeneration capacitor shorts the degeneration resistor and creates peaking. The peaking and DC gain can be tuned through adjustment of degeneration resistor and capacitor.

Pros

- Active CTLE provides gain and equalization with low power and area overhead.
- Cancel both precursor and long tail ISI

Cons

- Equalization is limited to 1st order compensation.
- Noise and cross are amplified
- Very sensitive to PVT and be hard to tune
- The speed is limited by gain bandwidth of the amplifier.

The transfer function of the active ctle is written as

$$H(s) = \frac{gm}{Cp} \frac{s + \frac{1}{RsCs}}{\left(s + \frac{1 + gmRs/2}{RsCs}\right)\left(s + \frac{1}{RdCp}\right)} \tag{10}$$

DC gain is expressed as

$$DC\ gain = \frac{gmR_D}{1 + gmR_s/2} \tag{11}$$

Ideal peak gain is equal to gm*R_D. Ideal peaking can be expressed as

$$Ideal\ peaking = \frac{Ideal\ peak\ gain}{DC\ gain} = 1 + gmR_s/2 \tag{12}$$

RX Decision Feedback Equalization (DFE)

Decision feedback equalizer is commonly implemented in high-speed links receiver-side. Slicer makes a symbol decision without amplifying noise. The results are fed back to the slicer input through an FIR filter to cancel post-cursor ISI. The major challenge in DFE implementation is the closing timing on the first tap feedback, which must be done in one bit period or one unit interval (UI).

Pros

- Boost high frequency content without noise and crosstalk amplification
- Tap coefficients can be adaptively tuned

Cons

- Due to the nature of feedback, pre-cursor ISI cannot be cancelled, but FFE can be used to complement the DFE equalization.
- If noise is large, chance for error propagation is high.
- Critical feedback timing path is less than one UI.
- CDR phase detection can be complicated due to the timing of ISI subtraction.

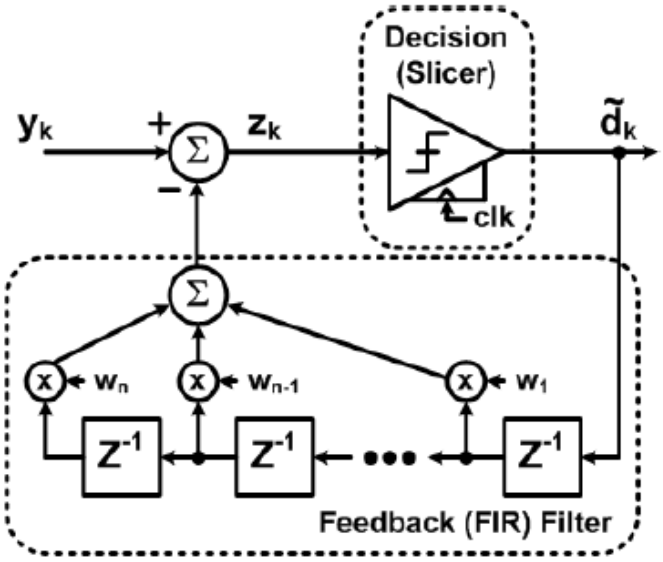


Figure 8 Receiver DFE equalization

Direct Feedback DFE Examples

6.25Gb/s 4-tap DFE from Texas Instrument **[2]** is shown in Figure 9. Amplifier A_1 works as the main tab of the equalizer which provides linear gain of the input. A2, A3, A4 and A5 are the feedback tabs, which equalizes ISI caused by the channel. All 5 tabs are summed into the resistor. The equalized signal is produced at RXEQ. The tap 1 is the most critical feedback path and it is shown in Figure 10. The comparator must make decision within ½ UI in order to meet the timing requirement of adaptive equalization tap values and CDR. CLK90/270 samples the RXEQ alternatively on top and bottom comparator. DFECLK shifts the sampled data into the proceeding latches and at the same time selects the DFE polarity based on the data sequence.

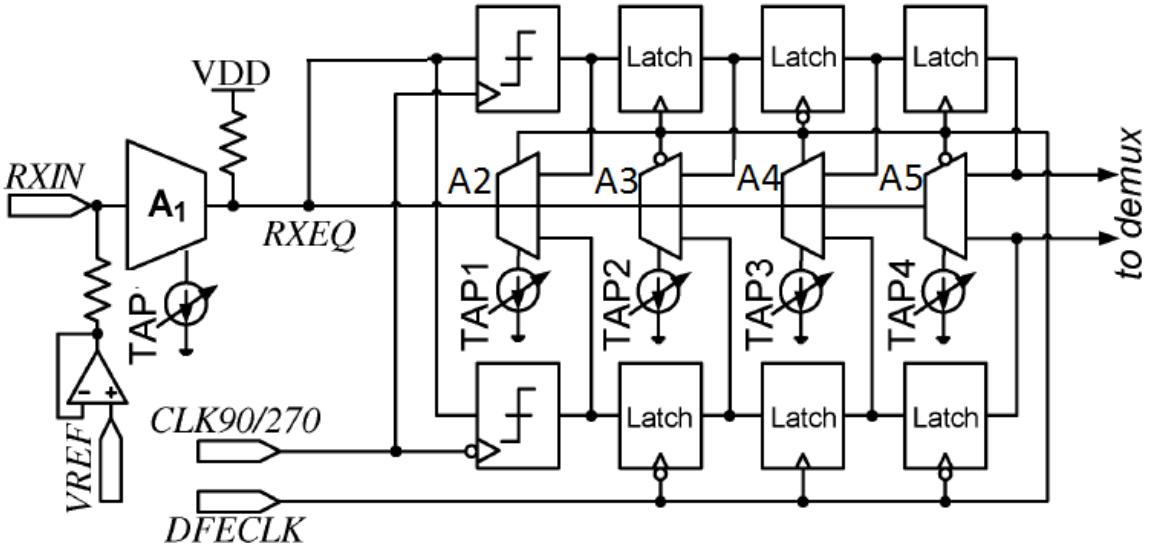


Figure 9 Direct Feedback DFE with Receiver analog front end (5-tap DFE for illustration)

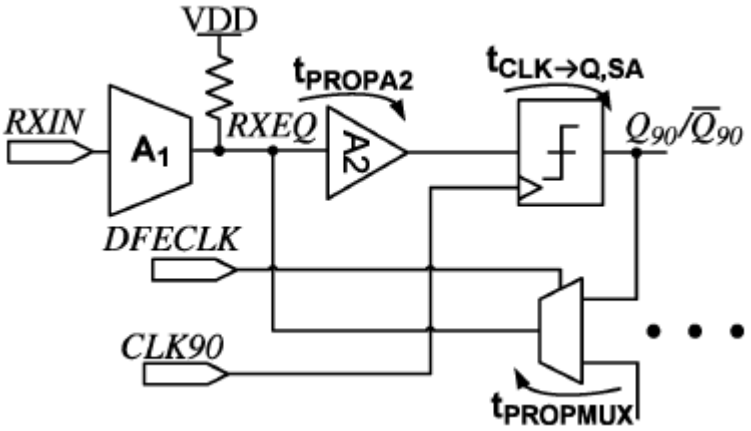
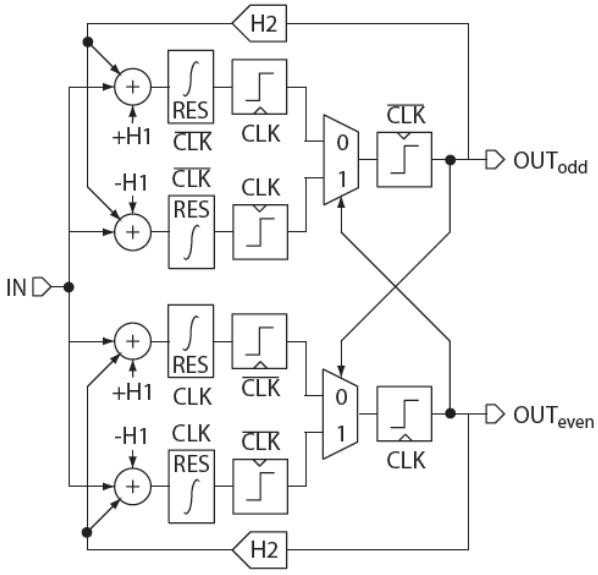


Figure 10 Schematic of the critical path of the direct feedback DFE

Half-rate DFE architecture with speculation technique is used in [3] to reduce the speed requirement on the slicer. ±H1 taps are speculated at the input of DFE summer instead of feeding back and subtracting ISI in 1UI. This method relaxes the design requirement than TI's direct feedback DFE.



Half-rate 2-tap DFE architecture with speculation.

Pre-Lab

1. Assuming a 3-tap TX FIR equalizer with the z domain transfer function as the following

$$W(z) = -0.101 + 0.645z^{-1} - 0.254z^{-2} \quad (13)$$

   Please find the low frequency response, Nyquist frequency response, and frequency peaking of this 3-tap TX FIR equalizer?

2. Please design a passive CTLE as shown in Figure 7(a) to realize the transfer function as shown in Figure 11 using R_1=500Ω and C_1=1pF. Please show your schematic.

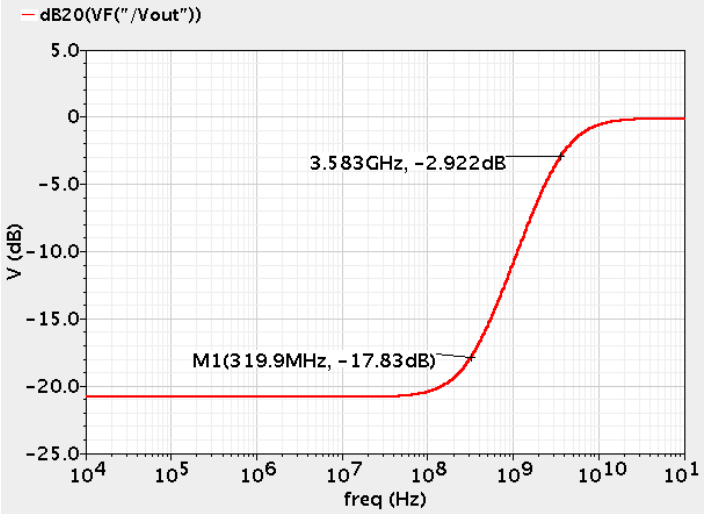


Figure 11 Passive CTLE Transfer Function

3. Please design a parallel PRBS generator and an error detector circuit with a testing circuit at 4Gb/s using ideal blocks. Using the test circuit, you should be able to inject error data pattern and observe the error signal. An example is shown in Figure 12. Please show the simulation results. You can re-use the blocks given by TA.

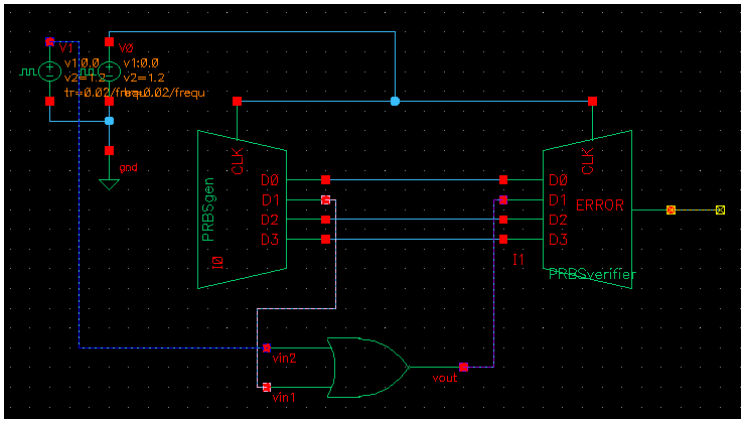


Figure 12 Parallel PRBS Testing Circuit

Questions

1. **TX FIR Equalization**. This problem investigates TX FIR equalization using the 12" Backplane channel "**peters_01_0605_B12_thru.s4p**" from course website. For parts (a) and (b), use the example matlab code "**channel_data_pulse_pda.m**" and produce the following 2 graphs:

   a) **Peak-Distortion Eye Height versus FIR tap number at 4, 8, and 16Gbps** (3 lines). For the tap numbers, use 1-tap (no equalization), 2-tap (1-post), 3-tap (1-pre and 1-post), and 4-tap (1-pre, 2-post). Don't restrict the TX equalizer resolution for this graph.

   b) **8Gb/s Peak-Distortion Eye Height versus Equalizer Resolution with 2, 3, and 4-tap equalization** (3-lines). For the tap resolution sweep, use 3, 4, 5, 6, and also include the infinite resolution data.

Note: The above matlab code also requires the "**tx_eq.m**" function. Also, this matlab code is only reference code. Feel free to modify and improve upon the code as you wish.

   c) **Design a 8Gb/s TX Driver with Equalization** [4]. Modify one of your drivers from lab3 to include FIR equalization.
      i. The maximum output voltage swing can be anywhere from 350mVppd (min.) to 1Vppd (max.). This gives you the flexibility to choose whichever driver you wish – from low-swing voltage-mode to current-mode.
      ii. Use the results from part (a) and (b) to justify your tap number and resolution.
      iii. **Include 2 8Gb/s PRBS eye diagrams** – one without equalization (all weight on cursor) and one with the proper equalization taps enabled. Import the s-parameter file into your Cadence simulation to produce the eye diagrams. Make sure the channel is properly terminated at both ends. Note, as you will have some additional driver capacitance, the equalization taps may change slightly.
      iv. The driver and at least one predriver stage should be full-transistor level design. The other blocks (PRBS, delay elements, etc) can be macromodeled.
      v. Report transmitter power consumption, power efficiency (mW/Gb/s), and 8Gb/s eye height and width.

2. **RX CTLE Equalization**. Design a 8Gb/s active CTLE to meet the following specifications:
   a) Min peak gain at Nyquist (4GHz) of 6dB
   b) Zero frequency tunable from a minimum range of 500MHz to 1GHz
   c) Minimum tunable peaking (magnitude difference between Nyquist and low frequency response) range of 12dB (Example: +6dB at 4GHz and -6dB at low frequency).
   d) Load capacitor = 25fF
      i. **Produce frequency response plots** showing the zero and peaking tenability.
      ii. **Produce a 8Gb/s PRBS eye diagram** with the 12" Backplane channel s-parameter channel output as the input to the CTLE. Optimize the CTLE settings for optimal eye opening.

iii. Report CTLE power, power efficiency (mW/Gb/s), and 8Gb/s eye height and width.

3. **RX DFE Equalization**. Design a 8Gb/s 2-tap DFE [2][3].
   a) Use one of the comparators you designed in Homework 5 in your design. Note, you will probably have to speed this design up – as you will need a 4GHz clock if you implement a ½ rate design.
   b) The only thing that has to be transistor level is the comparator. The rest of the blocks (summer, feedback taps, other logic) can be macromodeled. Note for the summer model, make sure to capture the RC settling if you use a linear resistive load summer. Feel free to investigate an integrating architecture if you prefer.
   c) **Produce a 8Gb/s PRBS eye diagram at the summer output** with the 12" Backplane channel s-parameter channel output as the input to the DFE. Optimize the DFE settings for optimal eye opening at the input of the comparator (summer output).
   d) Report DFE power, power efficiency (mW/Gb/s), and 8Gb/s eye height and width.
   e) Note, you will have to synchronize the DFE with the incoming data stream. A good way to do this is with an initial "lone pulse" input pattern. Adjust your comparator clock to sample near the peak of the lone pulse. Then simulate with the PRBS data.

Reference

[1] *Digital Systems Engineering*, W. Dally and J. Poulton, Cambridge University Press, 1998.

[2] R. Payne et al,"A 6.25-Gb/s Binary Transceiver in 0.13-um CMOS for Serial Data Transmission Across High Loss Legacy Backplane Channels," JSSC, vol. 40, no. 12, Dec. 2005, pp. 2646-2657

[3] M. Park, J. Bulzacchelli, and D. Friedman, "A 7 Gb/s 9.3 mW 2-tap current-integrating DFE receiver," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 230–231.

[4] J. F. Bulzacchelli, et al. "A 10-Gb/s 5-Tap DFE/4-Tap FFE Transceiver in 90-nm CMOS Technology", IEEE Journal of Solid-State Circuits, Vol. 41, No. 12, Dec. 2006, page 2885~2900.