A 22-Gb/s PAM-4 Receiver in 90-nm CMOS SOI Technology

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***Abstract*—We report a receiver for four-level pulse-amplitude modulated (PAM-4) encoded data signals, which was measured to receive data at 22 Gb/s with a bit error rate (BER) $< 10^{-12}$ at a maximum frequency deviation of 350 ppm and a 2^7-1 PRBS pattern. We propose a bit-sliced architecture for the data path, and a novel voltage shifting amplifier to introduce a programmable offset to the differential data signal. We present a novel method to characterize sampling latches and include them in the data path. A current-mode logic (CML) biasing scheme using programmable matched resistors limits the effect of process variations. The receiver also features a programmable signal termination, an analog equalizer and offset compensation for each sampling latch. The measured current consumption is 207 mA from a 1.1-V supply, and the active chip area is 0.12 mm^2.**

***Index Terms*—CML, CMOS, digital communication, latch, PAM-4, receiver, serial links, SOI.**

I. Introduction

SIGNALING over short distances—e.g., several centimeters on a multi-chip module (MCM) or between closely spaced single-chip modules (SCM) on a PCB board—is limited by the number of available IO pins. For a given band-limited channel, PAM-4 signaling [1]–[3] can be used to achieve higher data rates per pin at acceptable cost in chip area and power consumption.

The first PAM-4 receiver implementation for multigigabit communication in CMOS [1] achieved a data rate of 8 Gb/s in a 0.3-μm CMOS technology and using a 3-V supply. There, the design incorporates an analog fractionally spaced single-tap feed-forward equalizer in the receiver. The circuit in [2] targeted the use of PAM-4 signalling for backplane communication at a data rate of 5 Gb/s. In order to open the data eye the authors propose the use of a feed-forward equalizer (FFE) in the transmitter together with a coding scheme which avoids the largest transitions in the PAM-4 eye. The receiver circuit in [3] achieves a data rate of 10 Gb/s with a 0.13-μm CMOS technology. A combination of transmit equalization and decision feedback equalization (DFE) in the receiver is used to cope with channel attenuation and reflections.

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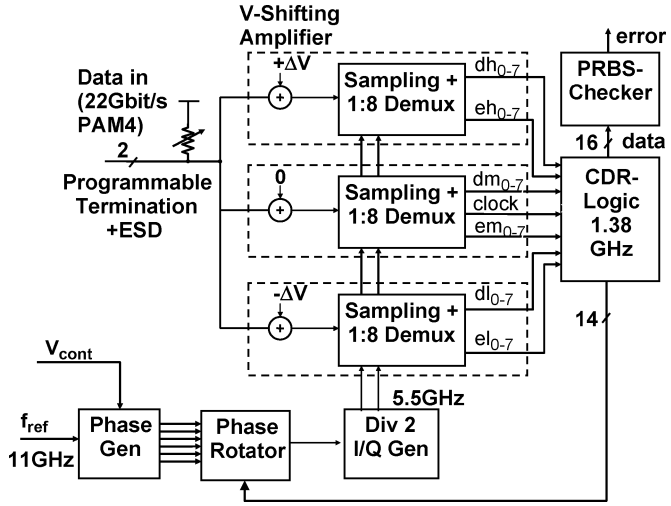

Fig. 1. Architecture of the PAM-4 receiver.

A PAM-4 transmitter at even higher data rates was demonstrated using a 90-nm CMOS technology [4]. The design of the analog receiver circuits with these technologies is becoming challenging, mostly due to the small supply voltages and available voltage margins. This receiver design benefits from several key features. First, we propose a novel voltage-shifting amplifier, which allows programmable equalization in the data path. The biasing concept applied in all current-mode logic (CML) stages uses adjustable unit resistor cells, which allows reducing the effect of process variations. A fast and supply-insensitive differential-to-CMOS clock converter allows a rapid transition from the CML to the full-swing CMOS clock domain. Also, since timing margins are very small, a fully differential CML-style clock path is implemented to achieve low jitter. A single phase rotator running at the baud rate, followed by an I/Q divider, provides low-jitter clocks with high accuracy.

II. Receiver Architecture

For the implementation of the proposed PAM-4 receiver, a bit-slice approach was taken as shown in Fig. 1. The differential data inputs *din* and *dinb* are terminated to the supply via programmable termination resistors. Three identical demux slices sample the input data, one for each vertical offset voltage, as shown in Fig. 2. Each demux slice consists of a voltage shifting amplifier, two 1:4 demuxes (one for the data and one for the edge samples), and two 4:8 demuxes. Due to this architecture

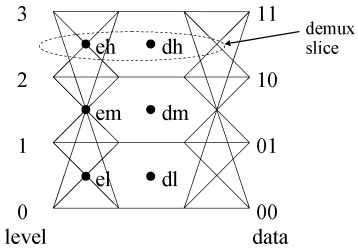

Fig. 2. PAM-4 eye diagram and the required sampling points.

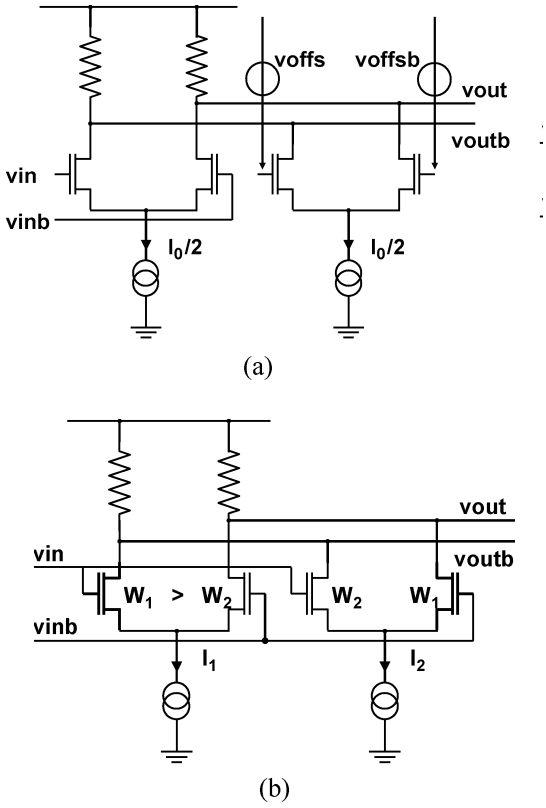

Fig. 3. Existing solutions for voltage shifting amplifiers.

the voltage shifting operation can be shared by both the data and edge bit samplers. The three demux slices receive two half-rate (5.5 GHz) differential clock phases I and Q, where the I and Q phases are used for the edge and data samples, respectively. Synchronization signals originating in the middle slice are shared by the blocks to avoid phase ambiguity in the locally divided clocks of the three slices. A phase rotator, running at symbol rate (11 GHz) provides a programmable phase shift for the clock signal, which is fed to a divide-by-2 prescaler to generate the quadrature clock phases. The phase rotator requires six clock phases, which are generated in a voltage-controlled delay line.

Each demux slice delivers eight data bits and eight edge bits at its output. Hence, a total number of 3×16 bits is fed to a digital logic block, which is running at 1/8 of the symbol rate. The data is first decoded according to the bit assignment of Fig. 2, where a binary enumeration of the levels is used for simplicity. The decoded data is fed to a pseudo-random bit sequence (PRBS) checker, which outputs a combined error signal for eight symbols. The sampled edge and data bits enter the clock and data recovery (CDR) unit which controls the phase rotator.

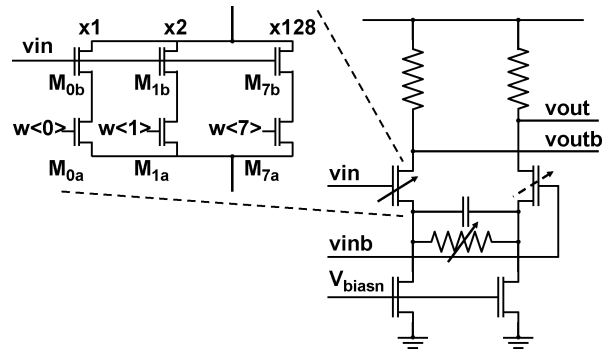

Fig. 4. Schematic of the proposed voltage shifting amplifier.

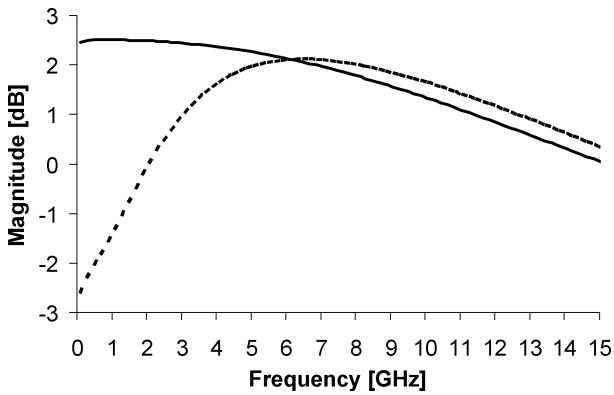

Fig. 5. Transfer function of the voltage shifting amplifier without (solid) and with (dashed) capacitive source degeneration.

III. Circuit Implementation

A. Receiver Front-End

The differential data signal passes two differential amplifier stages before it is sampled in the latches of the receiver front-end. The first stage is a voltage shifting amplifier, which is used to add a programmable offset voltage. It also provides equalization by capacitive source degeneration [5], which can be switched either on or off to adapt for different channel transfer functions. In order to achieve acceptable common-mode and supply-noise rejection and to cope with the small supply voltage and high bandwidth requirements we propose a novel topology. The second amplification stage also features programmable equalization and in addition provides offset correction for the sampling latches. Each of the 3×4 latches is fed by a separate amplification stage.

The requirements on the voltage shifting amplifier are the following. Besides providing the necessary voltage shift, gain and bandwidth, it should also offer programmable equalization with a transfer function independent of the setting of the offset voltage, as well as acceptable supply and common-mode voltage rejection. Fig. 3 displays previously used topologies.

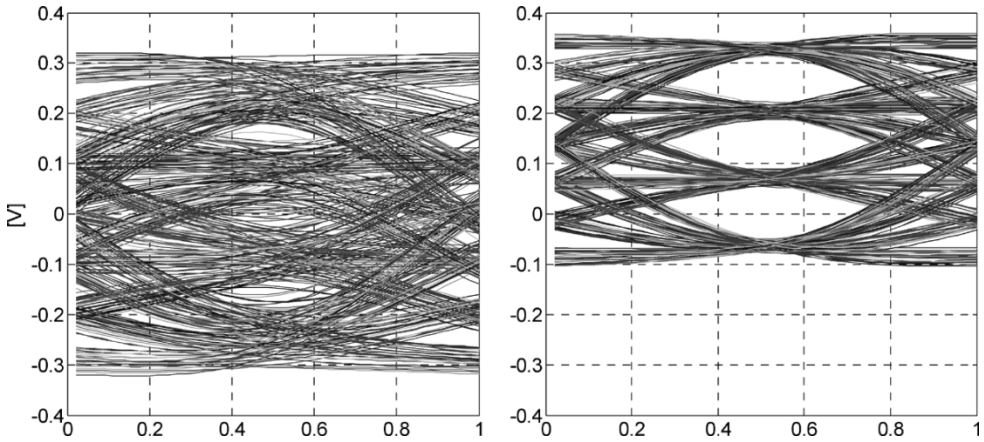

Fig. 6. Combined effect of voltage shift and equalization. Eye diagram at the input (left) and output (right) of the amplifier.

The circuit in Fig. 3(a) is a double differential stage, which sums the input voltage and a constant offset voltage generated in a voltage DAC. The circuit in Fig. 3(b) is a double-mismatched differential pair [6], [7]. Here, the voltage offset is controlled by changing the ratio of the bias currents.

While the structure in Fig. 3(a) has excellent common-mode and supply-noise rejection, it displays lower DC gain since only half the current is used in the input transistors. Also, its bandwidth is lower since the second differential pair adds capacitance to the output node. Additionally, the voltage DACs require a large chip area. Fig. 4 depicts the proposed voltage shifting amplifier. It is based on the principle that the effective width of the transistor in the differential stage can be programmed by a digital value. While transistors $\mathrm{M_{0b}}$ to $\mathrm{M_{7b}}$ are connected to the input voltage, transistors $\mathrm{M_{0a}}$ to $\mathrm{M_{7a}}$ act as switches, controlled by binary weights w<0:7>. Hence, the circuit consisting of $\mathrm{M_{0a,b}}$ to $\mathrm{M_{7a,b}}$ can be regarded as a single transistor where the effective width can be adjusted. In the opposite branch on the right side of Fig. 4 all transistors are always switched on. The proposed circuit has similar gain, bandwidth and common-mode rejection as the topology in Fig. 3(b). In contrast to this topology, however, the proposed structure can be easily combined with capacitive source degeneration to extend the bandwidth of the amplifier or to provide equalization. This is due to the fact that in the proposed circuit the zero generated by the source degeneration is independent of the applied voltage shift.

The difference in the effective transistor size leads to a programmable voltage offset ΔV, which—neglecting to first order the influence of the source degeneration resistors—is approximately given by

$$\Delta V = (V_{gs} - V_t)\left[\sqrt{\frac{w_{\max}}{w_x}} - 1\right] \tag{1}$$

where $V_{gs} - V_t$ is the gate overdrive of the maximum width transistor, $w_{\max}$ is the maximum gate width (all sub-transistors switched on), and w_x is the programmed gate width.

Fig. 5 displays the transfer function of the voltage shifting amplifier. The solid curve corresponds to the case without capacitive source degeneration, while the dashed curve represents the case when the amplifier is used in equalization mode. Fig. 6 displays simulated waveforms at the input and the output of the amplifier for the case of 200-mV voltage offset. For the simulation, the channel was described by measured S-parameter data of an 8-inch FR-4 board, together with 500 fF of load capacitance at the termination on both the transmit and receive side. Also, light transmit equalization with FFE coefficients [−0.02 0.9−0.05−0.03] was applied on the transmit side.

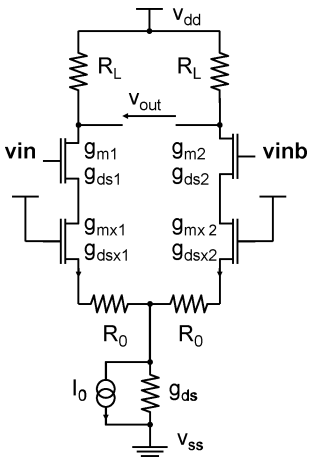

Fig. 7. Schematic used to derive small-signal gains.

Since the amplifier is an asymmetric circuit, its response to changes in the supply and common-mode voltages has to be carefully analyzed. Referencing Fig. 7, the common-mode gain, differential gain, gain with respect to vdd, and ground, defined as

$$A_{cc} = \frac{vout}{(vin + vinb)/2} \tag{2}$$

$$A_{dd} = \frac{vout}{(vin - vinb)} \tag{3}$$

$$A_{vdd} = \frac{vout}{\Delta vdd} \tag{4}$$

$$A_{vss} = \frac{vout}{\Delta vss} \tag{5}$$

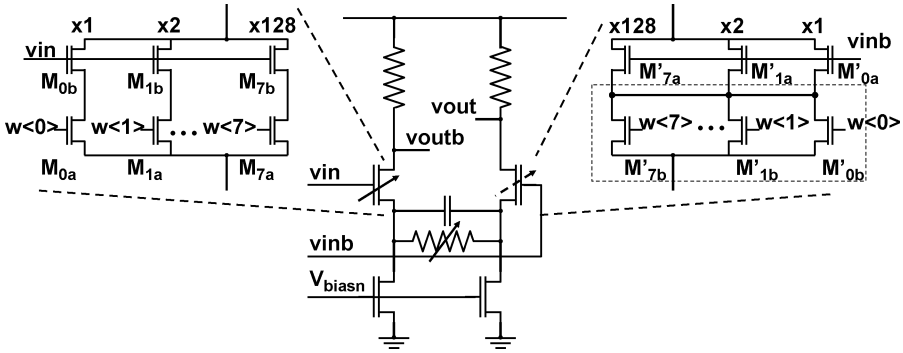

Fig. 8. Voltage shifting amplifier with improved common-mode rejection.

respectively, are given by

$$A_{cc} = \frac{R_L}{R_D}\left[2(\gamma_1-\gamma_2)+g_{ds}\left[R_L(\gamma_1-\gamma_2)+(\gamma_1 R_{d2}-\gamma_2 R_{d1})\right] +2\left[\gamma_1(1+\gamma_2)\xi_2-\gamma_2(1+\gamma_1)\xi_1\right]\right] \quad (6)$$

$$A_{dd} = \frac{R_L}{R_D}\left[\gamma_1(1+\gamma_2)(1+\xi_2)+\gamma_2(1+\gamma_1)(1+\xi_1) +\left(\frac{g_{ds}}{2}\right)\left[\gamma_1(R_L+R_{d2})+\gamma_2(R_L+R_{d1})\right]\right] \quad (7)$$

$$A_{vdd} = \frac{R_L}{R_D}\left[2(\gamma_1-\gamma_2)+g_{ds}\left[\xi_2(1+\gamma_2)(R_L+R_{d1}) -\xi_1(1+\gamma_1)(R_L+R_{d2})\right] +2\left[\gamma_1(1+\gamma_2)\xi_2-\gamma_2(1+\gamma_1)\xi_1\right]\right] \quad (8)$$

$$A_{vss} = \frac{R_L}{R_D}\left[g_{ds}\left[(1+\gamma_1+\xi_1+\gamma_1\xi_1)(R_L+R_{d2}) -(1+\gamma_2+\xi_2+\gamma_2\xi_2)(R_L+R_{d1})\right]\right] \quad (9)$$

where $\gamma_1 = g_{m1}/g_{ds1}$, $\gamma_2 = g_{m2}/g_{ds2}$, $\xi_1 = g_{mx1}/g_{dsx1}$, $\xi_2 = g_{mx2}/g_{dsx2}$, and

$$R_D = (R_L+R_{d1})(1+\gamma_2+\xi_2+\gamma_2\xi_2) +(R_L+R_{d2})(1+\gamma_1+\xi_1+\gamma_1\xi_1) +g_{ds}(R_L+R_{d1})(R_L+R_{d2}) \quad (10)$$

$$\frac{1}{R_{d1}} = \frac{g_{ds1}}{1+(g_{m1}+g_{ds1})\left[\left(R_0+\frac{1}{g_{dsx1}}\right)+\frac{R_0 g_{mx1}}{g_{dsx1}}\right]} \quad (11)$$

$$\frac{1}{R_{d2}} = \frac{g_{ds2}}{1+(g_{m1}+g_{ds2})\left[\left(R_0+\frac{1}{g_{dsx2}}\right)+\frac{R_0 g_{mx2}}{g_{dsx2}}\right]}. \quad (12)$$

Since the input signals are referenced to V_{dd} it is most important to guarantee sufficient immunity to supply noise on the ground node. The power supply rejection with respect to ground A_{dd}/A_{vss} is thus given by (13), shown at the bottom of the page, which is 20 dB in the current design for 200 mV of voltage shift. The common-mode rejection A_{dd}/A_{cc} results in (14), shown at the bottom of the page. In the present implementation, the common-mode rejection of the current implementation is 14 dB, which might be too low for a link where the common-mode level is modulated for back channel communication. The common-mode rejection can however be improved by 10 dB by matching the on-resistances of the switches in the variable width transistor, as shown in Fig. 8. Here, the combined series resistance of the switch transistors $\mathrm{M_{0a}}$–$\mathrm{M_{7a}}$ in the left branch matches the combined series resistance of $\mathrm{M'_{0a}}$–$\mathrm{M'_{7a}}$ in the right branch. Since this results in a more balanced configuration ($\xi_1 = \xi_2$), the contribution of the third term in the denominator of (14) is minimized.

There exists one voltage shifting amplifier per slice, which feeds its output voltage into four second amplifiers, one for each of the 2×2 half-rate edge and data sampling latches per slice. The second amplification stage, displayed in Fig. 9, provides additional amplification and equalization, and also allows compensating the offsets of the individual sampling latches. This is

$$\mathrm{SNRG} = \frac{\gamma_1(1+\gamma_2)(1+\xi_2)+\gamma_2(1+\gamma_1)(1+\xi_1)+\left(\frac{g_{ds}}{2}\right)\left[\gamma_1(R_L+R_{d2})+\gamma_2(R_L+R_{d1})\right]}{g_{ds}\left[(1+\gamma_1+\xi_1+\gamma_1\xi_1)(R_L+R_{d2})-(1+\gamma_2+\xi_2+\gamma_2\xi_2)(R_L+R_{d1})\right]} \quad (13)$$

$$\mathrm{CMRR} = \frac{\gamma_1(1+\gamma_2)(1+\xi_2)+\gamma_2(1+\gamma_1)(1+\xi_1)+\left(\frac{g_{ds}}{2}\right)\left[\gamma_1(R_L+R_{d2})+\gamma_2(R_L+R_{d1})\right]}{2(\gamma_1-\gamma_2)+g_{ds}\left[R_L(\gamma_1-\gamma_2)+(\gamma_1 R_{d2}-\gamma_2 R_{d1})\right]+2\left[\gamma_1(1+\gamma_2)\xi_2-\gamma_2(1+\gamma_1)\xi_1\right]} \quad (14)$$

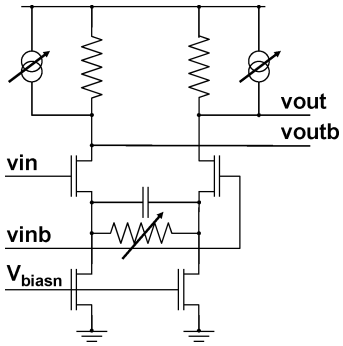

Fig. 9. Schematic of the second amplification stage providing per-latch offset compensation.

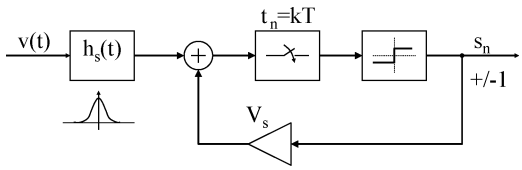

Fig. 10. Proposed sampling latch model.

achieved by adding small currents into one of the differential branches. The resolution of the offset compensation is 3 + 1 sign bit, which covers a range of ±25 mV.

B. Sampling Latch Characterization

The sampling latch marks the interface between the analog and digital domains. It functions as a regenerative amplifier, which samples the input signal at a certain time instant and then decides if the voltage at its input is below or above a threshold voltage. For digital applications, latches are usually described by their setup and hold times together with the latch delay. For the case of a sampling latch for analog applications, such as serial link receivers, latches are characterized by their sensitivity and bandwidth.

In order to be able to include the latch characteristic in the transfer function of the data path and to accurately compare different latch types we propose to characterize latches by the model shown in Fig. 10. In the proposed model, the latch is divided into a linear front-end, which is described by a latch sensitivity function $h_s(t)$, followed by an ideal sampler and binary slicer. The symbol after the slicer s_n, multiplied by a voltage factor V_s, is fed back and shifts the threshold of the slicer. The voltage V_s is equivalent to the latch sensitivity for DC input signals. The sensitivity function $h_s(t)$, which is normalized such that

$$\int_{T_1}^{T_2} h_s(\tau)d\tau = 1 \tag{15}$$

defines the time resolution of the latch. T_1 and T_2 mark the limits of the sensitivity window. The normalized latch transfer function $H_{s,n}(\omega)$ can then be derived by taking the Fourier transform of $h_s(t)$.

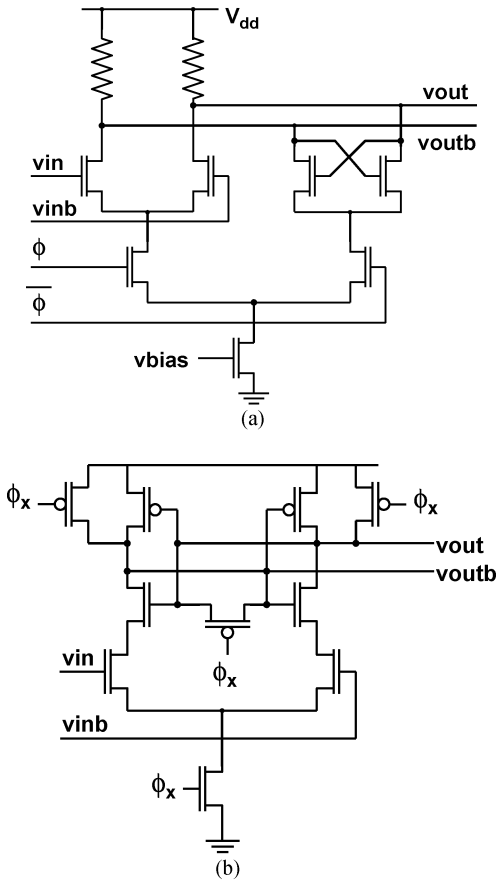

Fig. 11. Comparison of (a) CML-sampling latch and (b) SenseAmp-style latch for analog sampling.

The input signal $v(t)$ is folded with $h_s(t)$ before being sampled at $t = kT$. The latch flips if

$$\int_{T_1}^{T_2} v(\tau)h_s(\tau)d\tau > V_s \tag{16}$$

A measurement procedure to derive $h_s(t)$ from simulations is given in the Appendix. Using this procedure, the latch sensitivity function $h_s(t)$ and its DC sensitivity V_s was extracted for the two choices of sampling latches shown in Fig. 11, a CML-type latch and a SenseAmp latch [8]. For a fair comparison, the entire CML data path was included in the simulation, which consists of two CML latches followed by a SenseAmp latch, as shown in Fig. 12. A clock rise time of 30 ps was assumed in both cases.

The latch sensitivity function for the two cases is displayed in Fig. 13(a). Interestingly, the sensitivity window of the SenseAmp latch is smaller than in the CML case, indicating superior time resolution capability. The resulting DC sensitivities, however, are 2.6 mV for the CML case and 8.2 mV for the SenseAmp case, which is equivalent to $20 * \log 10(8.2/2.6) = 10$ dB more gain in the signal path for the CML case. Defining a target sensitivity value $V_{s,\text{target}}$ allows to derive a latch transfer function $H_s(\omega) = H_{s,n}(\omega)(V_{s,\text{target}}/V_s)$, which combines gain and

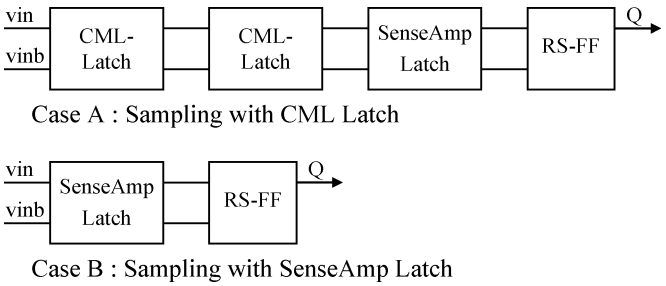

Fig. 12. Data paths for latch comparison.

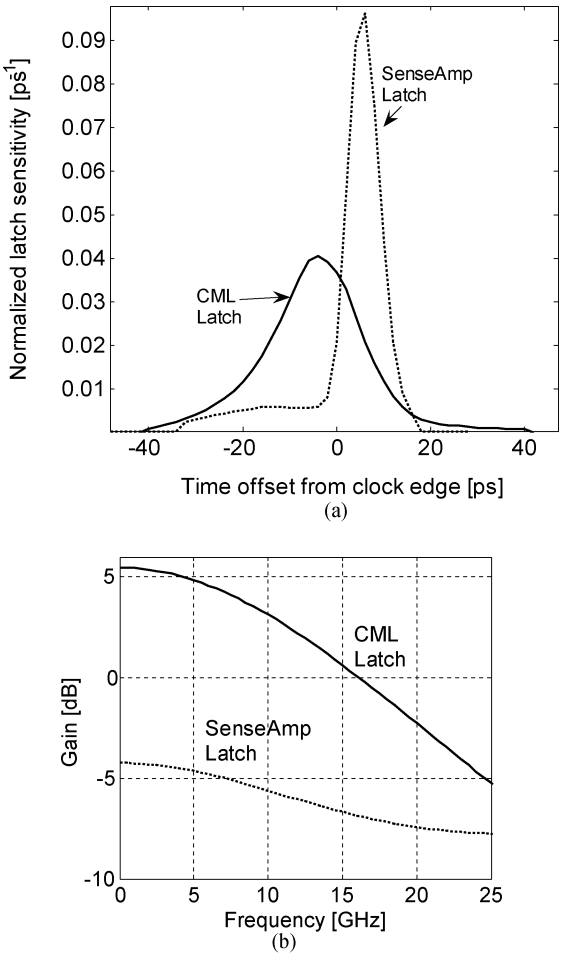

Fig. 13. (a) Latch sensitivity function for CML latch (solid) and SenseAmp latch (dotted). (b) Latch transfer function for CML latch (solid) and SenseAmp latch (dotted) at a target sensitivity of 5 mV.

frequency dependence of the latch in a single function, and can thus be included in simulations of the entire signal path. Fig. 13(b) compares $H_s(\omega)$ for a target sensitivity of 5 mV. It can be seen that the bandwidth of the SenseAmp latch is 14 GHz, while the bandwidth of the CML latch amounts to 10 GHz, albeit at higher equivalent gain.

Although SenseAmp latches provide high input bandwidth and consume far less power (200 μA) than the CML configuration ($\sim$2 mA), CML latches are used in the data path of the PAM-4 receiver because of their superior sensitivity and higher immunity to power supply variations.

C. Demux

Fig. 14 displays the sampling and 1:4 demultiplexing unit for one bit slice. The signal from the voltage shifting amplifier is distributed to the second amplification stage, which also provides the offset correction for the subsequent latches. The CML latches are clocked by the half-rate (5.5 GHz) differential clocks $\phi_{2i}/\overline{\phi}_{2i}$ and $\phi_{2q}/\overline{\phi}_{2q}$ for the edge and data samples, respectively. The output data is then converted to full-swing CMOS levels by the subsequent SenseAmp latches (denoted SAL). By running the SenseAmp latches also at half the baud rate, the 2:4 demultiplexing step can be implemented with standard latches from the digital library (denoted FF in Fig. 14), thus saving power and reducing latency when compared to a solution with another stage of CML-latches. This requires, however, that the clock generator derives the full-swing CMOS clocks ϕ_{2ix} and ϕ_{2qx} from the differential CML clocks ϕ_{2i} and ϕ_{2q} at 5.5 GHz with accurately defined timing, even in the presence of power-supply variations. The differential to full-swing converter, shown in Fig. 15, consists of a differential amplifier, which boosts the signal swing, followed by capacitively coupled inverters [9]. Using this structure, the simulated timing deviation in the worst case process corner for a 100-mV and 100-MHz square-wave power supply variation is $\pm$12 ps. The four edge samples e_0–e_3 and data samples d_0–d_3 are further de-multiplexed to octal rate in a subsequent stage not shown in the figure.

D. CML Biasing Concept With Variable Resistor

The bias generator for the CML stages in the demux (clock buffers, amplifiers, latches) is shown in Fig. 16. The common-mode voltage drop over the load resistor is regulated via an OpAmp to $0.3 \times V_{dd}$. Since bandwidth and power consumption of all CML stages linearly depend on the value of the load resistor, all resistors in the CML stages (and also the bias generator) were replaced by adjustable unit load resistors. This offers the possibility to adjust the resistor value in two steps (either high or low resistance) after fabrication, making the design less dependent on process variations of the resistor.

The value of the resistance R is specified to deviate from its nominal value R_0 due to chip-wide variations of manufacturing tolerance parameters T_m on the one hand, and nonmatching variations and changes in temperature T_{nmat} on the other hand. Hence, its actual value is given by

$$R = R_0(1+\alpha)(1+\beta) \tag{17}$$

with $|\alpha| \leq T_m, |\beta| \leq T_{nmat}$.

The resistance in the CML stages can be switched by shunting R with an auxiliary resistance R_p. Hence, when the shunt resistor is applied, the load resistance becomes

$$R = k_r R_0(1+\alpha)(1+\beta) \tag{18}$$

with resistance reduction factor $k_r = (R_0 \| R_p)/R_0$. Since the receiver should not be disturbed by switching values during operation, the shunt path is either switched on or off only at startup.

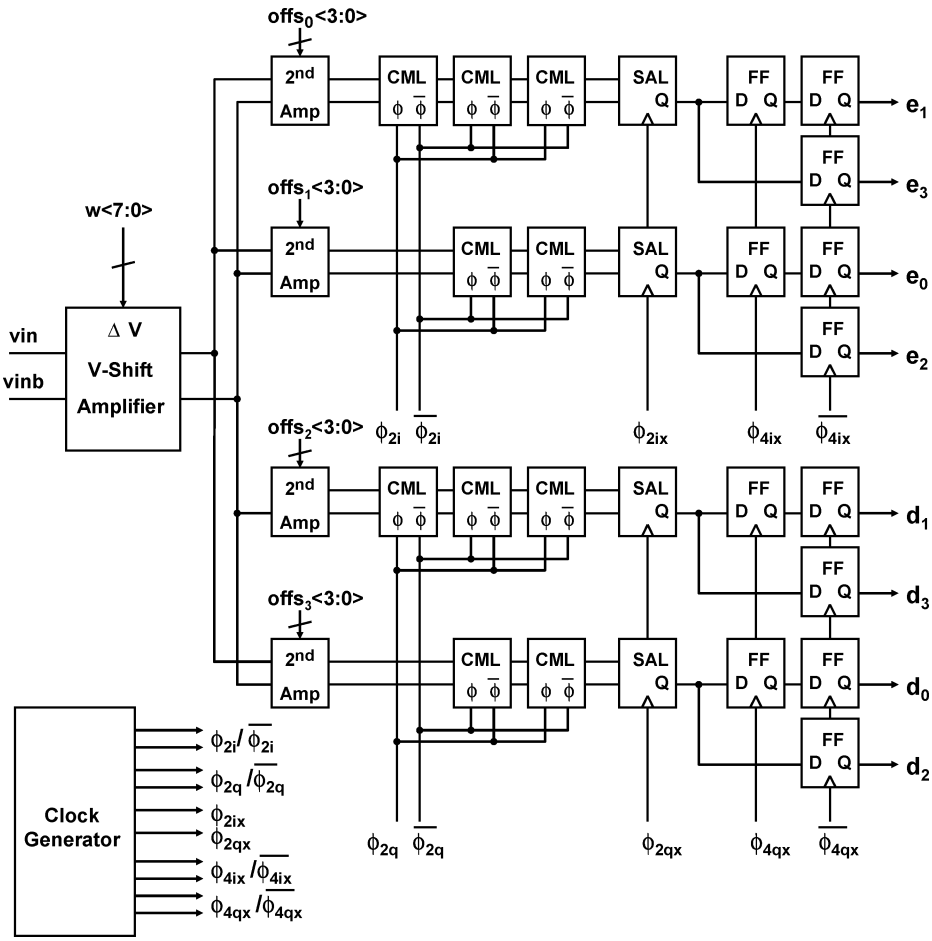

Fig. 14. Architecture of the 1:4 demux slice.

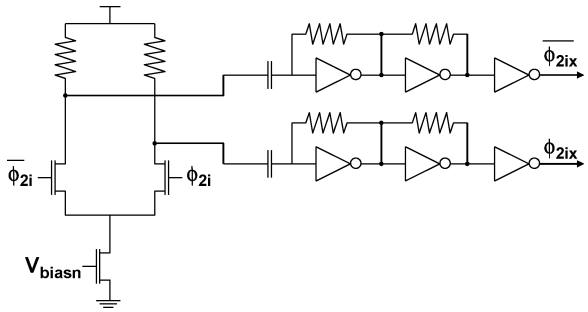

Fig. 15. Differential to single-ended converter.

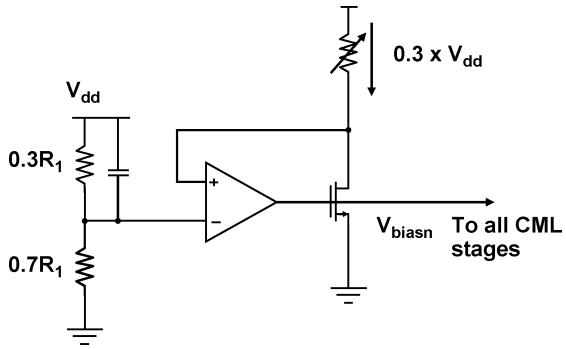

Fig. 16. Biasing concept with variable resistor.

Hence, the circuit has to be designed to take full account of the nonmatching and temperature variations. On the other hand, by choosing one of the two ranges, the influence of the manufacturing tolerance T_m can be approximately halved. The actual value of the manufacturing tolerance α can be determined after production, and compared to a threshold α_T, which defines if the upper or lower resistive range should be used. This defines two intervals $I_{p,\mathrm{off}}$ and $I_{p,\mathrm{on}}$ of resistance values for the two cases:

$$I_{p,\mathrm{off}} = [R_0(1-T_m)(1-T_{nmat}) < R < R_0(1+\alpha_T)(1+T_{nmat})] \quad (19)$$

$$I_{p,\mathrm{on}} = [k_r R_0(1+\alpha_T)(1-T_{nmat}) < R < k_r R_0(1+T_M)(1+T_{nmat})] \quad (20)$$

In order to derive the optimum values of α_T and k_r we note that in this case the lower and upper boundaries of the two intervals should be identical. Solving for α_T and $\mathrm{k_r}$ results in

$$k_{r,\mathrm{opt}} = \sqrt{\frac{1-T_m}{1+T_m}} \quad (21)$$

$$\alpha_{T,\mathrm{opt}} = \frac{1-T_m-k_{r,\mathrm{opt}}}{k_{r,\mathrm{opt}}}. \quad (22)$$

For $T_{\mathrm{m}} = 20\%$ and $T_{nmat} = 10\%$, this results in $k_{r,\mathrm{opt}} = 0.82$ and $\alpha_{T,\mathrm{opt}} = -0.02$. In this case, the overall tolerance is reduced from 30% to 19.9%.

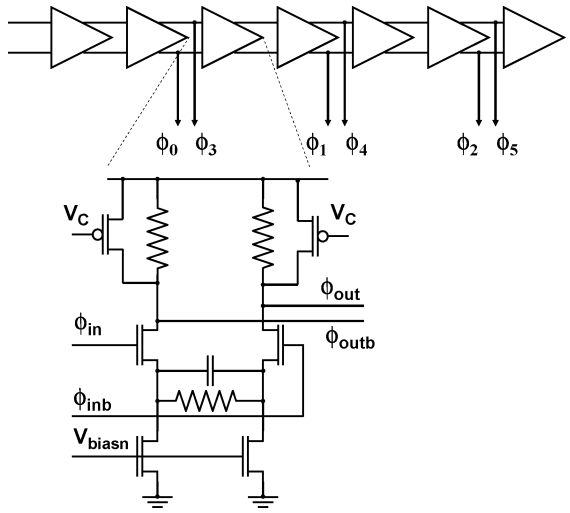

Fig. 17. Delay line with capacitive source degeneration.

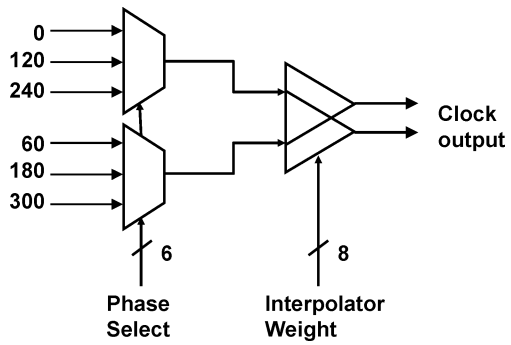

Fig. 18. Phase rotator implementation.

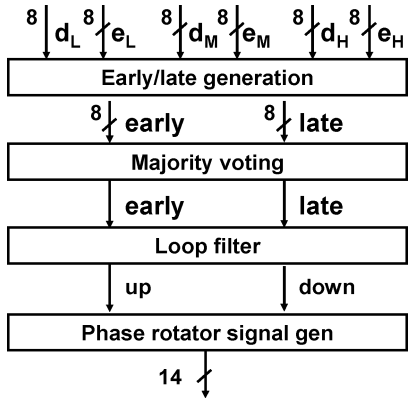

Fig. 19. Data flow in the digital CDR logic.

E. Delay Line and Phase Rotator

In order to guarantee a precise timing relationship between the quadrature clocks delivered to the sampling front-end, a single phase rotator is used, running at the baud rate (11 GHz). Precise half-rate clocks are then generated in the I/Q generator/divider after the phase rotator. Six clock phases, which are generated by the voltage-controlled delay line shown in Fig. 17, are fed to the phase rotator. A resistor is used in parallel to the tunable pMOS devices in order to speed up the circuit.

The phase rotator, shown in Fig. 18, consists of a phase selection stage followed by a phase interpolation stage [10]. All stages use a fully differential CML-style circuit topology. The first stage selects two clock phases from two adjacent phase sextants. Using six clock phases provides a good compromise between complexity and phase linearity. The phase interpolator, which blends the two selected phases, is controlled by an 8-bit thermometer-coded value. Hence, a total number of 48 phase steps are provided, resulting in a nominal timing resolution of 1.9 ps.

F. CDR Logic

The CDR logic is displayed in Fig. 19. In order to derive the edge information, all minor transitions (0–1, 1–2, 2–3) and the major transition (0–3) are used. It can be verified from Fig. 2 that the crossing point for these transitions are identical to the midpoint of the data samples.

The CDR logic is running at 1/8 of the baud rate (1.375 GHz). It receives 3×16 data and edge bits from the three analog slices, In a first step, the data and edge bits are transformed into an early and late vector, each of 8-bit length. Secondly, majority voting is applied in groups of four bits. The resulting early and late vectors, each two bits long, are then combined in a second level majority voting step to arrive at a single bit early or late information. This information is the input to a digital loop filter, which then decides if the value of the phase should be increased, decreased or left constant. A phase rotator signal generator encodes the 14 control signals used in the phase rotator.

IV. Measurement Results

The circuit has been fabricated in a 90-nm partially depleted digital CMOS SOI technology [11]. The test chip also contains a shift register to provide digital settings, and two inverter-based output buffers. An internal multiplexer allows to select the recovered clock, the undecoded latch outputs, the demultiplexed data signals, or derived signals, such as the bit error indicator, to be sent to the two output drivers.

The circuit was tested on-wafer with power-ground-signal-ground-signal-ground-power (P-G-S-G-S-G-P) probes. Fig. 20 displays the resulting offset versus the programmed value of the voltage-shifting amplifier. For a voltage offset of 200 mV, one bit corresponds to approximately 4 mV. The measured offset voltage for latch offset compensation versus programmed value is shown in Fig. 21.

For jitter tolerance tests, the input data was generated by an Anritsu 1775A four-channel bit pattern generator, where 4 channels were resisitively combined in order to generate a differential PAM-4 signal. The input eye as measured at the generator output for the 2^7-1 PRBS is depicted in Fig. 22. Although the overall differential eye amplitude is 650 mV p-p, the effective differential eye opening is about 95 mV vertically and 35 ps horizontally.

No special precoding was applied, so transitions between all PAM-4 levels are present. The output of the bit error signal was monitored in order to count the detected bit errors. For this test, the offset value for the voltage-shifting amplifier was set to 215 mV. The corresponding binary value w<0:7> was derived

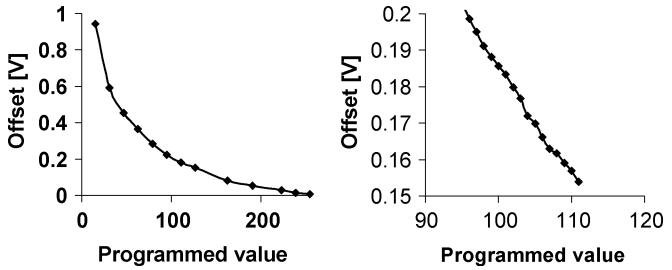

Fig. 20. Measured offset voltage versus programmed value of the V-shifting amplifier. Global characteristic (left) and detail (right).

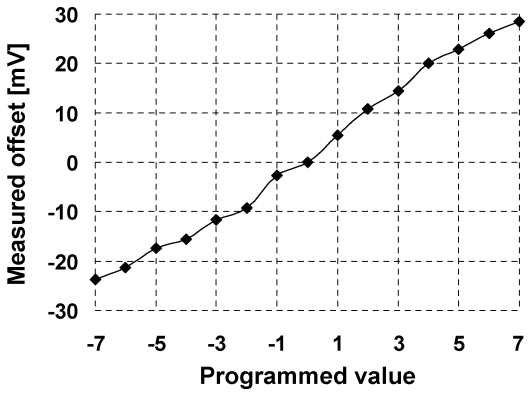

Fig. 21. Measured latch offset compensation capability.

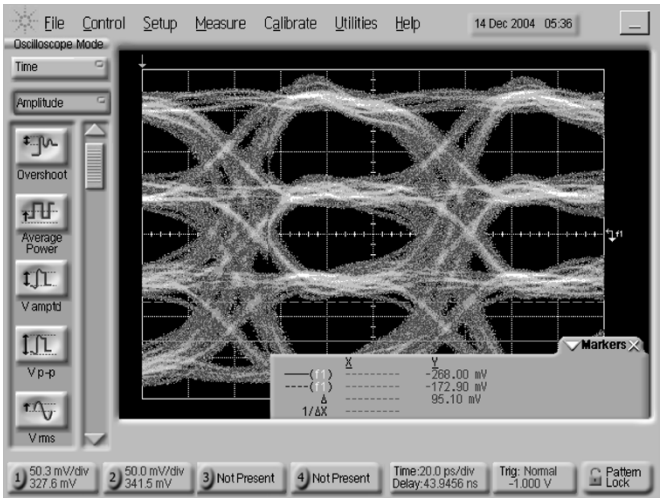

Fig. 22. PAM-4 eye diagram of the input data.

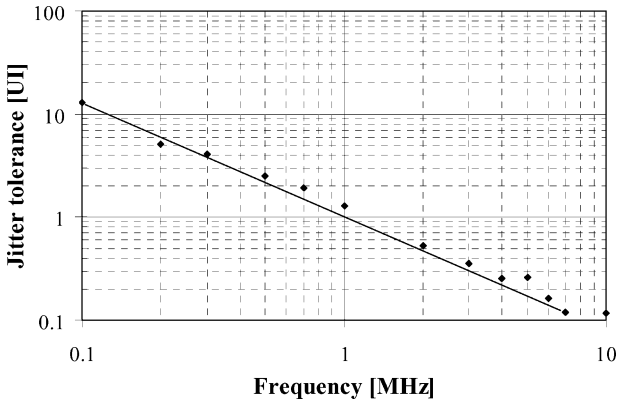

Fig. 23. Jitter tolerance at BER $= 10^{-12}$.

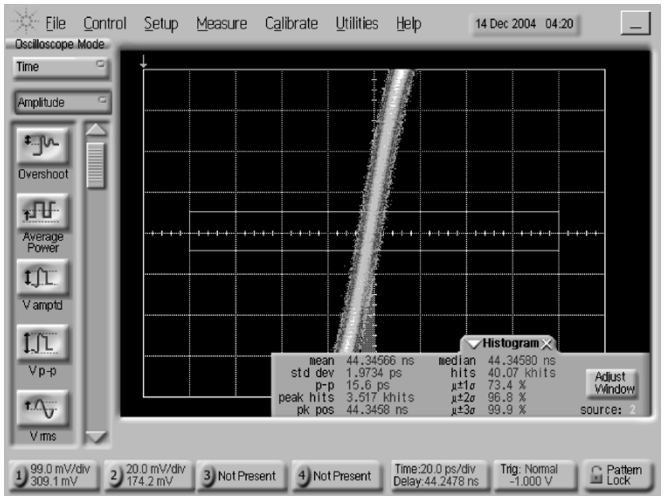

Fig. 24. Recovered clock from input data with 350 ppm frequency offset between data and receiver clock.

TABLE I
MEASURED JITTER UNDER DIFFERENT CONDITIONS

	RMS Jitter [ps]	P-P Jitter [ps]
Fixed clock	1.44	12.0
CDR on	1.64	13.3
Δf=350ppm	1.97	15.6
1 MHz 1 UI jitter	3.95	24.0

from the previous measurement of the offset voltage characteristic.

For the per-latch offset adjustment, the pattern generator was switched off. Then, for each of the 12 sampling latches, an automatic adaptation procedure was performed. The on-chip output multiplexer was programmed in order to monitor the unencoded output of a specific sampling latch. This output was fed on an oscilloscope, which was read out via a GPIB bus connected to a controlling PC. The digital latch offset value was then increased or decreased until the latch flipped.

Fig. 23 displays the measured jitter tolerance curve for a bit error rate (BER) of 10^{-12}. At the same error rate, the maximum acceptable frequency offset was measured to be 350 ppm.

Fig. 24 depicts the recovered 1/8 rate clock at a 350 ppm frequency offset. Jitter of the recovered clock under different stress conditions was measured with an Agilent 86100 scope, which is summarized in Table I. Fig. 25 depicts the demultiplexed output data.

The measured current consumption is 207 mA from a 1.1-V supply, which corresponds to a power consumption of 10.4 mW/Gb/s. Of the total current, 190 mA are consumed in the analog part, and 17 mA in the digital sections (4:8 demux, CDR logic, PRBS checker). The high-speed data input is protected with ESD diodes. Fig. 26 displays the layout of the test chip. The overall size of the chip is 1 mm^2, of which the active

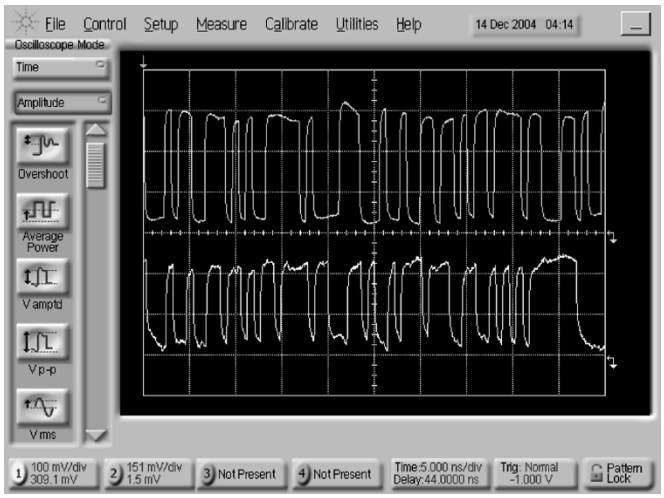

Fig. 25. Demultiplexed output data.

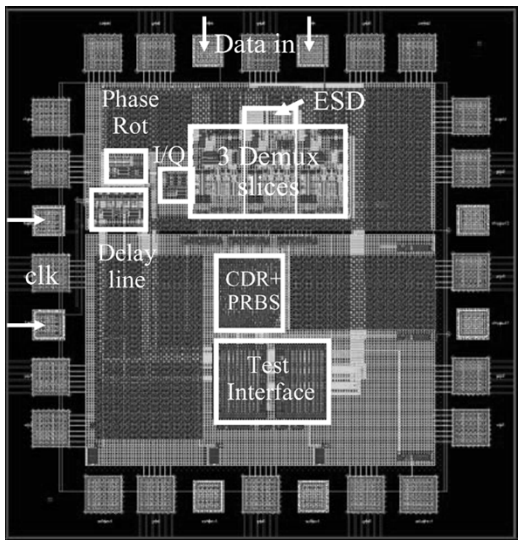

Fig. 26. Layout of the PAM-4 receiver.

components (including 0.03 mm^2 of debugging logic) occupy an area of 0.12 mm^2.

V. Conclusion

In this paper, we presented the architecture and the implementation of a PAM-4 receiver in 90-nm CMOS-SOI technology, capable of performing clock and data recovery at a data rate of 22 Gb/s.

We proposed a bit-slice architecture for the data path, where the voltage-shifter is shared by both the data and the edge sampling latches. A novel topology for a voltage shifting amplifier achieves the necessary high bandwidth and gain with acceptable power supply noise rejection.

The entire clock path, from the input clock to the sampling latches, is implemented with CML stages to achieve good power supply noise rejection. A single phase rotator followed by an I/Q divider assures accurate timing in the sampling front-end. To save power, the use of CML sampling latches is limited to the first sampling stage, where accurate timing is crucial. A capacitively coupled differential to CMOS converter allows a rapid transition from the differential CML clock domain to the CMOS logic swing domain.

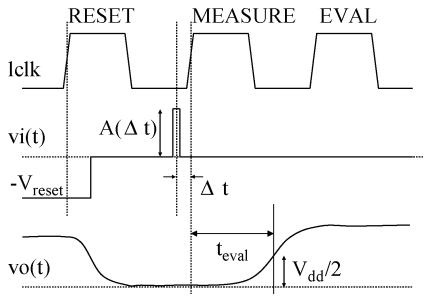

Fig. 27. Signal diagram for latch transfer function extraction procedure.

The proposed CML biasing scheme is based on a unit resistor cell, which allows adjusting the resistance in all CML stages after fabrication, and hence reduces the effective parameter tolerance.

We have proposed a new method for the characterization of sampling latches which captures the properties of the latch in a latch sensitivity function $h_s(t)$ and a DC sensitivity voltage V_s. Using this mode, latches of different topologies or different options for the data path can be easily compared. By dividing the latch in a linear front-end and a nonlinear decision-directed back-end, the dynamic properties of the latch (i.e., its sensitivity function) can be accurately included in the data path.

Appendix
Extraction Procedure for Latch Sensitivity Function

In order to extract the latch sensitivity function $h_s(t)$ from simulations we used the following procedure, which can also be applied to the entire data path. Referencing Fig. 27, the device under test is provided with a clock signal $lclk$, and an input voltage signal $vi(t)$, which both can be either differential or single-ended. The voltage at the latch output $vo(t)$ is evaluated.

The simulation is organized in three cycles. In the first cycle, denoted RESET, the latch is put in state zero by applying a reset voltage $-V_{\rm reset}$. In the next cycle, MEASURE in Fig. 27, the input signal to the latch is zero except for a short probe voltage pulse of amplitude A, width t_w, and time offset Δt with respect to the latch clock $lclk$. The latch detects the signal correctly, if the output signal of the latch $vo(t)$ crosses the midrail voltage $V_{\rm DD}/2$ before the required time $t_{\rm eval}$ in the third cycle EVAL. For a given time offset Δt, the amplitude $A(\Delta t)$ which is just sufficient to flip the latch can now be found. This is done by repeating the measurement cycles with constant Δt and adjusting $A(\Delta t)$ with a binary search algorithm. Stepping the values of Δt inside the sensitivity window then results in the function $A(\Delta t)$. The described algorithm was implemented in a Spectre/VerilogA module, which allows automatic extraction of $A(\Delta t)$ in a few minutes.

Now knowing $A(\Delta t)$, the sensitivity function can be derived. The measurement procedure above finds $A(\Delta t)$ such that

$$A(\Delta t)\int_{T_1}^{T_2} h_s(\tau)rect(t-\tau,t_w)d\tau = V_s \tag{23}$$

where $h_s(t)$ is the latch sensitivity function, T_1 and T_2 are the boundaries of the integration window, and $rect(t,t_w)$ denotes a rectangular pulse of width t_w centered at t and unity height. Rewriting (23) results in

$$h_s(\tau) * rect(\Delta t-\tau,t_w) = \frac{V_s}{A(\Delta t)} \tag{24}$$

from which $h_s(t)$ can be extracted by a deconvolution. For sufficiently small values of t_w

$$h_s(\tau) * rect(\Delta t-\tau,t_w) \cong t_w h_s(\tau) \tag{25}$$

and hence

$$h_s(\tau) \cong t_w \frac{V_s}{A(\Delta t)}. \tag{26}$$

The value of V_s follows from the normalization condition

$$\int_{T_1}^{T_2} h_s(\tau)d\tau = 1. \tag{27}$$

With

$$\int_{T_1}^{T_2} h_s(\tau)d\tau = \sum_n \int h_s(\tau)rect(nt_w-\tau,t_w)d\tau \tag{28}$$

and using (4)

$$V_s = \frac{1}{\sum_n \frac{1}{A(nt_w)}}. \tag{29}$$

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