Power Optimized ADC-Based Serial Link Receiver

E-Hung Chen, *Member, IEEE*, Ramy Yousry, and Chih-Kong Ken Yang, *Fellow, IEEE*

***Abstract*—Implementing serial I/O receivers based on analog-to-digital converters (ADCs) and digital signal post-processing has drawn growing interest with technology scaling, but power consumption remains among the key issues for such digital receiver in high speed applications. This paper presents an ADC-based receiver that uses a low-gain analog and mixed-mode pre-equalizer in conjunction with non-uniform reference levels for the ADC. The combination compensates for both the frontend non-ideality and the channel response while maintaining low ADC resolution and hence enables low power consumption. The receiver is fabricated in a 65 nm CMOS technology with 10 Gb/s data rate, and has 13 pJ/bit and 10.6 pJ/bit power efficiency for a 29 dB and a 23 dB loss channel respectively.**

***Index Terms*—Analog-to-digital converter (ADC), equalization, I/O link, receiver.**

I. Introduction

With aggressive technology scaling over past few decades, the on-chip processing and logic density has continued to increase and push the data rates for serial I/O links to exceed 10 Gbits/second (Gb/s) per lane. Due to the high logic density, receivers that rely on a large degree of digital signal processing are emerging as a potential solution for high-speed serial I/O receiver designs. As shown in Fig. 1, digital receivers incorporate an ADC to digitize the received signal and perform equalization in the digital domain. This type of architecture is commonplace and prevalent for lower data rate applications such as telephone line modems and magnetic disk read channels. The digital backend enables not only potentially more sophisticated signal processing but also better portability to a new fabrication technology. The biggest challenge in this type of receiver is maintaining a reasonable power budget for the ADC and signal processing especially with multi-gigasamples-per-second (GS/s) sampling rates.

Given a power-limited design space, the analog (continuous-time high-pass filter, CT-HPF) or mixed-mode (FIR/DFE) equalization approach still dominates in the low-to-medium attenuating ($<$20 dB) [1]–[3] or the ultra high-speed ($\geq$40 Gb/s) [4], [5] application. Recently, for data rate around 10 Gb/s in applications such as backplane with high attenuation ($>$20 dB) or multi-mode optical link environment, ADC-based receivers [6], [7] have shown sufficiently comparable power/performance

Manuscript received August 26, 2011; revised November 18, 2011; accepted November 20, 2011. Date of publication February 15, 2012; date of current version March 28, 2012. This paper was approved by Guest Editor Vivek De.

E-H. Chen was with the University of California, Los Angeles, Los Angeles, CA 90095 USA. He is now with Rambus, Inc., Sunnyvale, CA 94089 USA (e-mail: enochen@ee.ucla.edu).

R. Yousry and C.-K. K. Yang are with the University of California, Los Angeles, Los Angeles, CA 90095 USA.

Color versions of one or more of the figures in this paper are available online at http://ieeexplore.ieee.org.

Digital Object Identifier 10.1109/JSSC.2012.2185356

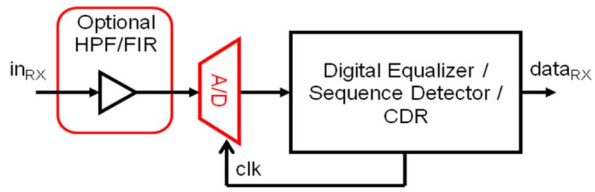


Fig. 1. Generic ADC-based receiver architecture.

to be considered a viable solution in addition to the traditional mixed-mode approach. The architecture proposed in this paper uses a low-gain mixed-signal/analog pre-filtering in conjunction with an ADC-based receiver to pre-shape the signal and reduce the amount of digital signal processing. An ADC-based serial I/O receiver has been implemented to experimentally demonstrate such architectural tradeoff. This paper further extends upon the analysis in [8] by demonstrating the benefits an ADC with non-uniform quantization levels to improve the performance and the power efficiency. The benefit and design consideration of the low-gain analog frontend (AFE) are discussed in Section II, and the implementation and adaptation method of variable reference adjustment and selection-based DFE are introduced in Section III. The receiver is implemented in a 65 nm CMOS technology and operates at 10 Gb/s data rate. The measurement results and the performance comparison of different ADC-based and mixed-mode receivers are provided in Section IV.

II. Low-Gain Analog and Mixed-Mode Frontend

The receiver design for high-loss serial link application usually adopts simple frontend circuitry to perform pre-filtering. In a mixed-mode receiver, a continuous-time HPF, or sometimes referred to as continuous-time linear equalizer (CTLE), is a common building block for receiver pre-filtering [9]–[11]. A CTLE contains variable DC gain to adjust received signal swing and variable high-frequency boosting to provide equalization. Even many of the published ADC-based receivers, a continuous-time HPF have been implemented [6] to pre-shape the signal, or a dedicated programmable gain amplifier (PGA, or a variable gain amplifier, VGA) is used [7], [12] to adjust signal swing to properly drive the ADC.

The diagram of the AFE in our proposed ADC-based receiver is shown in Fig. 2, which comprises a continuous-time HPF, a sampled-FIR, and a VGA to perform receiver pre-filtering. Based on the results in [8], this architecture uses the HPF and sampled-FIR to provide a power-efficient equalization and to dramatically reduce the power and resolution requirements of the following ADC and DSP. The circuit implementation is discussed in Section II.A. The VGA in the proposed AFE is designed to provide excess gain so that the signal sampled by the ADC is operated beyond the typical linear region. Although the

0018-9200/$31.00 © 2012 IEEE

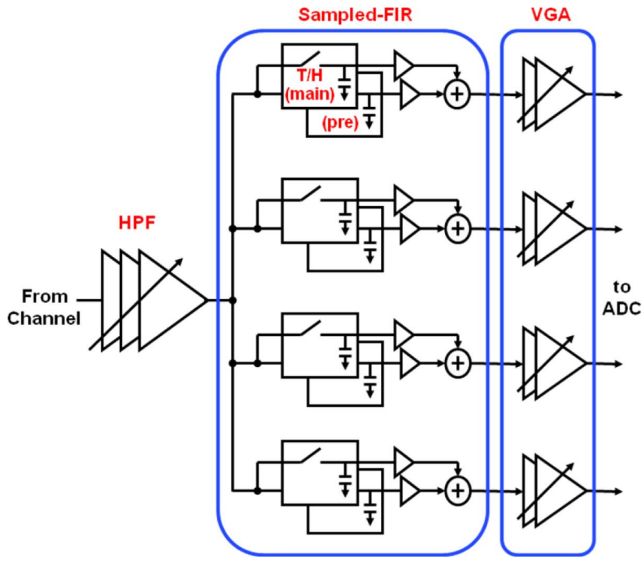


Fig. 2. Block diagram of the AFE in the proposed ADC-based receiver. It consists of a continuous-time HPF, a pre-tap sampled-FIR, and a VGA for receiver pre-filtering.

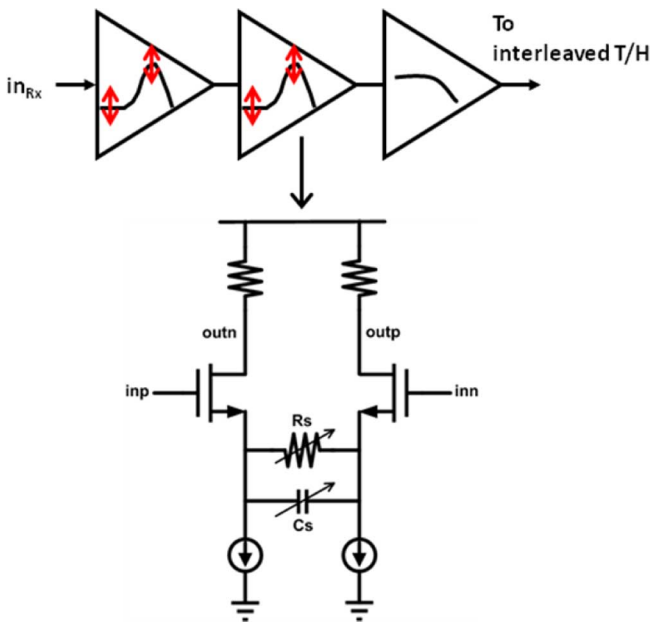


Fig. 3. Block diagram of a 3-stage continuous-time high-pass filter. The first two stages contain programmable degeneration resistors and capacitors, and the third stage is with low output impedance to drive interleaved T/H.

signal may experience nonlinearity and saturation in large VGA gain setting, this paper shows that a receiver performance is improved with proper VGA adaptation. The analysis of such nonlinear operation and the adaptation strategy is covered in Section II.B

A. Circuit Implementation of the HPF and Sampled-FIR

The first component in our AFE is a continuous-time HPF and it is realized by three CML stages with variable degeneration resistors and capacitors as shown in Fig. 3. While the first two stages provide a wide tunable range of both DC and high frequency boosting, the third stage is used to drive approximate

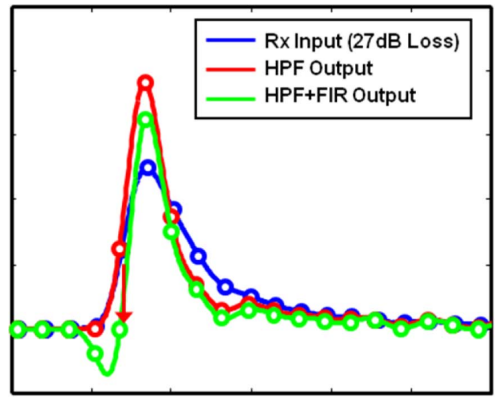


Fig. 4. An example of pulse responses before and after the HPF and FIR filter. The HPF provides 9 dB boosting at Nyquist frequency and the FIR cancels 1st pre-cursor ISI.

300 fF loading of following interleaved T/H circuitry. The HPF in the proposed receiver provides up to 12 dB boosting at 5 GHz (while DC gain is equal to 1) and only consumes 6 mW in 1.1 V supply. The main benefit of this continuous-time HPF is to apply a power-efficient receiver pre-filtering. The pulse responses in a 27 dB loss channel before and after a 9 dB gain boosting at Nyquist frequency are shown in Fig. 4. The HPF improves the ratio between main cursor and 1st pre-/post-cursor ISI, and also reduces the smooth long tail of the pulse response. Simulation shows a roughly 10% reduction in the ratio between the sum of 1st pre-/post-cursor ISI and the main cursor for every 3 dB boosting at Nyquist frequency across different channels. A notable result in this example is that the value of 1st pre-cursor ISI after the HPF is still substantial. This residual pre-cursor ISI cannot be cancelled by the following DFE and could degrade link performance.

The residual pre-cursor ISI can be cancelled using an FIR at the receiver.[1] This FIR can be implemented with little power cost when combined with the sample-and-hold (S/H) or track-and-hold (T/H) of the ADC. In order to realize multi-GS/s ADCs, an interleaving architecture using multiple clock phases of a slower frequency clock is adopted. In the proposed AFE, a 4-way interleaved structure is adopted after HPF to alleviate the bandwidth requirement. By using an interleaved T/H for each ADC path, each T/H is used as part of the sampled FIR. Although a 3-tap sampled FIR can be realized in a 4-way interleaving architecture [13], a 2-tap sampled FIR for pre-cursor ISI cancellation is used in order to satisfy the settling time of T/H and following stages. The circuit and timing diagrams of this 4-way interleaved 2-tap sampled FIR are shown in Fig. 5. A designated pre-tap T/H is used in each interleaved path to avoid the long wire routing and minimize the timing mismatch. Multiple clock phases for the sampled-FIR are generated by a capacitor-coupling interpolator [14] and have individual delay and duty-cycle control in each interleaving path to compensate the mismatch between paths.

As shown in [15], depending on the channel, a pre-tap FIR may degrade link performance because the pre-cursor subtraction would reduce the main cursor strength due to large 1st

[1]Alternatively, an FIR at the transmitter can be equally effective but at the cost of peak signal power.

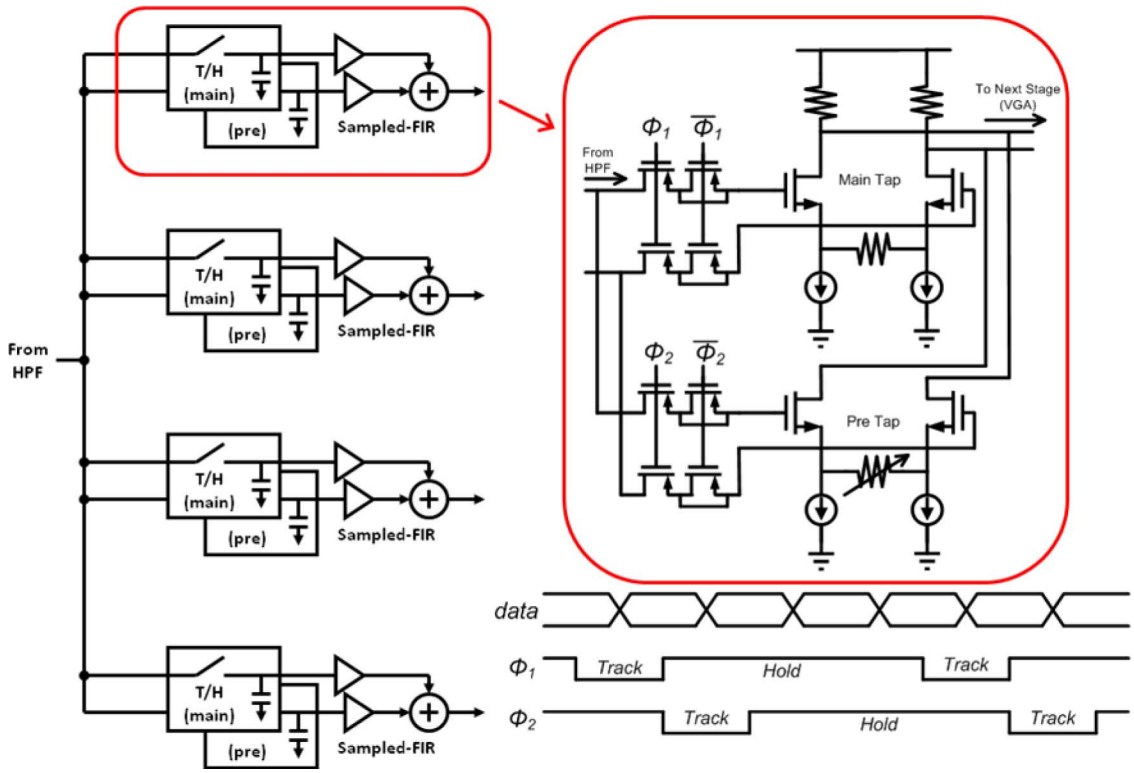


Fig. 5. Block and timing diagrams of a 4-way interleaved 2-tap sampled-FIR for pre-cursor ISI cancellation.

post-cursor ISI and could also introduce other uncompensated pre-cursor ISIs if the length of FIR is short. It is noteworthy that this implementation uses the preceding HPF to pre-shape the signal to increase the ratio between main cursor and 1st post-cursor, and hence increase the efficiency of this pre-tap FIR. The effective pulse response after this sampled FIR is shown in Fig. 4 where the 1st pre-cursor ISI is removed completely.[2] The total power consumption of the T/H with the sampled-FIR embedded is 11 mW.

By combining HPF and FIR, the AFE can perform more than 10 dB equalization and lead to around 1–2-bit saving in the required ADC resolution [8]. Moreover, the sampled-FIR replaces the costly digital FIR in the DSP and the digital DFE can be further simplified by using a selection-based architecture as discussed in Section III. The design maintains scalability for both data rate and technology by requiring no more than 10 dB of analog gain for any of the circuit blocks.

B. VGA Gain Setting and Nonlinear Operation

The capacitive loading of the comparators of the ADC is typically driven with a low output impedance buffer. In this implementation, CML buffers are used. Programmable source-degeneration resistors are added to the CML buffer to form a VGA. The two-stage design provides up to 12 dB gain to buffer the signal before the ADC and the second stage of the VGA includes a common-mode feedback circuit to set its output common mode equal to the midpoint of following ADC reference as shown in Fig. 6.

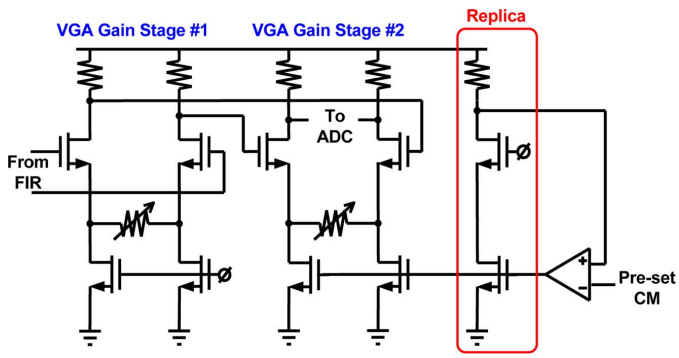


Fig. 6. Schematic of a 2-stage VGA with output common mode feedback.

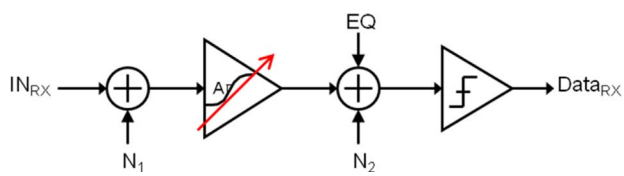


Fig. 7. Simplified AFE model with a VGA. The additive noises before and after VGA are denoted as N_1 and N_2 respectively.

In our receiver design, the VGA is followed by a variable reference ADC. The optimal gain for the VGA depends on the noise condition of the receiver. Fig. 7 shows a simplified diagram of the two primary sources of noise in the receiver. Intuitively, when the input referred noise of the AFE (or input signal), N_1, is the dominant noise source, the VGA does not

[2]Eliminating 1st pre-cursor ISI completely by the FIR doesn't guarantee optimum performance [15]. The simulated/measured results in this paper use a BER-based adaptation for equalizer coefficients can lead to near optimum performance across channels.

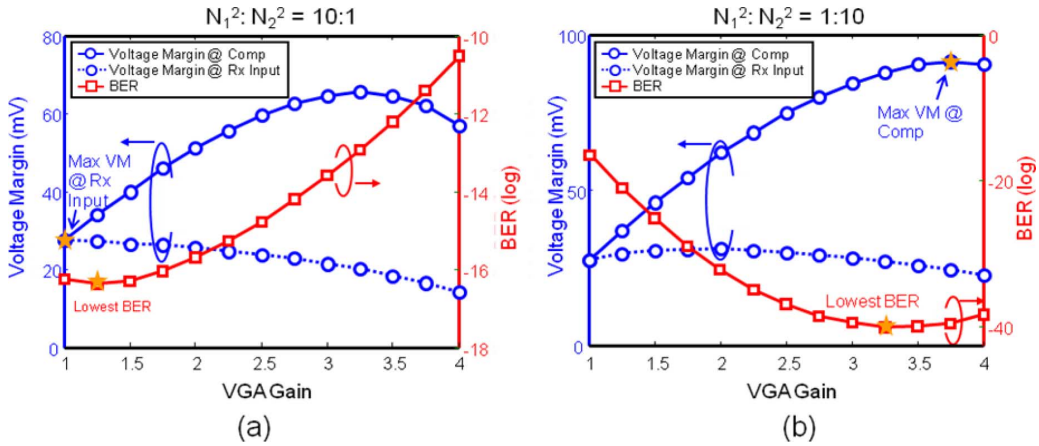


Fig. 8. Illustration of the dependence on noise condition of the VGA adaptation. The BER performance as a function of the VGA gain when the adaptation target is the voltage margin (a) at the receiver's input, and (b) at the comparator's input. The ADC's quantization error is ignored in this simulation.

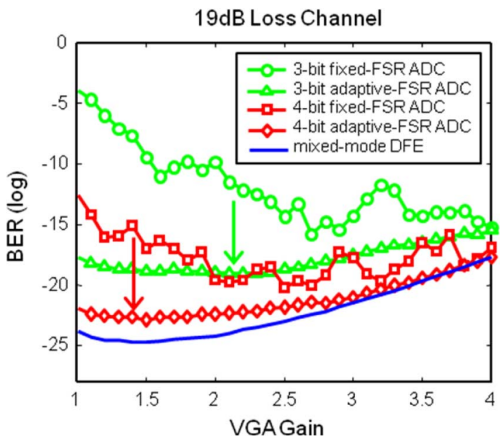


Fig. 9. BER performance as a function of VGA gain with different ADC resolution and setting. A 5-tap (digital) DFE is used as the post-processing. N_1 noise power is $4\times$ of N_2 in this simulation setup.

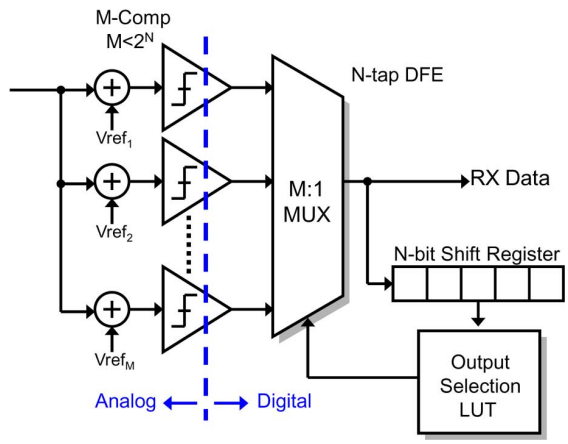


Fig. 10. Block diagram of a selection-based DFE with a look-up-table in the feedback path.

improve the SNR and the signal only needs to be amplified so that the signal magnitude spans the full-scale range (FSR) of the ADC [7], [16]. Alternatively, when the input referred noise of the comparator, N_2, dominates, a higher gain is desired to increase the SNR. This intuition is illustrated in simulation in Fig. 8.

While the quantization noise is presented in an ADC-based receiver, the receiver would favor a large VGA gain to reduce the effect of quantization noise even N_1 is larger than N_2 as shown in Fig. 9. Since a large output signal is desirable, the VGA outputs can be nonlinear and saturated once the effect is smaller than the quantization noise. However, using an adaptive FSR for the ADC following the VGA can relax the gain and voltage requirement of the VGA. The ADC reference adaptation can adjust the ADC's FSR to maximize the signal to noise ratio and compress the reference levels near the edges of the signal magnitude as needed.

Simulation results in Fig. 9 show that adaptive FSR ADCs (with 8 and 16 levels) can perform near the performance of an ideal DFE and considerably improved in comparison to 3 and 4 bit uniform ADCs with fixed FSR. Also note that fixed FSR ADCs exhibit zigzag patterns as VGA gain increases because the reference voltages may not slice the input signal at voltage levels with high SNR due to the ISI distribution from the particular channel. The adaptive ADC FSR can reduce the effect of quantization error and hence the SNR is improved. Because the references are more optimally placed, the receiver behaves like a loop-unrolled DFE so that the optimal VGA gain is lower. As we show in the measurements in Section IV, due to the HPF, and the sampled FIR, noise in our ADC-based receiver is dominated by the input noise rather than the noise of final decision comparator; hence, the input referred noise can be used as the metric to perform the VGA adaptation. Furthermore, from this analysis, only a modest gain of 6 dB is needed to minimize the BER hence potentially allowing further power savings.[3]

While the receiver performance is improved by the ADC with adaptive FSR, a possible half-LSB voltage margin degradation still exists in a uniform spacing ADC. Hence, the ADC quantization error can be further reduced by allowing non-uniform reference levels. The next section discusses the details of an ADC with non-uniform reference levels.

[3]Our design overdesigned the gain in anticipation for the potential of a very weak input signal. The input signal magnitude of a copper channel can be >500 mV differentially. Potentially, 4 mW of power can be saved.

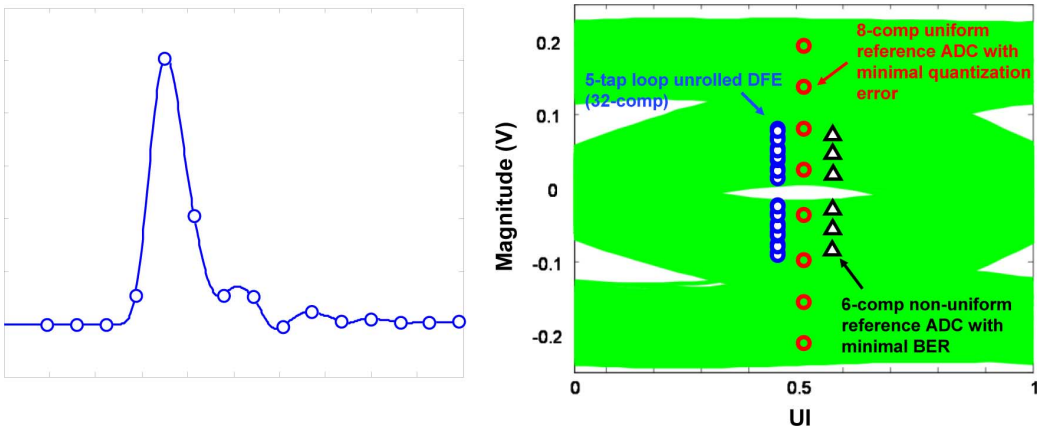


Fig. 11. Comparator reference positions in different ADC settings for a 13.5 dB loss channel. The channel exhibits a large 1st post-cursor ISI, similar 2nd and 3rd post-cursor ISIs, and small 4th and 5th post-cursor ISIs. A 6-comparator non-uniform reference ADC can achieve similar performance as a 32-comparator, 5-tap loop-unrolled DFE.

III. Non-Uniform ADC Reference

ADCs quantize the analog input signal into discrete digital steps for the subsequent digital signal processing. To preserve the information of the analog waveform, an ADC is usually designed to minimize the quantization errors, and because of the randomization of incoming signal level, the ADC references are usually equally-spaced. However, this may not be the optimum setting for an ADC used in the I/O receiver where the signal content depends on the filtering of the transmission medium.

As discussed in Section II, the FIR has been implemented in the receiver AFE. This approach saves a substantial amount of power since a digital FIR at 10 GS/s can be exceedingly power hungry [17], [18]. Furthermore, as Section III.A will show, a digital selection-based DFE can be very efficiently implemented along with a non-uniform ADC. The section focuses on the similarity and differences between such architecture with a loop-unrolled DFE [19]. Section III.B discusses the implementation details of the ADC with programmable references. Section III.C describes the implementation of the proposed selection-based digital DFE. Since the reference levels of the non-uniform ADC depends on the channel characteristics, Section III.D describes the adaptation algorithm for the ADC. Finally, Section III.E discusses the implications of the non-uniformity on timing recovery and the implementation of baud-rate timing recovery.

A. Selection-Based DFE Using Non-Uniform ADC Outputs

A basic diagram of a selection-based DFE is shown in Fig. 10. Such selection-based DFE does not require additional resolution internal to the filter beyond the resolution of its input (i.e., ADC's resolution), and have identical performance as a digital DFE using multiply-adds. In the case of a flash-ADC, ADC's thermometer outputs are used by the DFE directly without converting to binary, and one comparator's output is selected as the final data according to prior data history. For a M-comparator ADC with N-tap DFE, N-bit data history is mapped to M threshold levels by a look-up-table (LUT) [20], [21].

Because one comparator's output is selected as the final decision based on previous data, the position of the comparator's threshold level is critical to the equalizer's performance. In a uniform quantization ADC, the maximal deviation of comparator's reference from its optimum value could be as large as half-LSB of ADC. Hence, a straightforward method to improve receiver performance is to increase ADC's resolution. Because both the hardware and power penalties of a high-speed high-resolution ADC are large, a low-power design can be realized by implementing an ADC with non-uniform quantization levels.

The concept of combining non-uniform ADC reference and selection-based DFE is equivalent to a loop-unrolled or partial response DFE when using 2^N comparators for N-bit history. While adopting a pure digital implementation without any analog feedback loop after ADC's comparators, this approach offers more flexibility than a loop-unrolled DFE by using only the necessary number of comparators. For instance, if the link pulse response has similar ISIs or some ISIs are close to linear combinations of others [20], a small set of optimum reference levels can be determined by a recursive method [20], [21].

Fig. 11 shows an example of reference levels in a uniform ADC and a non-uniform ADC for a 13.5 dB loss channel. Because 1) the 2nd and 3rd post-cursor ISIs in this channel have similar magnitude, and 2) the 4th and 5th post-cursor ISIs are relatively small compared to 1st–3rd post-cursor ISIs, the optimal reference levels are gathered into 6 groups, and a 6-comparator non-uniform ADC can already achieve similar performance as a 5-tap loop-unrolled DFE which requires 32 comparators.

Because the improvement of such non-uniform references is channel dependent, more performance analysis is verified in simulation by using 10 backplane channels with 15 to 35 dB attenuation at the Nyquist frequency ([8] Fig. 4). These 10 channels are combined with four receiver high-pass filter and two pre-tap FIR settings to create total 80 different link responses. Fig. 12 shows the simulated performance of a receiver with low resolution ADC compared to a receiver with 5-tap loop-unrolled DFE. The receiver input swing is set to 800 $\mathrm{mV_{pp-diff}}$. By allowing 13 mV degradation compared to a 5-tap loop-unrolled DFE, simulation shows a 12-comparator non-uniform ADC with optimum reference setting plus a 5-tap selection-based DFE can achieve this goal in all link responses.

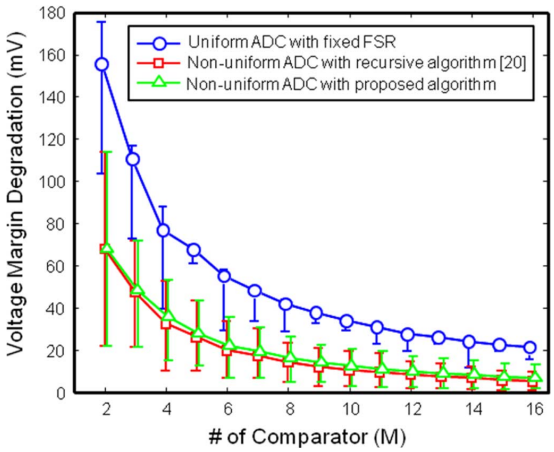


Fig. 12. Simulated voltage margin degradation of a receiver with uniform and non-uniform ADC reference. Zero voltage margin reference is a 32-comparator, 5-tap loop-unrolled DFE. The graph shows the minimal, maximal, and average voltage margin reduction of a receiver with different ADC configurations in 80 different link responses. The adaptation method proposed in Section III.D can achieve near-optimum non-uniform ADC reference setting.

If using an ADC with 0.5 pJ/conv-step figure of merit (FoM) as the benchmark, it implies around 100 mW power saving for a 10 GS/s ADC implementation.

B. Circuit Implementation of ADC With Variable Reference

With the aid of low-gain AFE and non-uniform reference setting, the ADC in the proposed receiver only requires a small number of slicing levels to achieve the targeted performance. Moreover, due to the nature of selection-based DFE, the ADC's thermometer outputs are used directly. Hence, a 4-bit flash architecture is chosen to be the ADC in our receiver. Unused reference levels can be optionally turned off to potentially yield more power savings. To achieve the non-uniform reference levels, each comparator's reference can be adjusted over a wide tuning range with small step size because any residual offset would adversely affect the receiver performance. The receiver input referred offset is around 20 mV (σ_{os}) before compensation, and the offset due to AFE are compensated in advance by the offset cancellation circuitry inside the AFE block with offline calibration.

The proposed reference adjustment of ADC's comparator is embedded in the offset cancellation and combines two methods to achieve larger tuning range as shown in Fig. 13. The first approach is to select the tap-point from the resistor ladder by a 3-bit coarse control signal. The nominal setting of each coarse step is 15 mV. The selected voltage is connected to a PMOS reference buffer, where the bodies of PMOS devices are connected to another resistor ladder with 3-bit digital control to perform reference fine-tuning [22]. The MOS threshold voltage changes with body bias and its value changes with PVT. Simulation shows the PMOS threshold voltage has $\pm 25\%$ variation across PVT and around 62.5 mV/V sensitivity in 65 nm technology. The fine-tuning range covers 1.5 coarse steps, but both coarse and fine-tuning can be adjusted by changing the current through the resistor ladder to further increase the adjustable range. By combining both methods, the reference tuning range

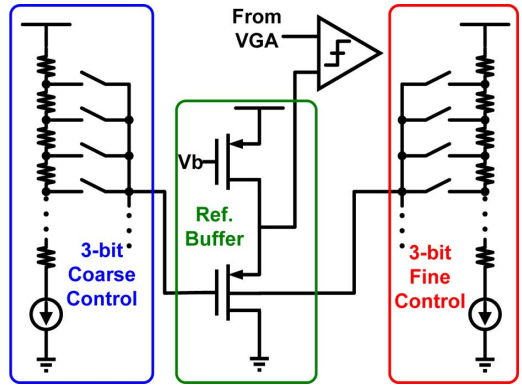


Fig. 13. The comparator reference level adjustment combines coarse and fine-tuning to achieve a large range.

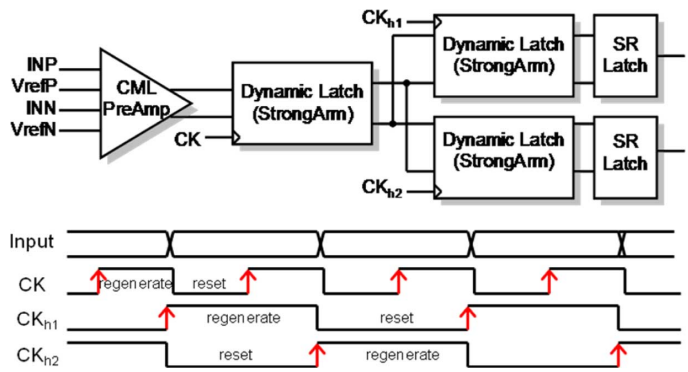


Fig. 14. Block and timing diagrams of the multi-stage comparator in the ADC. The data path is interleaved after 2nd stage.

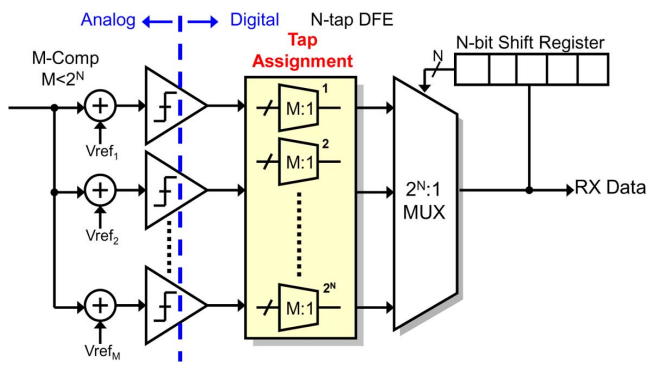


Fig. 15. The proposed selection-based DFE with the tap assignment block which routes ADC's outputs to proper positions of final selection MUX.

of each comparator is more than 100 mV with minimal 2 mV step size in default setting, which is sufficient to provide the offset cancellation of a 4-bit ADC, and also enables the variable reference tuning.

Because there is no analog feedback loop in an ADC-based receiver, the regeneration time or the latency of comparator is not a critical design issue. Hence, a multi-stage architecture is used in the comparator design to reduce the probability of metastability and also achieve low power consumption. The first stage of the comparator is a four-input CML to perform the reference subtraction and is followed by a dynamic StrongArm latch [23]. The data path is further interleaved after the second stage by two more dynamic latches triggered by half-rate clocks.

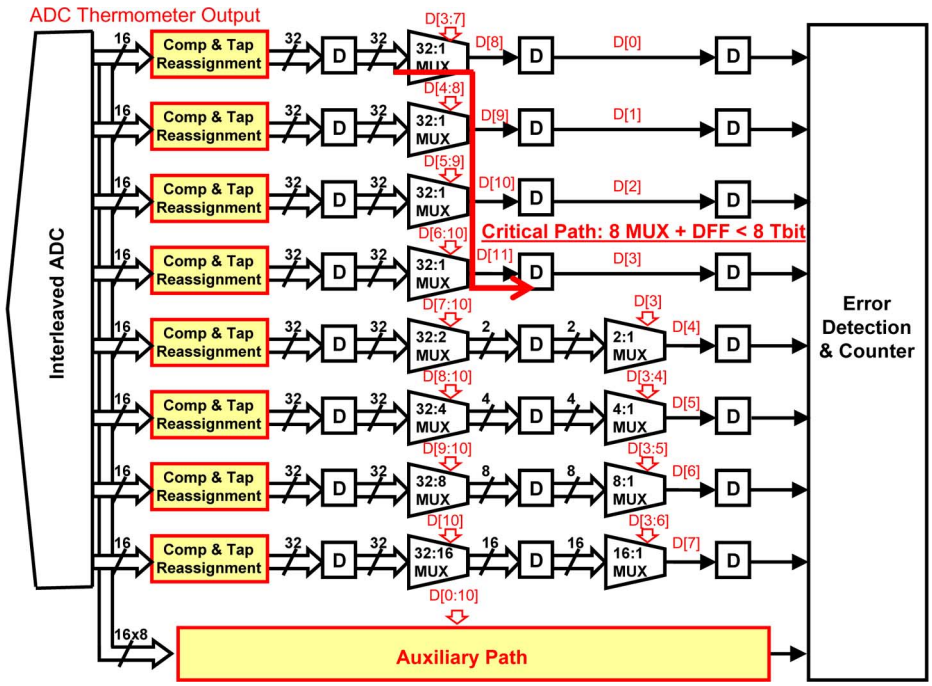


Fig. 16. Block diagram of the 8× parallel 5-tap selection-based DFE in the test chip.

Since the signal is amplified by the first two stages to some extent, the design requirement of half-rate dynamic latches is relaxed and can use small device size to achieve low power. The block and timing diagrams of a comparator are shown in Fig. 14.

Each comparator operates at 2.5 GS/s to achieve a total 10 GS/s in a 4-way interleaved architecture and consumes 0.75 mW including the clock power. With this comparator architecture, the ADC's outputs are 1.25 Gb/s with 8× parallelism, which accommodate the speed of subsequent digital processing and no further de-serializing is required.

C. Implementation of Selection-Based DFE

The key component of a selection-based DFE is the LUT which maps stored data history to ADC's outputs. However, as shown in Fig. 10, this LUT exists in the feedback path and can limit the maximum data rate [21]. This paper proposes a selection-based DFE architecture for low number of tap by using a tap assignment block as shown in Fig. 15. The tap assignment block for N-tap DFE consists of 2^N M-to-1 MUX to route M-comparator ADC's outputs to proper positions of following final selection 2^N-to-1 MUX. Each tap reassignment block is selected by static control bits and can be embedded into the comparator reassignment algorithm for offset cancellation to increase the yield. It is equivalent to the LUT but implemented in the feed-forward path and also makes the following N-tap DFE as simple as a 2^N-to-1 tree-type MUX. Each input of the final 2^N-to-1 MUX is assigned to one of 2^N possible ISI offsets. Such regular structure of tree-type MUX is easy for pipelining to meet the timing constraint. However, the hardware requirement of proposed selection-based DFE grows exponentially with number of DFE tap. Our implementation shows a 5-tap DFE is achievable for 10 Gb/s throughput in a 65 nm CMOS technology with less than 40 mW power consumption. With this architecture, the receiver can also be configured as a traditional 1–4-tap loop-unrolled DFE for verification purpose because there are only 16 comparators in the ADC.

Fig. 16 shows the complete diagram of the 8× parallel 5-tap selection-based DFE in our test chip. The entire digital DFE only consists of simple multiplexer and flip-flop and is synthesized with a 65 nm CMOS standard cell library. The final 32-to-1 MUX is pipelined carefully to achieve critical path equal to the delay of 8 2-to-1 MUX + 1 F/F, which must be less than 8-bit times (800 ps for 10 Gb/s).

An auxiliary path is also implemented for testability and adaptation. The path has same structure as the data path except it accommodates the input and feedback data from any of the interleaving paths so that it can be programmed as the replica of the data path. Since each comparator's output in the data path is selected as the decision of one or more particular 5-bit data patterns, the voltage margin can be traced by comparing its output to an extra comparator with adjustable reference voltage. The output of this extra comparator is routed into the replica path to replace the targeted comparator, and because the tap reassignment block acts as the data filtering, the output of replica path are XORed with the result from data path directly to perform pseudo BER detection [15]. The true BER measurement is also implemented in the test chip by using a PRBS decoder in the DSP.

The completed voltage margin information can be constructed by tracing through all possible data patterns. A simple diagram of voltage margin detection is illustrated in Fig. 17. This method only requires one extra comparator in a multi-bit ADC for voltage margin measurement and enables the BER-based adaptation without affecting the performance in data path.

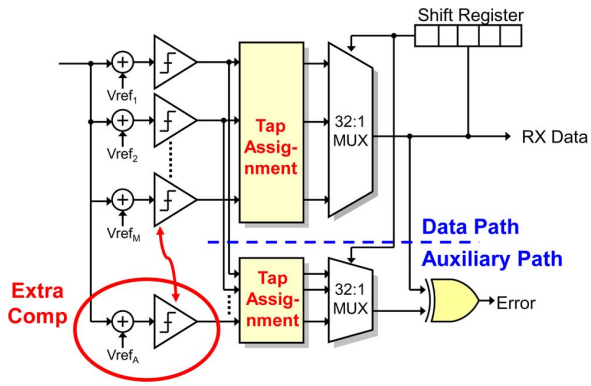


Fig. 17. Pseudo BER and voltage margin measurement by using the auxiliary path.

D. BER-Based Adaptation for Non-Uniform ADC Reference

The optimum ADC reference setting for an ADC-based receiver can be determined by solving a complex set of optimizations or running a recursive programming procedure. The method proposed in [20] requires prior knowledge of exact ISI values, and the hardware and computation time grow quickly with ADC resolution and DFE tap number. This paper proposes a non-uniform ADC reference setting that combines traditional SS-LMS and BER-based approach for fast adaptation and practical implementation. The algorithm of the proposed adaptation method is shown in Fig. 18.

The first step of the algorithm is applying SS-LMS adaptation for DFE coefficient setting in a 16-comparator uniform reference ADC. This step is the same as the DFE adaptation of a uniform reference ADC-based receiver and is to have an initial grouping that assigns ISI offsets to the nearest comparator reference. Because traditional SS-LMS is known for its simple hardware requirement and fast convergence time, this step provides the system an acceptable initial point. Note that because of the non-uniform distribution of ISI offsets, there may be some comparators in the ADC that are not used after the initial assignment.

In the next step, the pseudo-BER measurement described previously is applied to find the voltage margin of received signal. Because each comparator's output represents one or more data patterns, the receiver performance is optimized by placing comparator's reference in the center of each partial-response eye. The voltage margin after the reference adjustment is compared with a target value, 30 mV voltage margin at $\mathrm{BER} = 10^{-6}$ for example. If the target is met, the comparator with maximal voltage margin is turned off to save the power and its corresponding ISI offsets are assigned to the adjacent comparator(s). Then the new comparator reference levels are set again according to the measured voltage margin. After few iterations, the ADC can achieve a setting that satisfies the targeted performance with minimal number of comparators.

The result of this adaptation strategy depends on the initial assignment by SS-LMS adaptation so that it may not be able to achieve optimum ADC reference setting. The simulation results in Fig. 12 show the joint-adaption with SS-LMS and non-uniform reference tuning in proposed adaptation method has around 2 mV reduction in voltage margin compared to the results using an exhaustive recursive algorithm across different link responses.

E. Baud-Rate Timing Recovery

The sampling clock of the design is generated by an on-chip interpolator and its phase is determined according to the measured BER [16]. Although the complete CDR loop is not implemented in the digital post-processing, a baud-rate timing recovery scheme is proposed for the ADC-based receiver and verified using a feedback loop closed with the test setup. A baud-rate timing recovery algorithm is usually preferred in an ADC-based receiver because no additional samples are needed, ADC's outputs are reused, and the design can take advantage of low-cost digital signal processing. Such data-driven method uses the discrete samples to estimate phase information. However, in the proposed receiver with non-uniform ADC reference, each comparator's reference is located in the eye center of certain data pattern(s); hence the ADC's output cannot be used directly to extract accurate phase information.

In the proposed baud-rate timing recovery for the ADC-based receiver with non-uniform quantization, a data filter stores the data history of 3 bits which include the data from previous sample (bit), current sample (bit) and next sample (bit). The data filter removes the impact of the previous bit to eliminate the noise due to large 1st post-cursor ISI. This implementation allows the potential for longer or different data filtering if necessary [24]. One extra comparator is used to monitor the data transition and its threshold level is placed in the middle of the selected data patterns. The clock sampling phase is moved forward or backward according to the probabilities of different data patterns above or below this threshold.

For example, 3-bit data transition 1-0-1 and 1-0-0 in a 20 dB loss channel are shown in Fig. 19(a), where the 1st pre-cursor ISI has been cancelled by the FIR. The thick dash line in the figure represents the comparator's threshold which is set to the mean of the two data transitions. The sampling clock phase is moved backward if the probability of a "101" transition that is sampled with a value above the threshold is equal or smaller than the probability of a "100" transition. Conversely, the phase is moved forward if the probabilities are reversed. With this algorithm, the clock locks at the phase with zero 1st pre-cursor ISI. In the case where the 1st pre-cursor ISI is not cancelled completely, the clock locks at an earlier phase as shown in Fig. 19(b). The locking phase can be intentionally shifted by changing the weighting factor when counting the probability of transition to favor the case above or below the threshold, and this weighting factor can be controlled by the BER results [15].

IV. Measurement Results

Fig. 20 shows the complete block diagram of the proposed ADC-based receiver. Receiver's outputs are fed into on-chip PRBS checkers or pseudo-BER detector and their results are stored in an 11-bit counter. The test chip's micrograph is shown in Fig. 21. It is fabricated in a standard 65 nm CMOS technology with active area of 0.26 mm^2, and is tested in a chip-on-board assembly. In the measurement setup, a 10 GHz synchronized

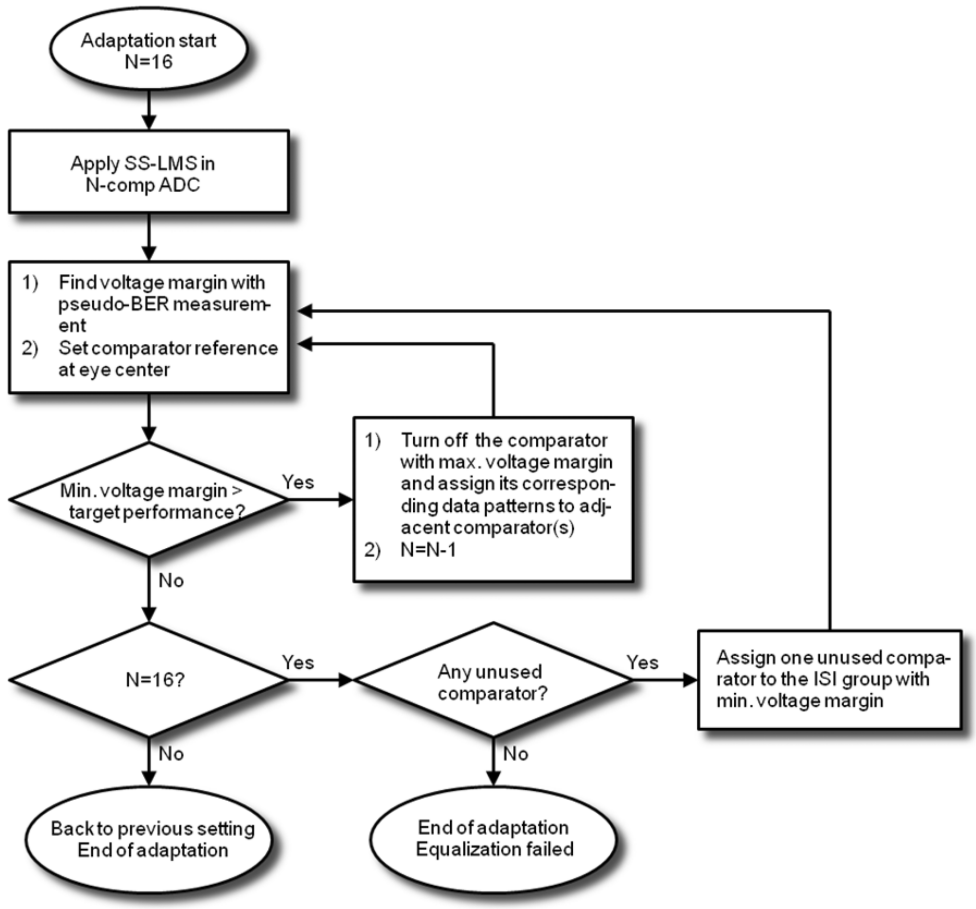


Fig. 18. Flow diagram of non-uniform ADC reference adaptation algorithm.

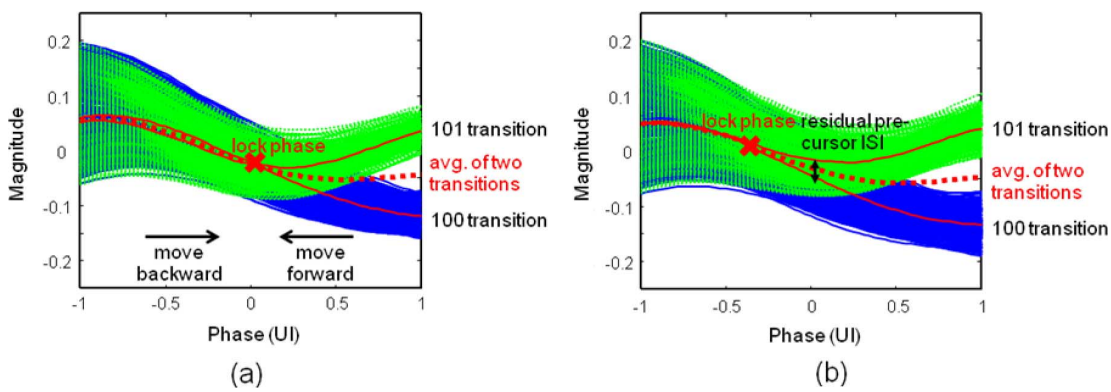


Fig. 19. Lock position of proposed baud-rate timing recovery while (a) the 1st pre-cursor ISI is cancelled, and (b) the 1st pre-cursor ISI is uncompensated. The "101" and "100" data transitions are monitored by the data filter.

clock is forwarded along with PRBS31 data from the transmitter module and then divided by the on-chip dividers into four 2.5 GHz quadrature-phase clocks. The sampling clock is then generated by an on-chip interpolator and its phase is determined using the BER based adaptation. The receiver performances with different configurations are tested over two channels with 23 dB and 17 dB loss at Nyquist frequency to demonstrate the architectural tradeoff of an ADC-based receiver.

Section IV.A shows the laboratory results of receiver's performance in different AFE settings. The performance improvement of non-uniform reference ADC in three different link responses are examined in Section IV.B, and the measured data transition for the proposed timing recovery is shown in Section IV.C. The performance of proposed ADC-based receiver is summarized and compared with recent publications in Section IV.D.

A. AFE Pre-Filter Experimental Results

Fig. 22 shows the impact of the HPF and FIR on the receiver performance with different ADC resolution while a 5-tap digital DFE is used.

The HPF consumes only 6 mW while the sampled FIR (which includes the ADC's T/H) consumes 11 mW. The results indicate

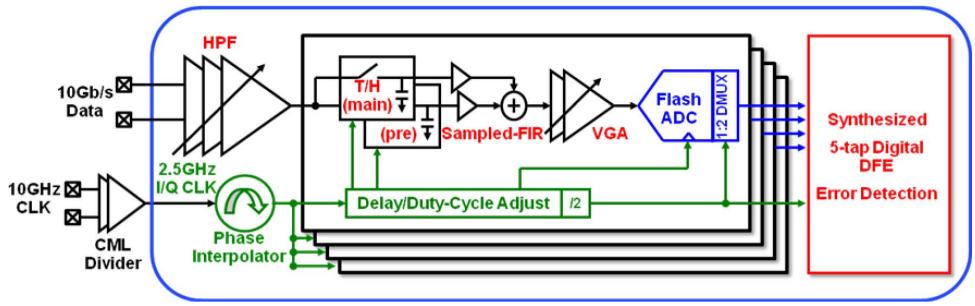


Fig. 20. Block diagram of the proposed ADC-based receiver.

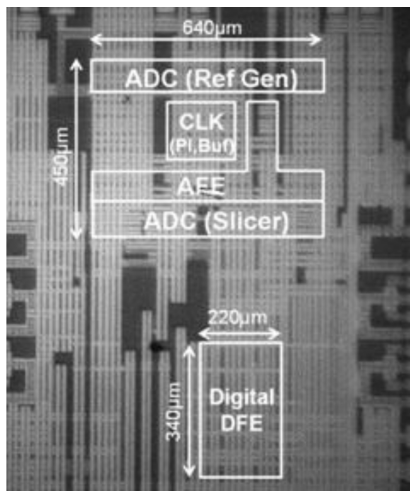


Fig. 21. Micrograph of the test-chip.

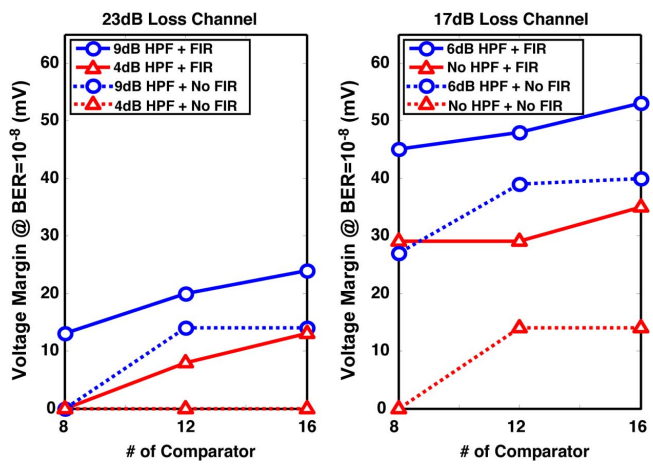


Fig. 22. Measured receiver voltage margin with different HPF and FIR settings.

that with the aid of the low-gain pre-filtering, the requirement of the following ADC can be relaxed. Roughly 1-bit is saved in the ADC resolution when either the HPF or FIR is used in these two channels. The unused comparators in the test chip can be turned off to improve the power efficiency. For example, if an 8-comparator ADC is used in the receiver instead of a 16-comparator ADC, a total 24 mW can be saved in ADC's power.

In addition to the pre-filter, the VGA's gain control can increase the SNR. In the test chip, the multi-stage AFE contributes more noises than ADC's comparator, and because the signal is sampled before the VGA, the jitter-induced voltage noises are also added into the system before the VGA amplification. Hence, the optimum VGA gain setting is adapted according to the voltage margin at receiver's input with the presence of nonlinearity and limited swing in the VGA. The voltage margin at receiver's input is obtained through dividing the measured voltage margin at ADC's input by AFE's low-frequency gain. This AFE low-frequency gain can be obtained either through the off-line characterization or a live monitoring which derives a normalized gain by comparing the value of non-uniform ADC reference in different VGA settings.

Fig. 23 shows the receiver performance with different VGA gain settings. The receiver input swing is 600 $\mathrm{mV_{pp-diff}}$ and the receiver configuration is set to use the 8-comparator ADC and 5-tap digital DFE. The BER at the eye center is the result of extrapolating the measured BER bathtub curve which is only down to 10^{-11} BER due to limited measuring time.

B. Non-Uniform ADC Experimental Results

The non-uniform ADC reference setting relies on the ISI offset distribution. Hence, its performance improvement over the uniform quantization ADC is channel dependent. The performance of different receiver configurations in several pulse responses created from a 17 dB loss channel by applying different pre-filtering are examined.

The effective pulse response of one sampling phase and pre-filter setting is shown in Fig. 24(a). Because the response has one large post-cursor ISI of 53 mV followed by many small taps, the optimal reference levels are clustered around $+53$ mV and -53 mV levels. Such uneven distribution of the required ADC reference is difficult to realize with a low-resolution, uniform quantization ADC and as a result, the uniform ADC receiver have worse performance. The receiver with non-uniform reference ADC outperforms other architectures[4] including loop unrolled DFE and reducing the full-scale range of an uniform ADC as shown in Fig. 24(b).

A different pulse response can illustrate a different tradeoff between architectures. The effective pulse response shown in Fig. 25(a) also has a dominant 1st post-cursor ISI and many

[4]The other options are verified and measured using different settings and configurations of our ADC and DSP.

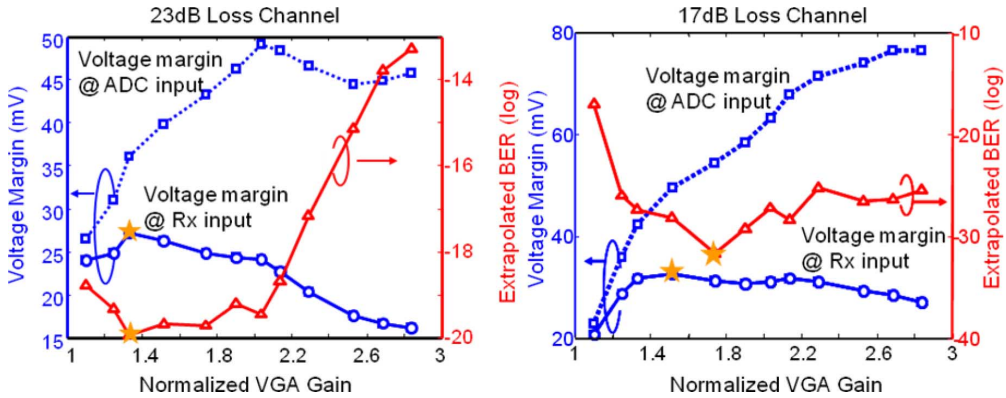


Fig. 23. Measured receiver performance with different VGA gain settings.

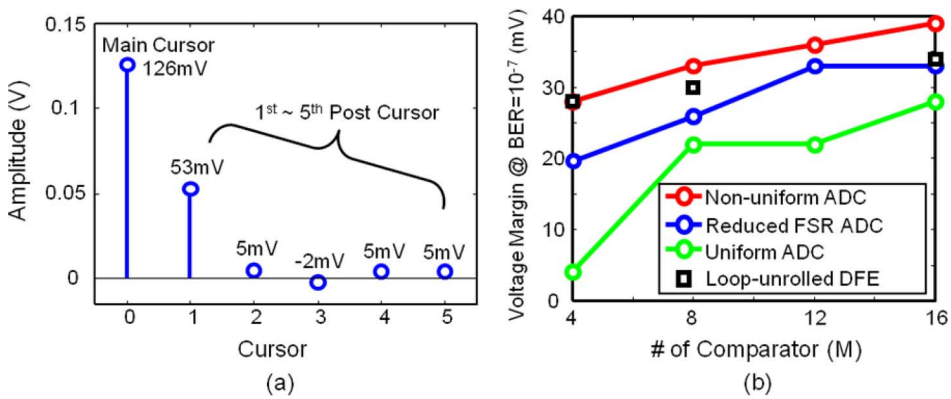


Fig. 24. (a) The channel response for this measurement, (b) measured voltage margin versus the number of comparator for different ADC-based receiver configurations.

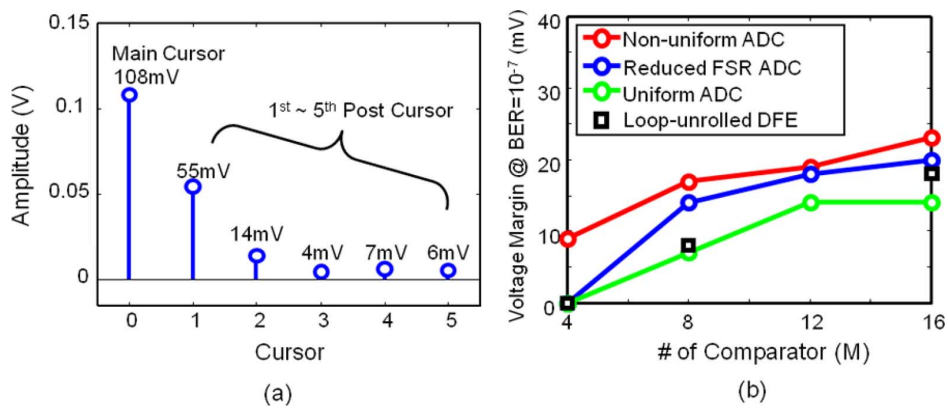


Fig. 25. (a) The channel response for this measurement, (b) the voltage margin versus the number of comparator with different ADC-based receiver configurations.

smaller ones. Similar to Fig. 24, the non-uniform ADC reference outperforms other architectures. Such non-uniform reference ADC setting can achieve similar performance as a uniform ADC with 1–1.5-bit reduction in ADC resolution.

In Fig. 26(a), a strong pre-filtering is applied to over-equalize the channel so that the pulse response has substantial 1st to 4th post-cursor ISIs with distinct values. In this case, the non-uniform ADC reference continues to outperform the uniform ADC and reduced-FSR ADC, but it has no performance gain over the receiver with loop-unrolled DFE. It is because the post-cursor ISIs have very distinct values and their distribution did not result in some overlaps among the possible ISI offsets to allow non-uniform reference setting to save comparators for the same BER performance. The above three cases illustrates the dependence on the channel characteristics and the performance benefits of a receiver with non-uniform reference ADC.

The extra comparator in the ADC and the auxiliary digital DFE path can perform the pseudo-BER detection for voltage margin measurement. By changing its sampling phase, the effective eye-diagram seen by the DFE can be constructed by measuring the BER as a function of voltage and timing offsets. Fig. 27 plots the effective eye diagrams measured for different receiver configurations with 4 comparators. As expected, the non-uniform ADC reference receiver achieves the largest eye opening.

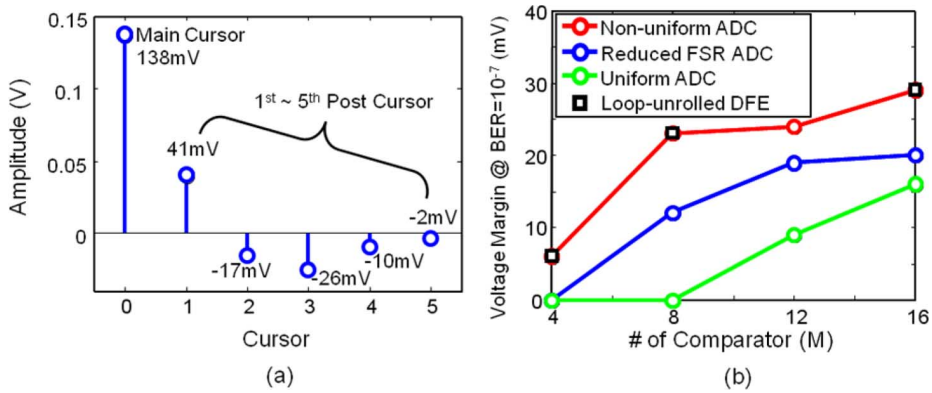


Fig. 26. (a) The channel response for the measurements, and (b) the voltage margin versus the number of comparator with different ADC-based receiver configurations. The non-uniform reference ADC has same performance as loop-unrolled DFE due to distinct ISI values.

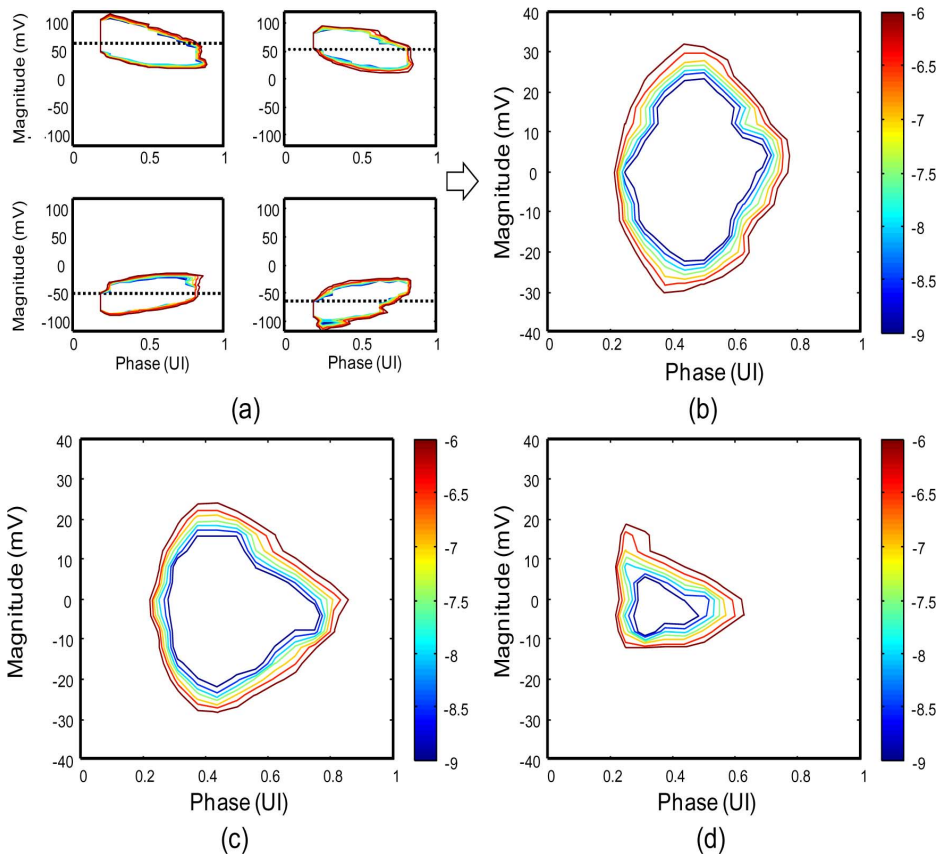


Fig. 27. Measured eye diagrams of a 4-comparator ADC receivers: (a) the partial response eye diagrams of the individual 4 comparators; the effective eye diagrams of (b) non-uniform ADC reference, (c) reduced-FSR ADC, and (d) uniform quantization ADC.

C. Baud-Rate Timing Recovery Experimental Results

The on-chip data transitions are measured to demonstrate the feasibility of the baud-rate timing recovery. Fig. 28(a) shows the measured "101" and "100" data patterns with 1st pre-cursor ISI cancelled by sampled FIR in a 17 dB loss channel. The reference offset of the extra comparator used for the timing recovery is also shown in the figure. The clock phase is designed to move forward or backward according to the probabilities of the two data transitions with respect to this threshold level. The proposed timing recovery would lock at the phase where 1st pre-cursor ISI is zero and it is near the peak of main cursor in this case because the 1st pre-cursor is already cancelled. For the link setting in Fig. 28(b), the system locks at an earlier phase because a large 1st pre-cursor ISI exists.

D. Performance Comparison

The proposed receiver operates at 10 Gb/s data rate and consumes 130 mW in 1.1 V supply. It can equalize a 29 dB loss channel with less than 10^{-12} BER in the optimum setting with 16 comparators in the ADC. The power breakdown is shown in Fig. 29. It is noteworthy that the sum of ADC and DSP power are almost 70% of total power and they are both expected to be reduced with the technology scaling.

Table I summarizes the power and performance of proposed ADC-based receiver along with other high-speed serial link receivers published recently. The power efficiency of proposed receiver is 13 pJ/bit for a 29 dB loss channel. Because the performance of non-uniform ADC reference is channel dependent, in some channels the receiver only requires a lower resolution

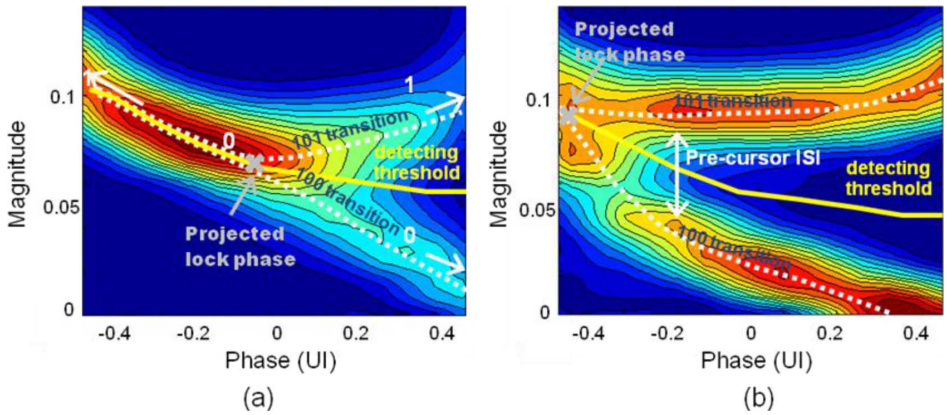


Fig. 28. Measured data transition while (a) the 1st pre-cursor ISI is cancelled, and (b) the 1st pre-cursor ISI is uncompensated. The baud-rate timing recovery would lock at the phase with zero 1st pre-cursor ISI.

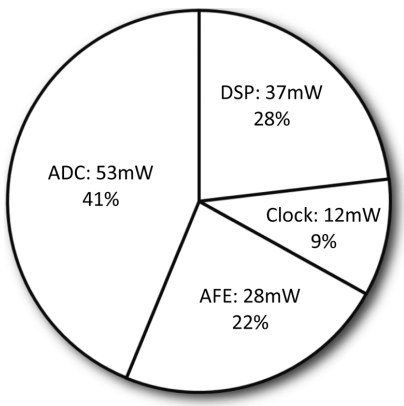


Fig. 29. Receiver power breakdown.

TABLE I
PERFORMANCE COMPARISON OF HIGH-SPEED SERIAL LINK RECEIVERS

	ADC-based				Mixed-mode		
	This work	Harwood '07 [6]	Cao '09 [7]	Yamaguchi '10 [25]	Hidaka '11 [9]	Joy '11 [10]	Quan '11 [11]
Technology	**65nm**	65nm	65nm	65nm	90nm	40nm	40nm
Data Rate (Gb/s)	**10**	12.5 (-15dB) 7.5 (-24dB)	10	5	12.5	16	14.025
Rx Power (mW)	**130**	~230	~400 (exclude DSP)	~180	156	~150	~260
Power Efficiency (pJ/bit)	**13 (-29dB)** **10.6 (-23dB)**	18.4 (-15dB*) 30.7 (-24dB*)	40 (-26dB*)	36 (-15dB)	12.5 (-35dB*)	9.4 (-34dB*)	18.5 (-26dB*)

* with both Tx and Rx EQ

ADC to achieve similar performance; hence, the unused comparators can be turned off to save the power. The measurement results show that only 8 comparators are needed for the non-uniform reference ADC to equalize a 23 dB loss channel. The power efficiency for this link improves to 10.6 pJ/bit. This number is the lowest among other ADC-based receiver and is comparable to those serial link receivers using mixed-mode approach. Note that the equalization capabilities of those publications in Table I include both Tx and Rx equalization (except [25]) and a 3 or 4-tap Tx-FIR can effectively achieves 10–15 dB equalization. It implies when cooperating with transmitter equalization, the proposed receiver is a suitable solution for a higher-loss (>35 dB) serial link application, and its power performance also makes such ADC-based approach a viable solution for the next generation serial link receivers.

V. CONCLUSION

This paper describes the design and measurements from a hybrid architecture ADC-based receiver for serial link application. The low-gain AFE dramatically reduces the requirement of ADC and digital post processing, and also allows scalability for both data rate and technology. The non-uniform ADC reference setting adapted according to the channel response shows substantial improvement in comparison to traditional uniform reference ADC enabling reduced number of reference levels and hence lower power dissipation. The receiver is fabricated in a 65 nm CMOS technology and achieves 10 Gb/s data rate in 1.1 V supply. While the performance improvement of non-uniform reference ADC strongly depends on the channel pulse response, the receiver shows improved power performance across a wide range of channels achieving 13 pJ/bit and 10.6 pJ/bit power efficiency in a 29 dB and 23 dB loss channel respectively.

REFERENCES

[1] J. Poulton, R. Palmer, A. M. Fuller, T. Greer, J. Eyles, W. J. Dally, and M. Horowitz, "A 14-mW 6.25-Gb/s transceiver in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2745–2757, Dec. 2007.

[2] M. Ramezani, M. Abdalla, A. Shoval, M. Van Ierssel, A. Rezayee, A. McLaren, C. Holdenried, J. Pham, E. So, D. Cassan, and S. Sadr, "An 8.4 mW/Gb/s 4-lane 48 Gb/s multi-standard-compliant transceiver in 40 nm digital CMOS technology," in *IEEE Int. Solid-State Circuits Conf. Digest of Tech. Papers (ISSCC)*, Feb. 20–24, 2011, pp. 352–354.

[3] G. Balamurugan, J. Kennedy, G. Banerjee, J. E. Jaussi, M. Mansuri, F. O'Mahony, B. Casper, and R. Mooney, "A scalable 5–15 Gbps, 14–75 mW low-power I/O transceiver in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 43, no. 4, pp. 1010–1019, Apr. 2008.

[4] A. Momtaz and M. M. Green, "An 80 mW 40 Gb/s 7-tap T/2-spaced feed-forward equalizer in 65 nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 3, pp. 629–639, Mar. 2010.

[5] M.-S. Chen, Y.-N. Shih, C.-L. Lin, H.-W. Hung, and J. Lee, "A 40 Gb/s TX and RX chip set in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. Digest of Tech. Papers (ISSCC)*, Feb. 20–24, 2011, pp. 146–148.

[6] M. Harwood, N. Warke, R. Simpson, T. Leslie, A. Amerasekera, S. Batty, D. Colman, E. Carr, V. Gopinathan, S. Hubbins, P. Hunt, A. Joy, P. Khandelwal, B. Killips, T. Krause, S. Lytollis, A. Pickering, M. Saxton, D. Sebastio, G. Swanson, A. Szczepanek, T. Ward, J. Williams, R. Williams, and T. Willwerth, "A 12.5 Gb/s SerDes in 65 nm CMOS using a baud-rate ADC with digital receiver equalization and clock recovery," in *IEEE Int. Solid-State Circuits Conf. Digest of Tech. Papers*, 2007, pp. 436–591.

[7] J. Cao, B. Zhang, U. Singh, D. Cui, A. Vasani, A. Garg, W. Zhang, N. Kocaman, D. Pi, B. Raghavan, H. Pan, I. Fujimori, and A. Momtaz, "A 500 mW digitally calibrated AFE in 65 nm CMOS for 10 Gb/s serial links over backplane and multimode fiber," in *IEEE Int. Solid-State Circuits Conf.—Digest of Tech. Papers, ISSCC*, 2009, pp. 370–371.

[8] E.-H. Chen and C.-K. K. Yang, "ADC-based serial I/O receivers," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 57, no. 9, pp. 2248–2258, Sep. 2010.

[9] Y. Hidaka, T. Horie, Y. Koyanagi, T. Miyoshi, H. Osone, S. Parikh, S. Reddy, T. Shibuya, Y. Umezawa, and W. W. Walker, "A 4-channel 10.3 Gb/s transceiver with adaptive phase equalizer for 4-to-41 dB loss PCB channel," in *IEEE Int. Solid-State Circuits Conf. Digest of Tech. Papers, ISSCC*, Feb. 20–24, 2011, pp. 346–348.

[10] A. K. Joy, H. Mair, H.-C. Lee, A. Feldman, C. Portmann, N. Bulman, E. C. Crespo, P. Hearne, P. Huang, B. Kerr, P. Khandelwal, F. Kuhlmann, S. Lytollis, J. Machado, C. Morrison, S. Morrison, S. Rabii, D. Rajapaksha, V. Ravinuthula, and G. Surace, "Analog-DFE-based 16 Gb/s SerDes in 40 nm CMOS that operates across 34 dB loss channels at Nyquist with a baud rate CDR and 1.2 vpp voltage-mode driver," in *IEEE Int. Solid-State Circuits Conf. Digest of Tech. Papers, ISSCC*, Feb. 20–24, 2011, pp. 350–351.

[11] S. Quan, F. Zhong, W. Liu, P. Aziz, T. Jing, J. Dong, C. Desai, H. Gao, M. Garcia, G. Hom, T. Huynh, H. Kimura, R. Kothari, L. Li, C. Liu, S. Lowrie, K. Ling, A. Malipatil, R. Narayan, T. Prokop, C. Palusa, A. Rajashekara, A. Sinha, C. Zhong, and E. Zhang, "A 1.0625-to-14.025 Gb/s multimedia transceiver with full-rate source-series-terminated transmit driver and floating-tap decision-feedback equalizer in 40 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. Digest of Tech. Papers (ISSCC)*, Feb. 20–24, 2011, pp. 348–350.

[12] O. E. Agazzi, M. R. Hueda, D. E. Crivelli, H. S. Carrer, A. Nazemi, G. Luna, F. Ramos, R. Lopez, C. Grace, B. Kobeissy, C. Abidin, M. Kazemi, M. Kargar, C. Marquez, S. Ramprasad, F. Bollo, V. Posse, S. Wang, G. Asmanis, G. Eaton, N. Swenson, T. Lindsay, and P. Voois, "A 90 nm CMOS DSP MLSD transceiver with integrated AFE for electronic dispersion compensation of multimode optical fibers at 10 Gb/s," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2939–2957, Dec. 2008.

[13] J. E. Jaussi, G. Balamurugan, D. R. Johnson, B. Casper, A. Martin, J. Kennedy, N. Shanbhag, and R. Mooney, "8-Gb/s source-synchronous I/O link with adaptive receiver equalization, offset cancellation, and clock de-skew," *IEEE J. Solid-State Circuits*, vol. 40, no. 1, pp. 80–88, Jan. 2005.

[14] T. A. Ali, A. A. Hafez, R. Drost, R. Ho, and C.-K. K. Yang, "A 4.6 GHz MDLL with -46 dBc reference spur and aperture position tuning," in *IEEE Int. Solid-State Circuits Conf. Digest of Tech. Papers (ISSCC)*, Feb. 20–24, 2011, pp. 466–468.

[15] E.-H. Chen, J. Ren, B. Leibowitz, H.-C. Lee, Q. Lin, K. Oh, F. Lambrecht, V. Stojanovic, J. Zerbe, and C.-K. K. Yang, "Near-optimal equalizer and timing adaptation for I/O links using a BER-based metric," *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 2144–2156, Sep. 2008.

[16] E.-H. Chen, W. Leven, N. Warke, A. Joy, S. Hubbins, A. Amerasekera, and C.-K. K. Yang, "Adaptation of CDR and full scale range of ADC-based SerDes receiver," in *Proc. Symp. on VLSI Circuits*, 2009, pp. 12–13.

[17] O. E. Agazzi, M. R. Hueda, D. E. Crivelli, H. S. Carrer, A. Nazemi, G. Luna, F. Ramos, R. Lopez, C. Grace, B. Kobeissy, C. Abidin, M. Kazemi, M. Kargar, C. Marquez, S. Ramprasad, F. Bollo, V. Posse, S. Wang, G. Asmanis, G. Eaton, N. Swenson, T. Lindsay, and P. Voois, "A 90 nm CMOS DSP MLSD transceiver with integrated AFE for electronic dispersion compensation of multimode optical fibers at 10 Gb/s," *IEEE J. Solid-State Circuits*, vol. 43, no. 12, pp. 2939–2957, Dec. 2008.

[18] H. Chung and G.-Y. Wei, "Design-space exploration of backplane receivers with high-speed ADCs and digital equalization," in *IEEE Custom Integrated Circuits Conf., CICC'09*, 2009, pp. 555–558.

[19] S. Kasturia and J. H. Winters, "Techniques for high-speed implementation of nonlinear cancellation," *IEEE J. Sel. Areas Commun.*, vol. 9, no. 5, pp. 711–717, Jun. 1991.

[20] J. Kim, E.-H. Chen, J. Ren, B. S. Leibowitz, P. Satarzadeh, J. L. Zerbe, and C.-K. K. Yang, "Equalizer design and performance trade-offs in ADC-based serial links," *IEEE Trans. Circuits Syst. I: Reg. Papers*, vol. 58, no. 9, pp. 2096–2107, Sep. 2011.

[21] M. Lu, N. Shanbhag, and A. Singer, "BER-optimal analog-to-digital converters for communication links," in *Proc. IEEE Int. Symp. on Circuits and Systems (ISCAS)*, May 30–Jun. 2 2010, pp. 1029–1032.

[22] E. Alpman, H. Lakdawala, L. R. Carley, and K. Soumyanath, "A 1.1 V 50 mW 2.5 GS/s 7b time-interleaved C-2C SAR ADC in 45 nm LP digital CMOS," in *IEEE Int. Solid-State Circuits Conf. Digest of Tech. Papers, ISSCC*, Feb. 8–12, 2009, pp. 76–77, 77a.

[23] J. Montanaro, R. T. Witek, K. Anne, A. J. Black, E. M. Cooper, D. W. Dobberpuhl, P. M. Donahue, J. Eno, W. Hoeppner, D. Kruckemyer, T. H. Lee, P. C. M. Lin, L. Madden, D. Murray, M. H. Pearce, S. Santhanam, K. J. Snyder, R. Stehpany, and S. C. Thierauf, "A 160-MHz, 32-b, 0.5-W CMOS RISC microprocessor," *IEEE J. Solid-State Circuits*, vol. 31, no. 11, pp. 1703–1714, Nov. 1996.

[24] K.-L. J. Wong, E.-H. Chen, and C.-K. K. Yang, "Edge and data adaptive equalization of serial-link transceivers," *IEEE J. Solid-State Circuits*, vol. 43, no. 9, pp. 2157–2169, Sep. 2008.

[25] H. Yamaguchi, H. Tamura, Y. Doi, Y. Tomita, T. Hamada, M. Kibune, S. Ohmoto, K. Tateishi, O. Tyschenko, A. Sheikholeslami, T. Higuchi, J. Ogawa, T. Saito, H. Ishida, and K. Gotoh, "A 5 Gb/s transceiver with an ADC-based feedforward CDR and CMA adaptive equalizer in 65 nm CMOS," in *IEEE Int. Solid-State Circuits Conf. Digest of Tech. Papers, ISSCC*, 2010, pp. 168–169.

[26] E.-H. Chen, R. Yousry, T. Ali, and C.-K. K. Yang, "10 Gb/s serial I/O receiver based on variable reference ADC," in *Proc. Symp. on VLSI Circuits (VLSIC)*, Jun. 15–17, 2011, pp. 288–289.

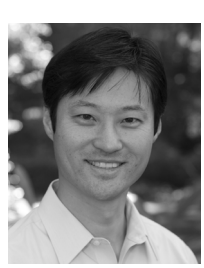
E-Hung Chen (S'05–M'12) was born in Taipei, Taiwan. He received the B.S. degree from National Taiwan University in 2002 and the M.S. and Ph.D. degrees from University of California at Los Angeles (UCLA), in 2008 and 2011, respectively, all in electrical engineering.

During his graduate studies, he held several summer positions at Broadcom Corporation, Rambus Inc. and Texas Instruments working on channel equalization technique and receiver modeling. He joined Rambus Inc., Sunnyvale, CA, in 2011 where he has worked on mixed-signal circuit design and equalization for high-speed serial links and memory interfaces.

Ramy Yousry received the B.Sc. and M.Sc. degrees in electrical engineering from Ain-Shams University, Cairo, Egypt, in 2003 and 2007, respectively. He is currently pursuing the Ph.D. degree in integrated circuits and systems at the University of California, Los Angeles.

His research interests include high-speed analog-to-digital converters for high-speed serial links.

Mr. Yousry is the recipient of a UCLA Fellowship for academic year 2007–08 and Spring 2009.



Chih-Kong Ken Yang (S'94–M'98–SM'07–F'10) was born in Taipei, Taiwan. He received the B.S. and M.S. degrees in 1992 and the Ph.D. degree in 1998 from Stanford University, Stanford, CA, all in electrical engineering.

He joined the University of California at Los Angeles as an Assistant Professor in 1999 and has been a Professor since 2009. His current research area is high-performance mixed-mode circuit design for VLSI systems such as clock generation, high-performance signaling, low-power digital functional blocks, and analog-to-digital conversion.