24.1 A 12.5Gb/s SerDes in 65nm CMOS Using a Baud-Rate ADC with Digital Receiver Equalization and Clock Recovery.

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A key challenge in designing high-bandwidth systems such as data-routers and super-computers is to transferring large amounts of data between ICs – either on the same circuit board or between boards. Analysis of typical backplane channel attenuation (-24dB) and package losses (-1 to -2dB) in the presence of crosstalk predict that an un-equalized transceiver provides inadequate performance and that DFE is needed to achieve error rates of <10^{-17}.

Traditional DFE methods for SerDes receivers rely on either modifying the input signal based on the data history [1-3] or on having an adaptive analog slicing level [4]. This paper describes an alternative approach. The input data is sampled at the baud-rate, digitized, and the equalization and CDR are performed using numerical digital processing techniques. This approach enables power/area scaling with process, simplifies production testing, allows integration of a FFE, and provides a flexible design with a configurable number of filter taps. Implemented in 65nm CMOS, the 12.5Gb/s transceiver uses the baud-rate sampling ADC, a RX with digital 2-tap FFE and digital 5-tap DFE to correct channel impairments, and a TX with a 4-tap FIR filter to pre-compensate for channel impairments.

The RX is shown in Fig. 24.1.1. The received data is digitized at the baud-rate, 1.0 to 12.5Gb/s, using a pair of interleaved T/H stages and 23-level (4.5b) full-flash ADCs. The 2 T/H circuits enable interleaving of the half-rate ADCs and reduce signal-related aperture timing errors. Two ADCs, each running at 6.25Gb/s, provide baud-rate quantization of the received data. The dynamic range of the ADC is normalized to the full input amplitude using a 7b AGC circuit. A loss-of-signal indication is obtained by detecting an out-of-range AGC. An optional attenuator is included in the termination block to enable reception of large signals whilst minimizing signal overload.

The detailed full-flash ADC is shown in Fig. 24.1.2(A). The first linear transconductor stage (24.1.2(B)) is optimized for handling large input signals combined with low supply voltages. Resistive interpolation is used to reduce the input DNL. The second CML latch-stage (C) is conventional, but optimized for speed and metastability performance. The final sense-amp latch (D) uses a cross-coupled NMOS pair with PMOS loads. Cross-coupled inverters further enhance the gain and reduce the meta-stability occurrence probability by adding hysteresis.

The output from the ADCs is fed into a custom DSP data-path that performs the numerical FFE and DFE, as shown in Fig. 24.1.3(A). The digital FFE/DFE is implemented using standard library gates. An advantage of digital equalization is that it is straightforward to include FFE as a delay-and-add function without any noise-sensitive analog delay elements. The FFE tap weight is selected to compensate for pre-cursor ISI and can be bypassed to reduce latency. While many standards require pre-cursor de-emphasis at the TX, inclusion at the RX allows improved BER performance with existing legacy transmitters.

The DFE uses an unrolled non-linear cancellation method [4]. The FFE output is compared with a stored slicer-level to generate the data output. The slicer-level is selected from one of 2^n possible options depending on the previous n bits of data. Unrolled tap adaption is performed using an LMS method where the optimum slicing position is defined to be the average of the 2 possible symbol amplitudes (±1) when preceded by identical history bits. Although 5-taps of DFE are chosen for this implementation, this

parameter is scaleable and performance can be traded-off against power consumption and die area. In addition, the digital equalizer can be tested using standard ATPG and circular BIST approaches.

A Mueller-Muller approach [5] is used for clock recovery where the timing function adapts the T/H sample position to the point where the calculated pre-cursor ISI or h(-1) is zero, an example is shown in Fig. 24.1.3(B). The 2 curves show the post-equalized response for 010 and 011 data sequences, respectively. The intersection at 3440ps occurs when the sample of the second bit is independent of the third bit – that is, h(-1) = 0. This position can be detected by comparing the post-equalized symbol amplitude with the theoretical amplitude h(0) and using the difference to update the phase-interpolator of the CDR.

An outline diagram of the TX is shown in Fig. 24.1.4. The data to be transmitted is sequentially delayed to produce a nibble-wide word containing the pre-cursor, cursor, and 2 post-cursor components. These allow a 4-tap FIR output waveform to be obtained from simple current summing of the time-delayed contributions. The relative amplitude of each contribution is weighted to allow the FIR coefficients to be optimized for a given backplane and minimize the overall residual ISI. The line-driver is implemented using CML techniques and operates using 4 interleaved nibbles at 3.125Gb/s to ease timing closure. The 4 line drivers are implemented as a single structure minimizing return-loss.

A PLL is used to generate low-jitter reference clocks for the TX and RX to meet standards [6, 7]. The PLL uses a ring oscillator to produce 4 clock-phases at a quarter of the line data-rate. The lower-speed clocks allow power-efficient clock distribution using CMOS logic levels, but need duty-cycle and quadrature correction at the point of use. The 3.125GHz clocks are frequency doubled (XOR function) to provide the 6.25GHz clock for the T/H and the ADC. The TX uses the 4 separate 3.125GHz phases, but they require accurate alignment to meet jitter specifications of $0.15UI_{pp}$ RJ and $0.15UI_{pp}$ DJ.

The fabricated chip supports error-free operation at 12.5Gb/s over short channels (two 11mm package traces, 30cm low-loss PCB, and 2 connectors). A legacy channel with -24dB of attenuation at 3.75GHz supports error-free operation at 7.5Gb/s. Figure 24.1.5 shows a 12.5Gb/s 2^7-1 PRBS transmitted eye-pattern with 20% de-emphasis on the first post-cursor. The differential amplitude is $700mV_{pp}$ (200mV/div). Figure 24.1.5 also shows the ADC output when a 6.25GHz sine-wave is sampled and the phase between the sine-wave and RX is incremented using a programmable delay-line. The measured codes are within ±1 LSB of the expected values. This level of performance ensures robust operation over a wide range of cables, green-field, and legacy channels. The worst-case power of a single TX/RX pair is 330mW/lane and the total macro area is 0.45mm^2 per lane. A chip-plot of a quad (4-lane) SerDes macro with the key circuit elements identified is shown in Fig. 24.1.6.

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[7] "IEEE Draft 802.3ap/Draft 3.0 – Amendment: Electrical Ethernet Operation over Electrical Backplanes," *IEEE ,* Jul., 2006.
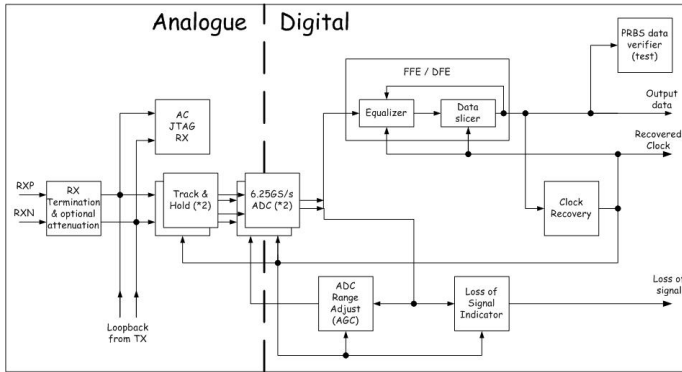
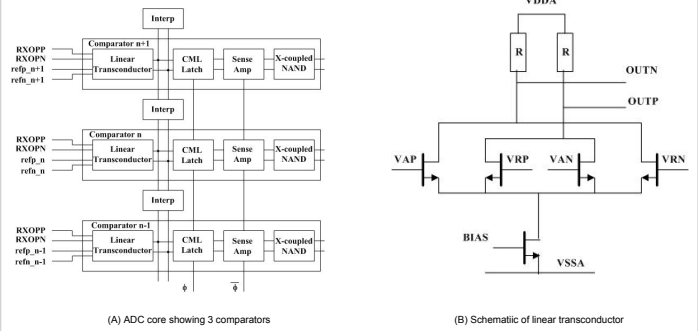**Figure 24.1.1: A 12.5Gb/s receiver with 2 ADCs, a 2-tap FFE and a 5-tap DFE.**

(A) ADC core showing 3 comparators

(B) Schematiic of linear transconductor

Figure 24.1.2: A) Sub-sections of the ADC including 3 comparator sections, and B) the linear transconductor.

(C) Schematic of CML latch

(D) Schematic of sense-amp latch
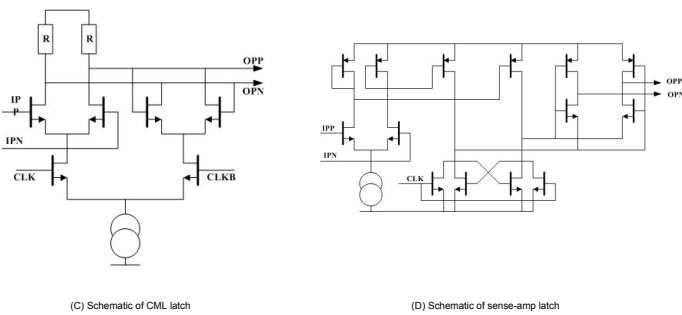
Figure 24.1.2: C) The CML latch and D) the sense-amp latch.

(A) Equalization implementation

(B) Post-equalized signal amplitude
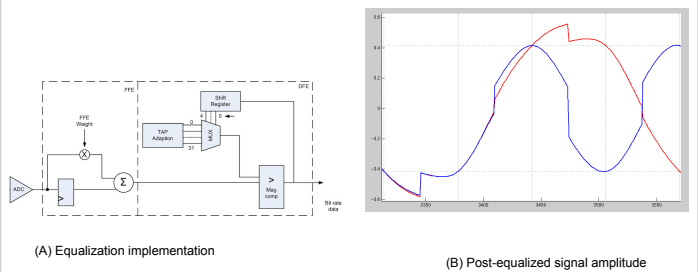
Figure 24.1.3: A) Digital receiver equalizer implementation, B) Post-equalized signal amplitude against time in ps–indicates ideal eye sampling point at 3440ps where h(-1)=0.
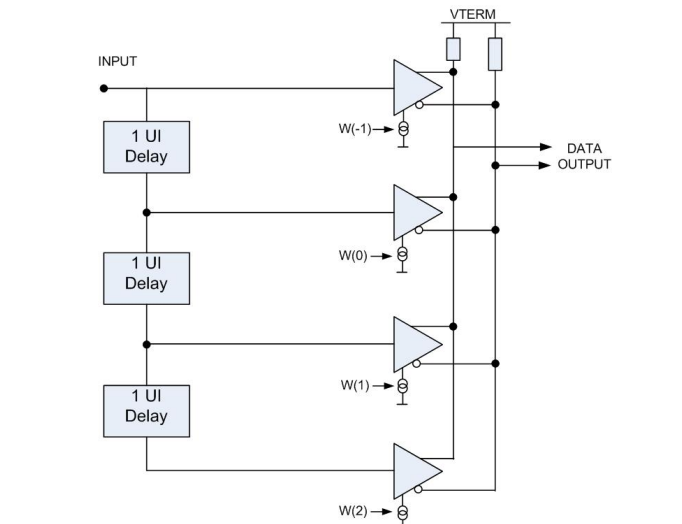

Figure 24.1.4: Transmitter with weighted 4-tap FIR filter and current-summing CML output stage.
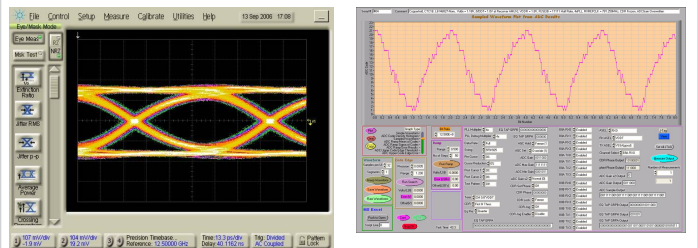

Figure 24.1.5: Lab measurements of the 12.5Gb/s transmitter (vertical scale 200mV/div) – left, and Interleaved ADCs -right.

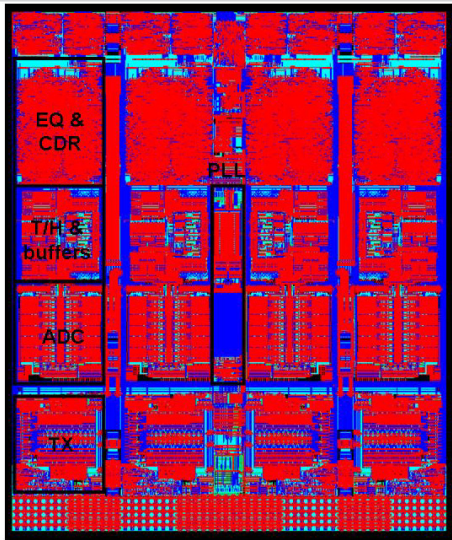*Continued on Page 613*

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Figure 24.1.6: Quad SerDes macro with the key components of a single lane and the central PLL indicated.