12Gb/s Duobinary Signaling with x2 Oversampled Edge Equalization

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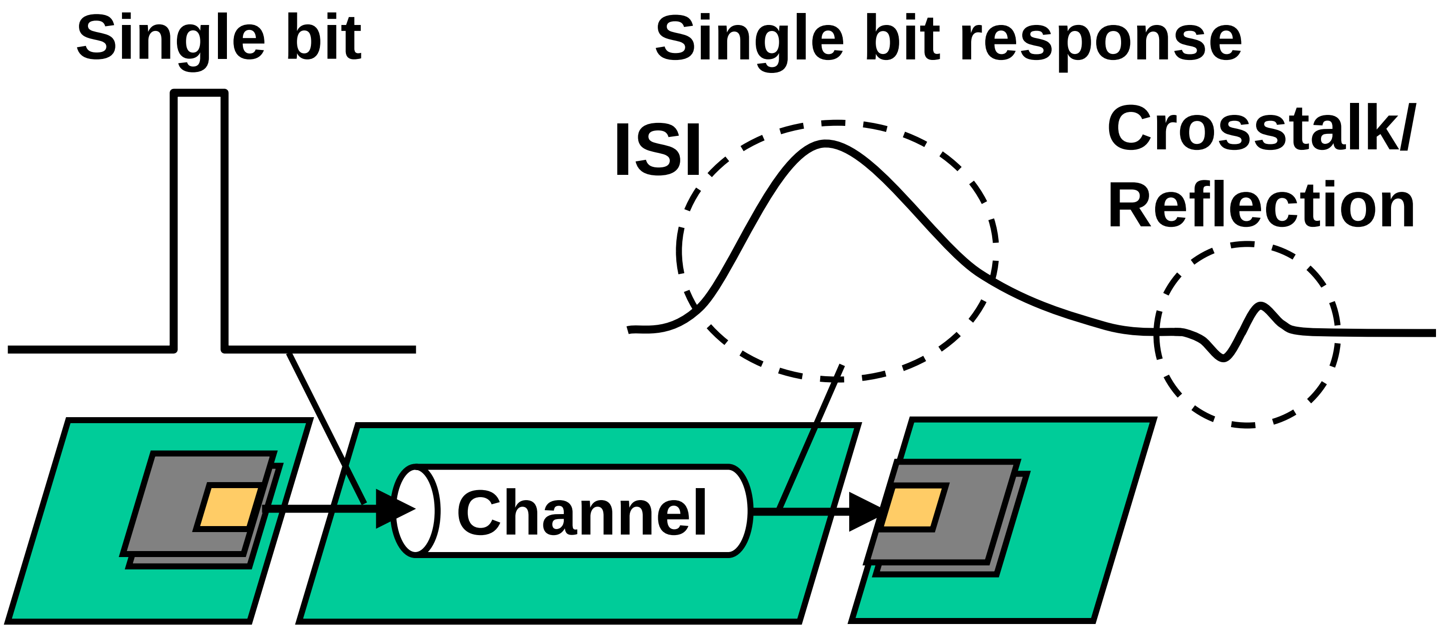
Outline

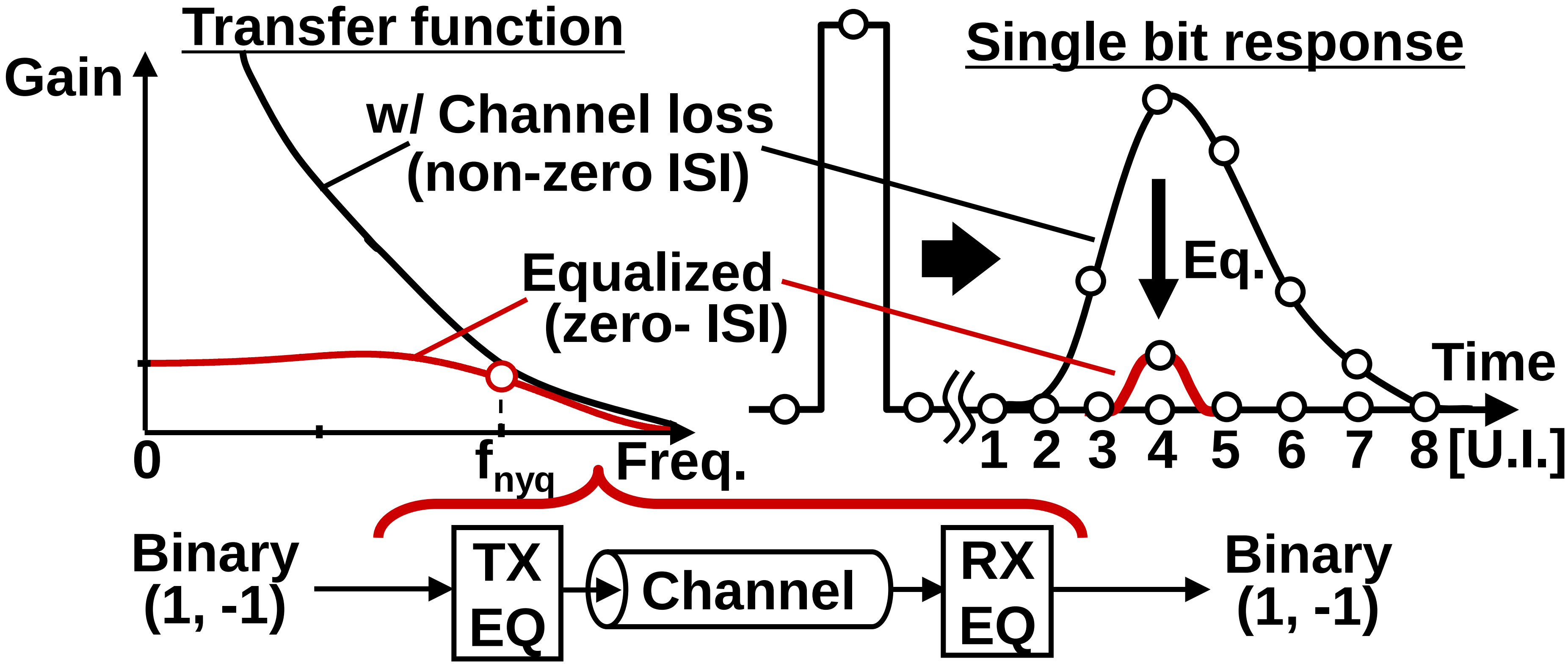
- Background
- Concept
- Developed techniques
- Results of experiments
- Conclusions

Background



- **Increasing demands for high I/O bandwidth**
- **I/O bandwidth is limited by channel distortion**
  - **Intersymbol Interference (ISI), crosstalk/reflection**
- **Channel equalization is a key technique**
  - **Nyquist (zero-ISI) signaling in PAM-2, PAM-4**

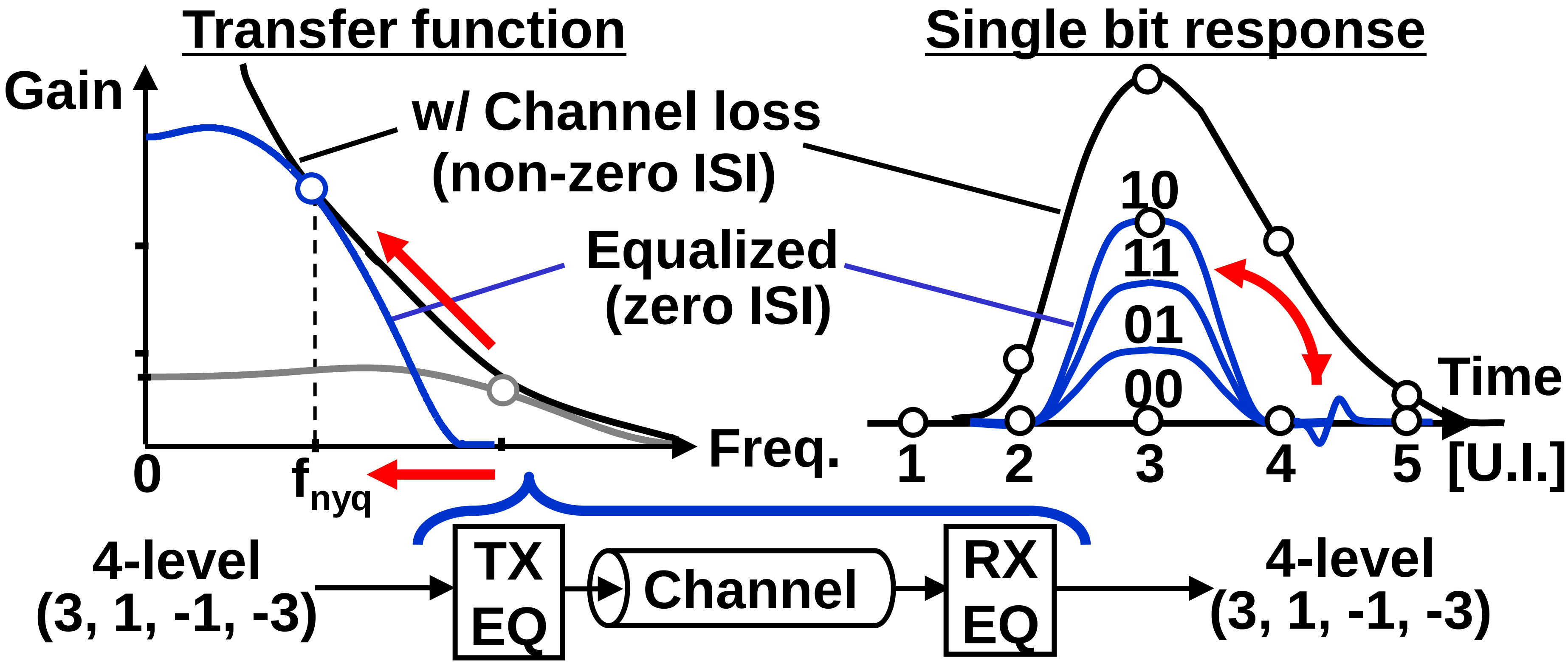
PAM-2 Nyquist Signaling



- Channel loss produces ISI: $1+a_1z^{-1}+a_2z^{-2}+a_3z^{-3}+...$
- Nyquist-freq. bandwidth, zero ISI (a_k=0)

Cons: High Nyquist rate leads to lower eye height
Lower-Nyquist-freq. signaling is required

PAM-4 Nyquist Signaling



- PAM-4 coding halves symbol rate

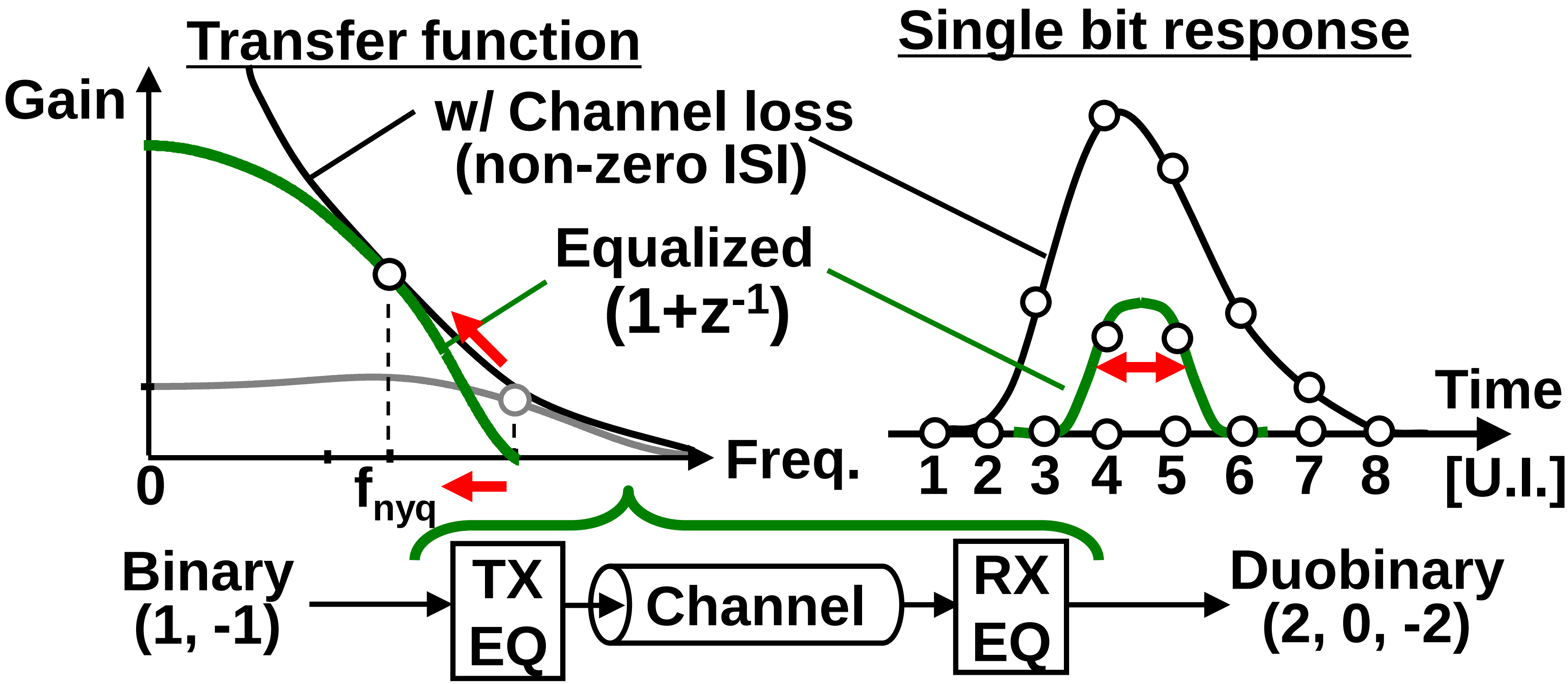
Pros: f_{nyq} = 1/2 of PAM-2 Nyquist-freq. , zero-ISI

Cons: Different symbol rate from PAM-2

9-dB-larger crosstalk sensitivity

–1/3 eye height of maximum transition

Duobinary Signaling



- Duobinary allows controlled amount of ISI: $1+z^{-1}$

Cons: 3 level output: 1+(-1) / -1+(1)=0, 1+(1)=2, -1+(-1)=-2

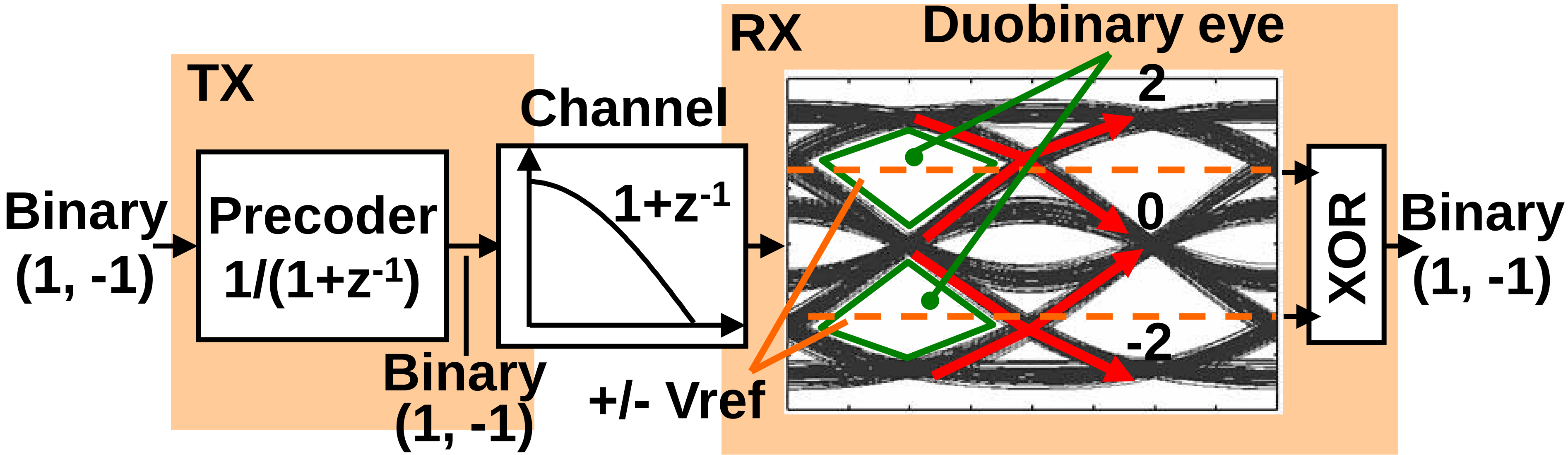
Previous data

Pros: f_{nyq} = 2/3 of PAM-2 Nyquist-freq.

= 4/3 of PAM-4 Nyquist-freq.

Same symbol rate as PAM-2

Duobinary Signaling (cont.)

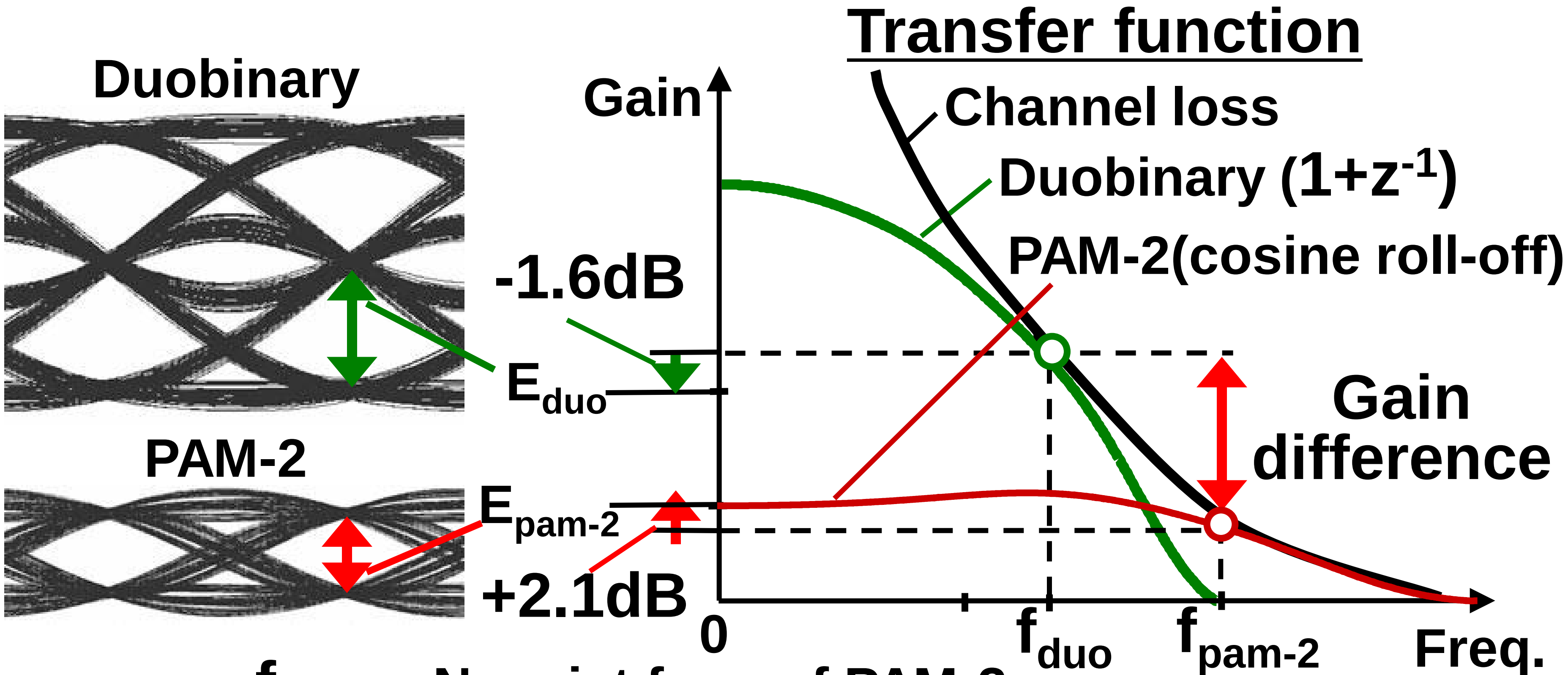


Pros: No enhanced crosstalk sensitivity

–**Duobinary signal includes only adjacent transitions**

- **Duobinary interference ($1+z^{-1}$) is removed by precoder in advance**
  - **Precoder encodes tx data according to $1/(1+z^{-1})$**
  - **No error propagation**
  - **Binary data is recovered at sampling instant**

Eye Height Comparison with PAM-2

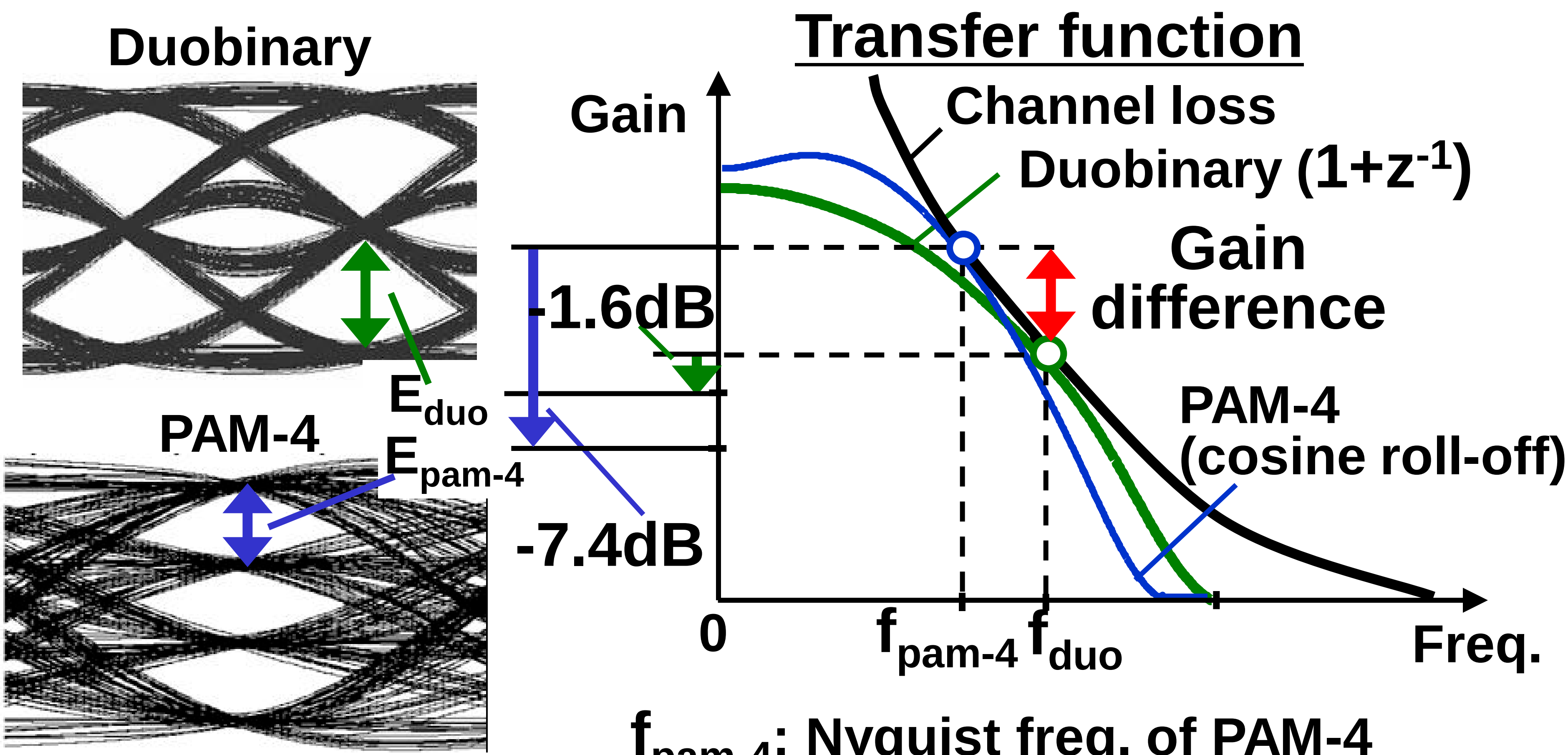


f_{pam-2}: Nyquist freq. of PAM-2

f_{duo}: Nyquist freq. of Duobinary, 2/3* f_{pam-2}

If gain difference is larger than 3.7dB, $E_{duo} > E_{pam-2}$

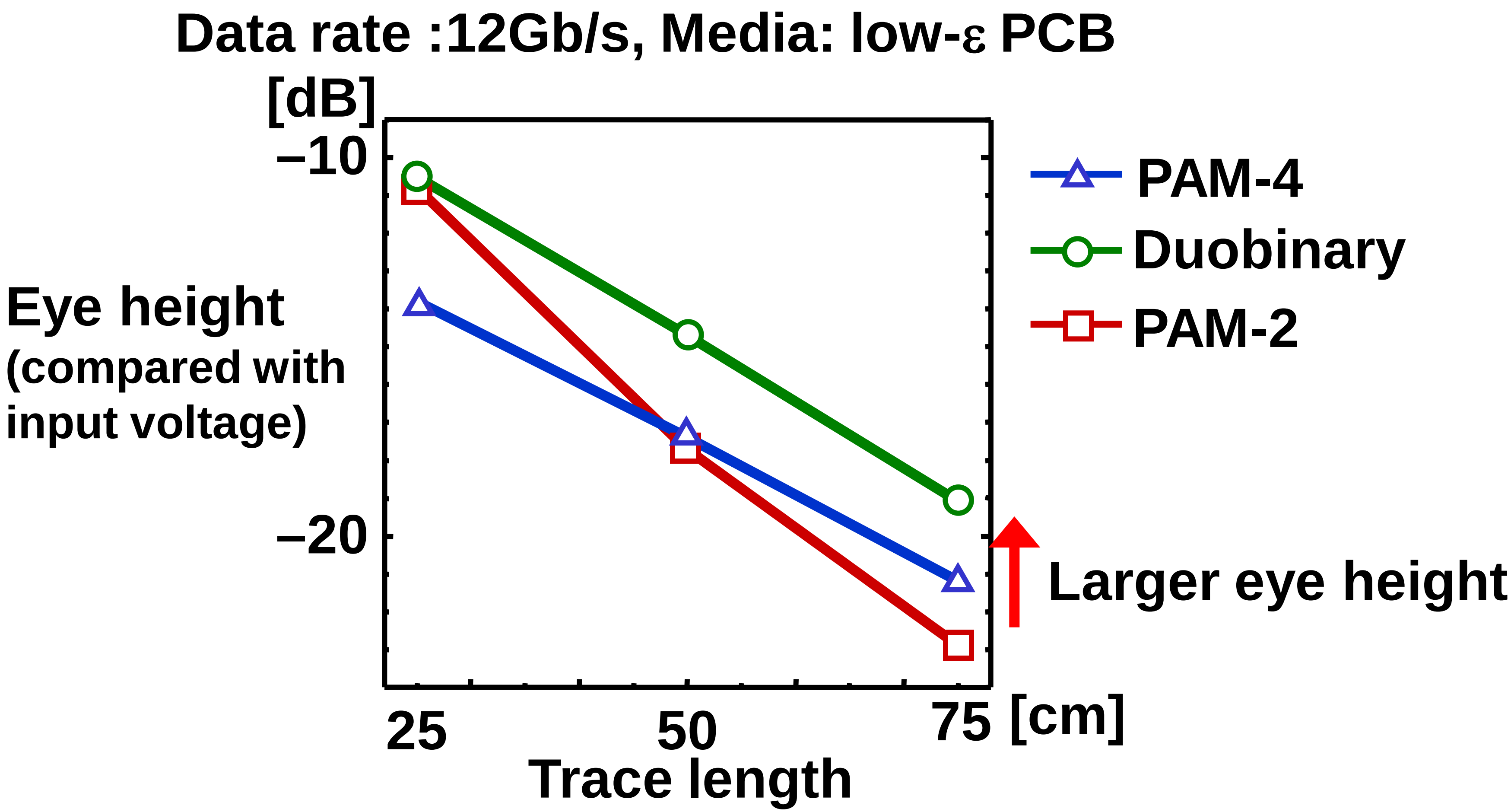
Eye Height Comparison with PAM-4



$f_{pam\text{-}4}$: Nyquist freq. of PAM-4

If gain difference is less than 5.8dB, $E_{duo} > E_{pam\text{-}4}$

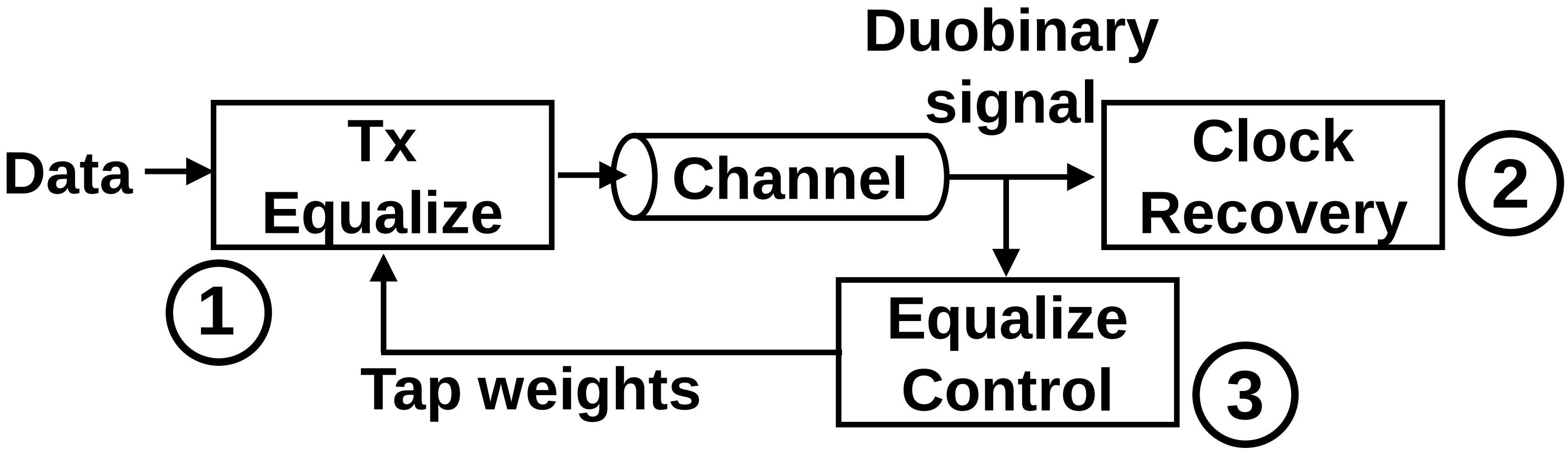
Eye Height Comparison



- Duobinary signaling over 75-cm trace
  – 3.8-dB larger than PAM-2
  – 2.1-dB larger than PAM-4

Development Problems

1. **How can signals be equalized into duobinary?**
   – X2 oversampled equalization
2. **How can clock signals be recovered from duobinary signals?**
   – 2bit-transition-ensured coding
3. **How can equalization be optimized?**
   – Edge equalization



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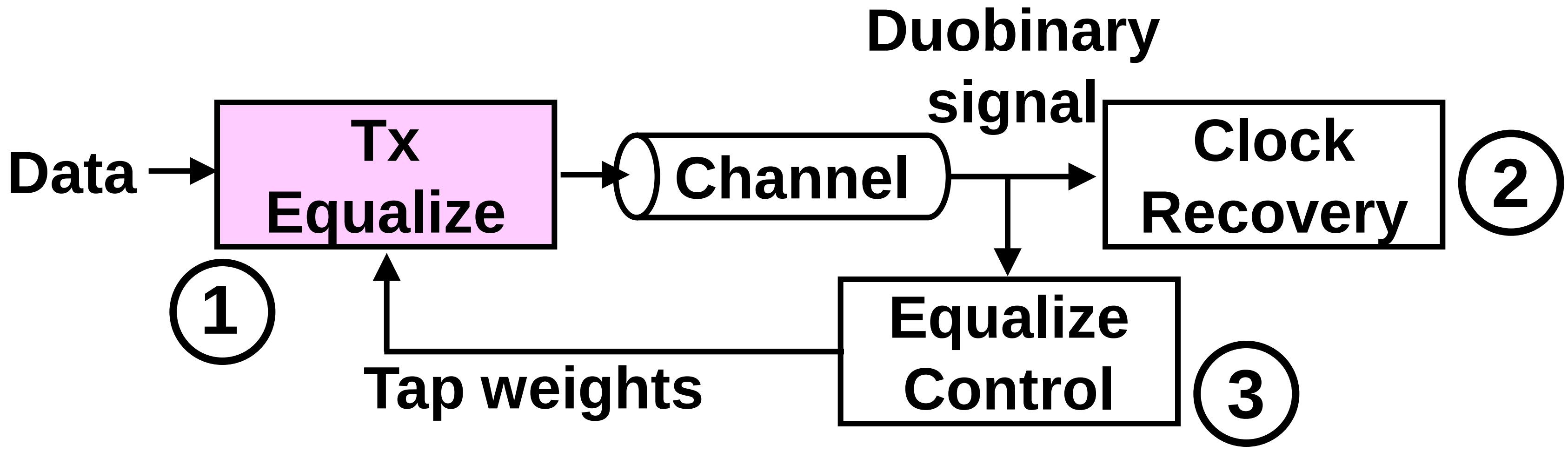
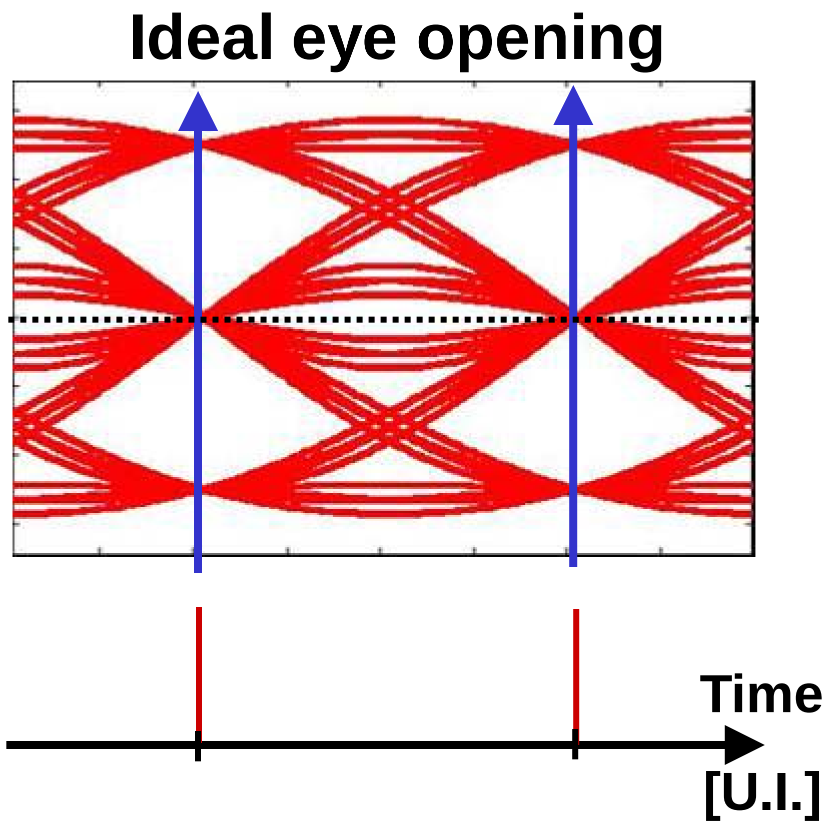
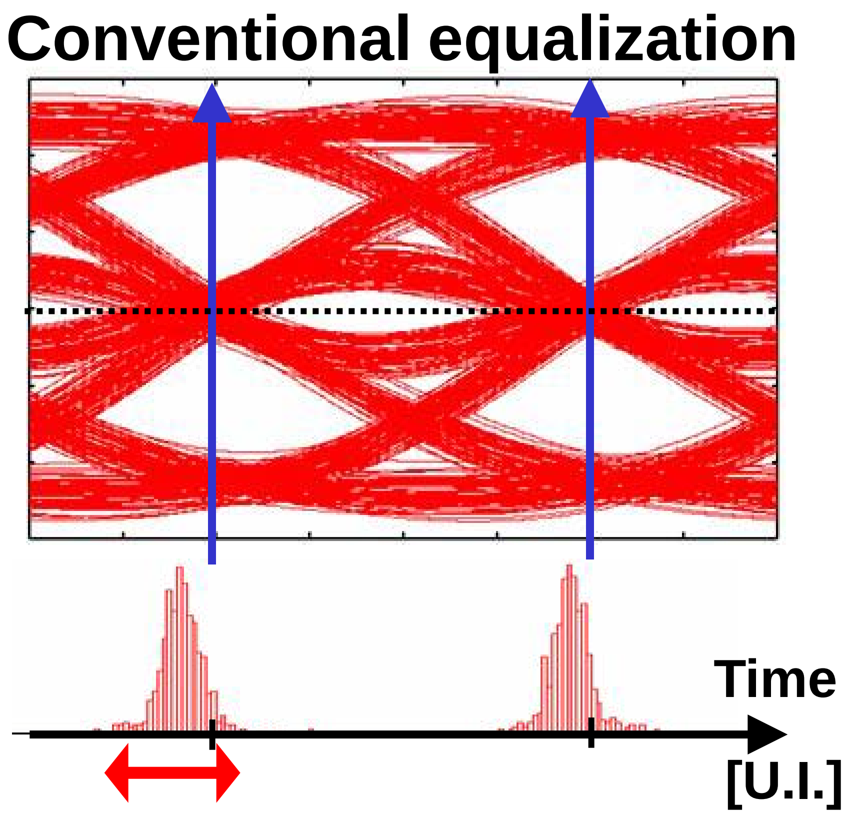


How to Equalize Duobinary Signals?





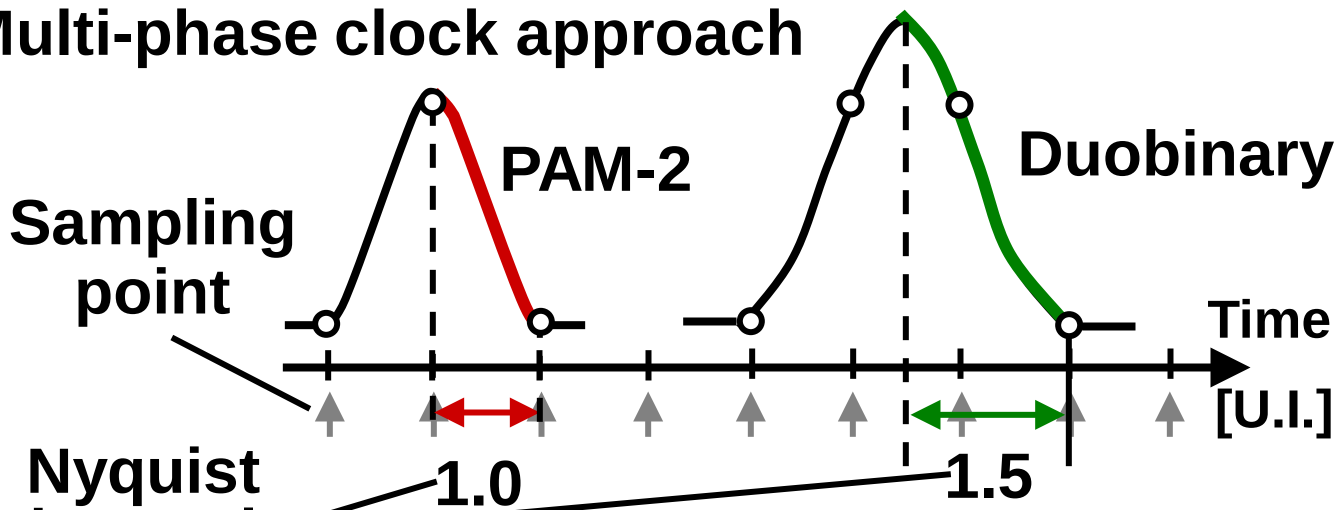
Conventional symbol-rate equalization in duobinary

– **Cannot cancel Nyquist-frequency phase delay**

– **Reduces timing margin**

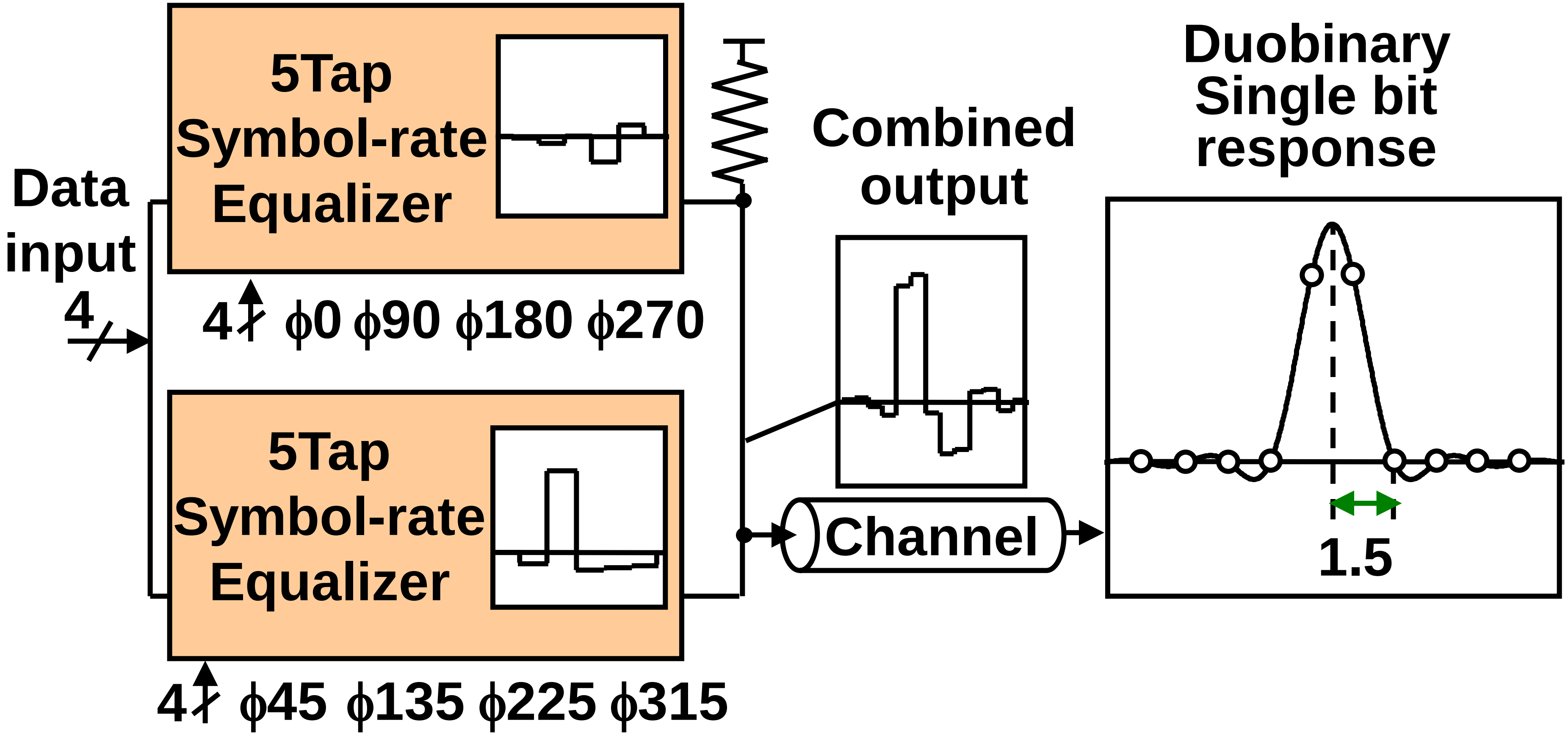
Duobinary Equalization

- Nyquist interval*, $1/(2f_{nyq})$
  - PAM-2/4: 1.0 U.I.
  - Duobinary: 1.5 U.I.
- Equalization
  - PAM-2/4: Symbol-rate
  - Duobinary: Fractional-rate
- X2 oversampled equalizer
  - Multi-phase clock approach



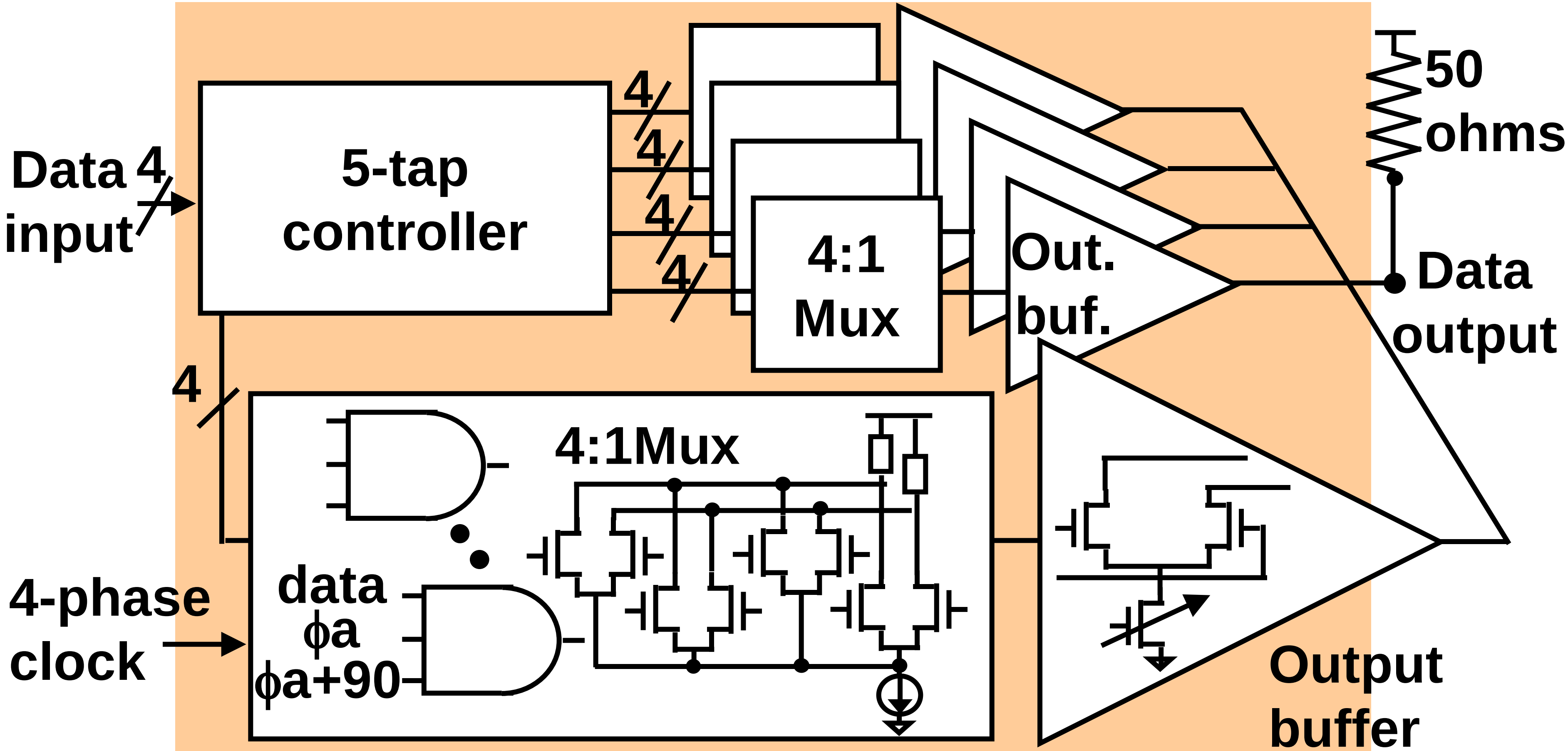
* least transition time in signaling

X2 Oversampled Equalizer



- **Multi-phase clock approach**
  - 12Gb/s signaling by using 3GHz 8phase clock
  - 45 degrees corresponds to 0.5 U.I.

5-tap Symbol-rate Equalizer



- 5-tap controller produces delayed data for each tap
- 4:1MUX by using 4-phase clock
- CML output buffer with variable amplitude

Development Problems

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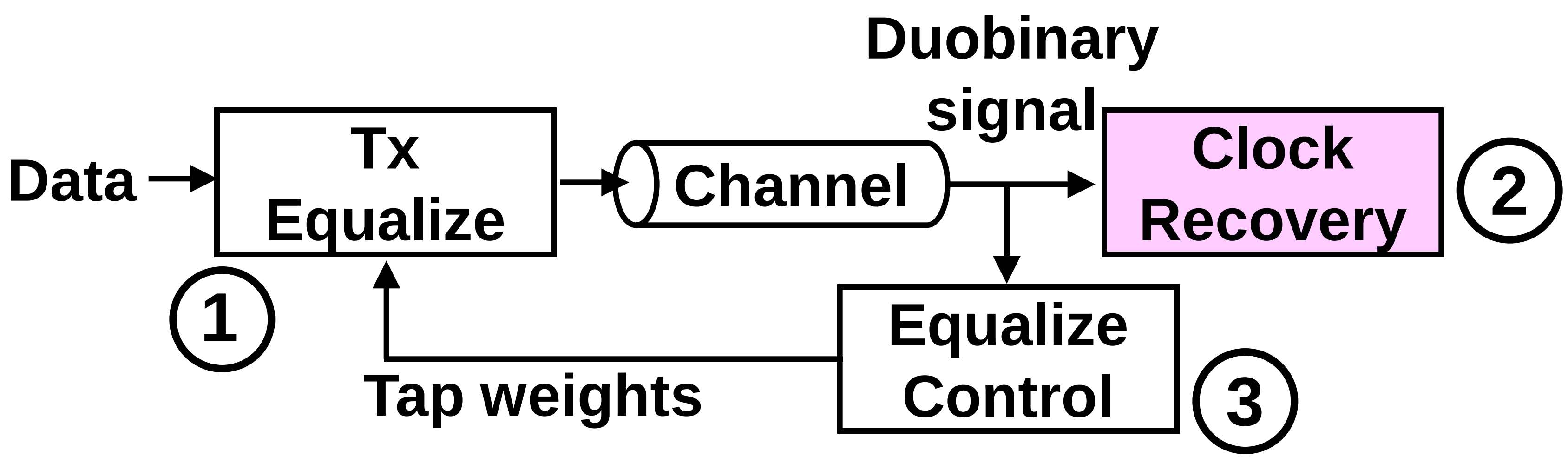
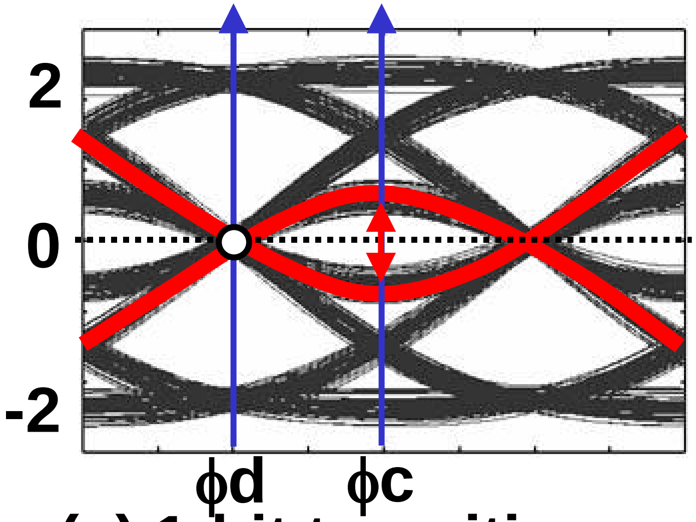
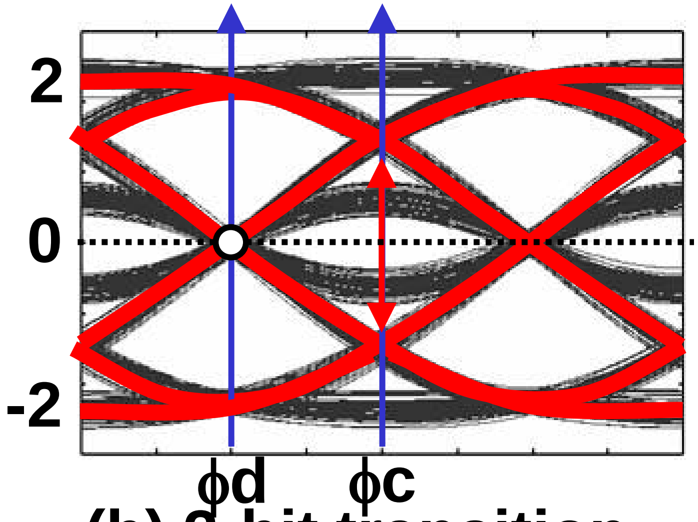


How to Recover Clock from Duobinary?

- **Oversampling clock recovery**
  - **High speed operation**
  - **PAM-2 compatibility**
- **Stable sampling at timing ϕc is required**
  - **1-bit transition (2002 / -200-2): NG,**
  - **2-bit transition (20-2 / -202): <u>has to be ensured</u>**

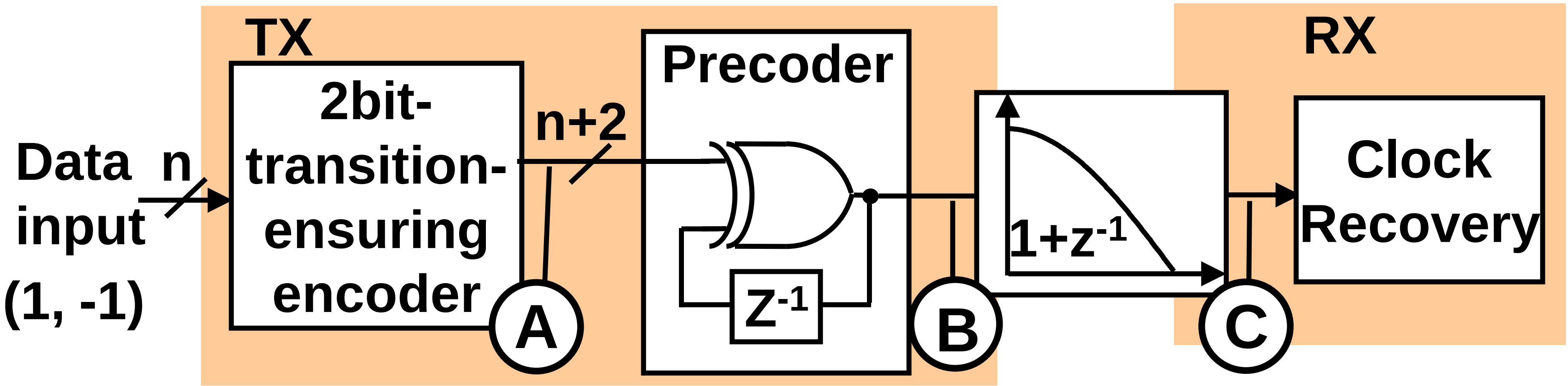


(a) 1-bit transition



(b) 2-bit transition

Ensuring 2-bit Transition

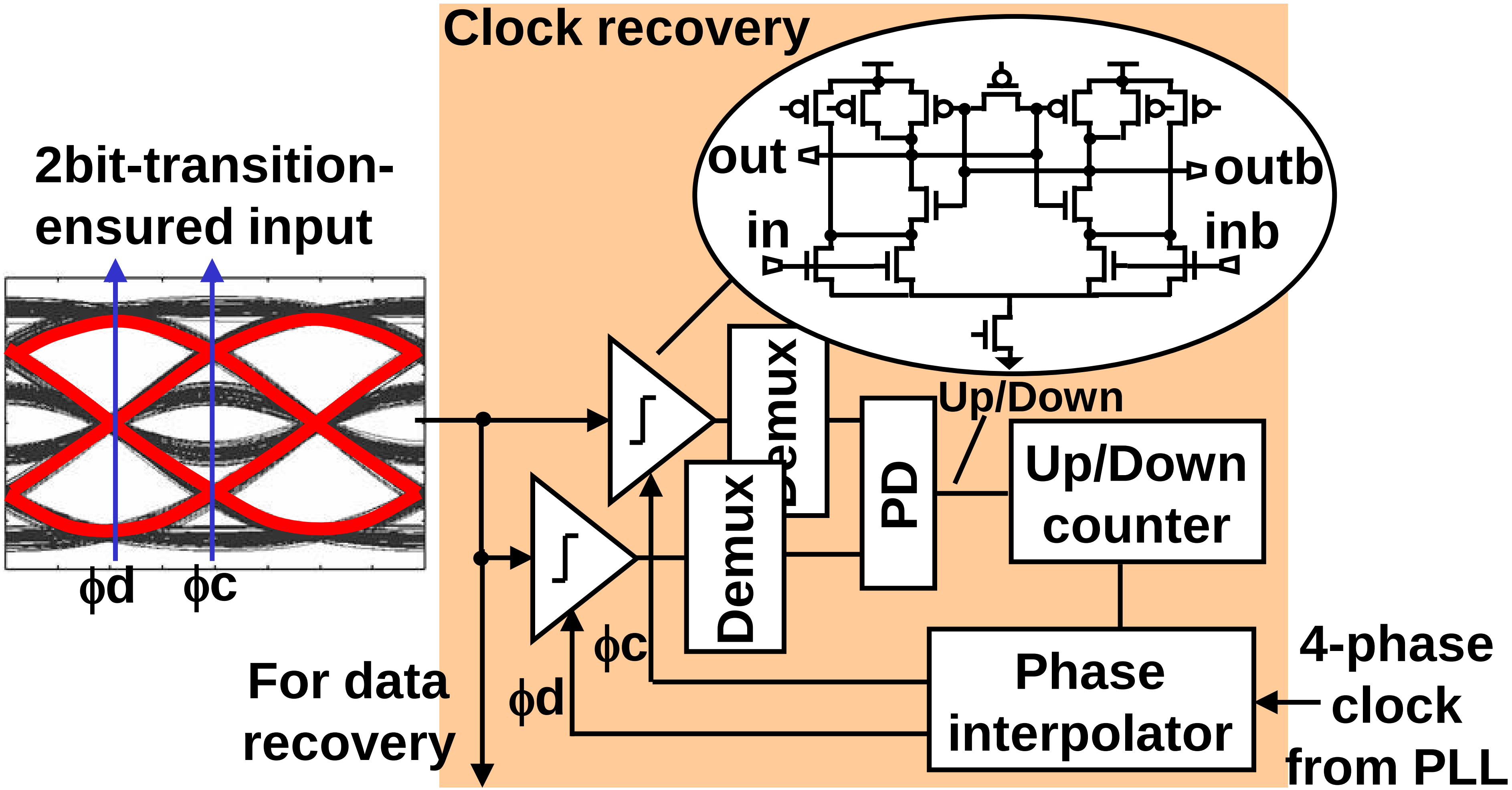


Coding example: Half-rate transition 2-bit transition

LSB[1:0]	Encoded (A)	Precoded (B)	Rx input (C)
-1-1	-1-1 1-1	(-1)-1-111 / (1)11-1-1	-2-202 / 220-2
-1 1	-1 1-1 1	(-1)-111-1 / (1)1-1-11	-2020 / 20-20
1-1	1-1 1-1	(-1)11-1-1 / (1)-1-111	020-2 / 0-202
1 1	-1 1-1-1	(-1)-1111 / (1)1-1-1-1	-2022 / 20-2-2

2-bit transition is ensured by using simple encoding

Clock Recovery in Duobinary Signaling



- Phase-interpolator-based clock recovery is adopted
- Duobinary signal is sampled at ϕd and ϕc

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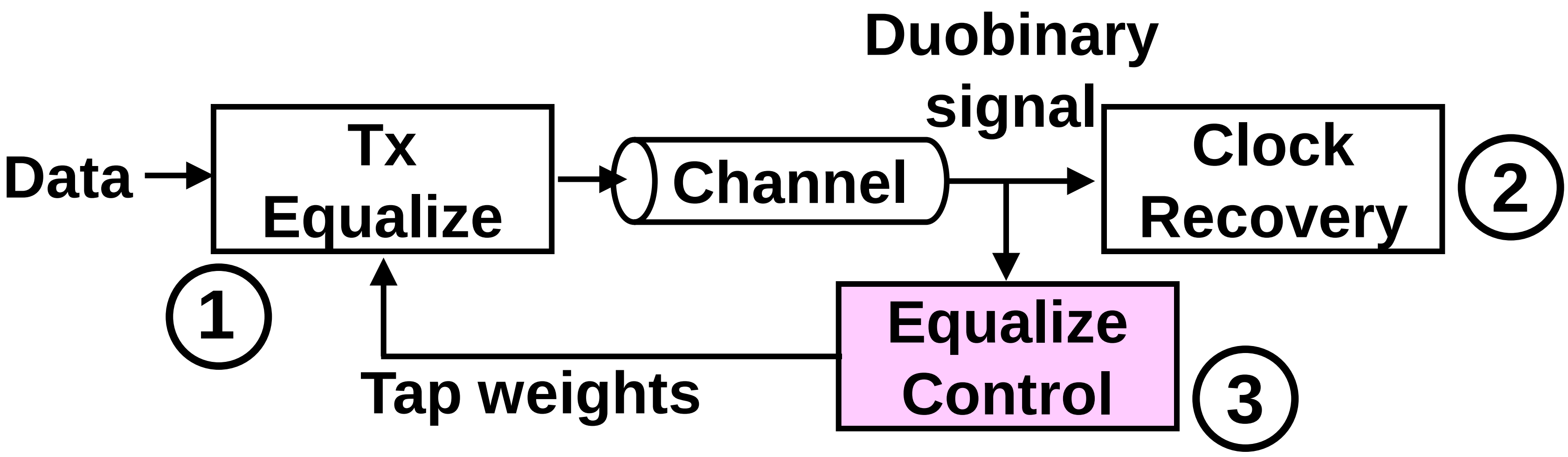
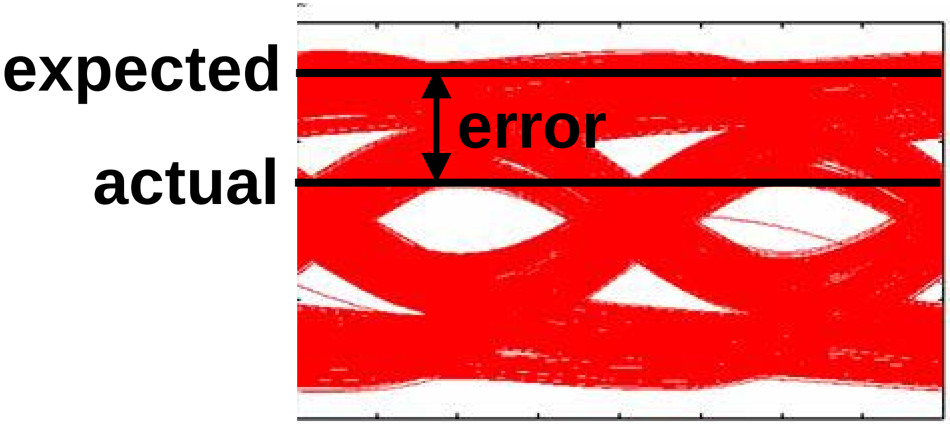


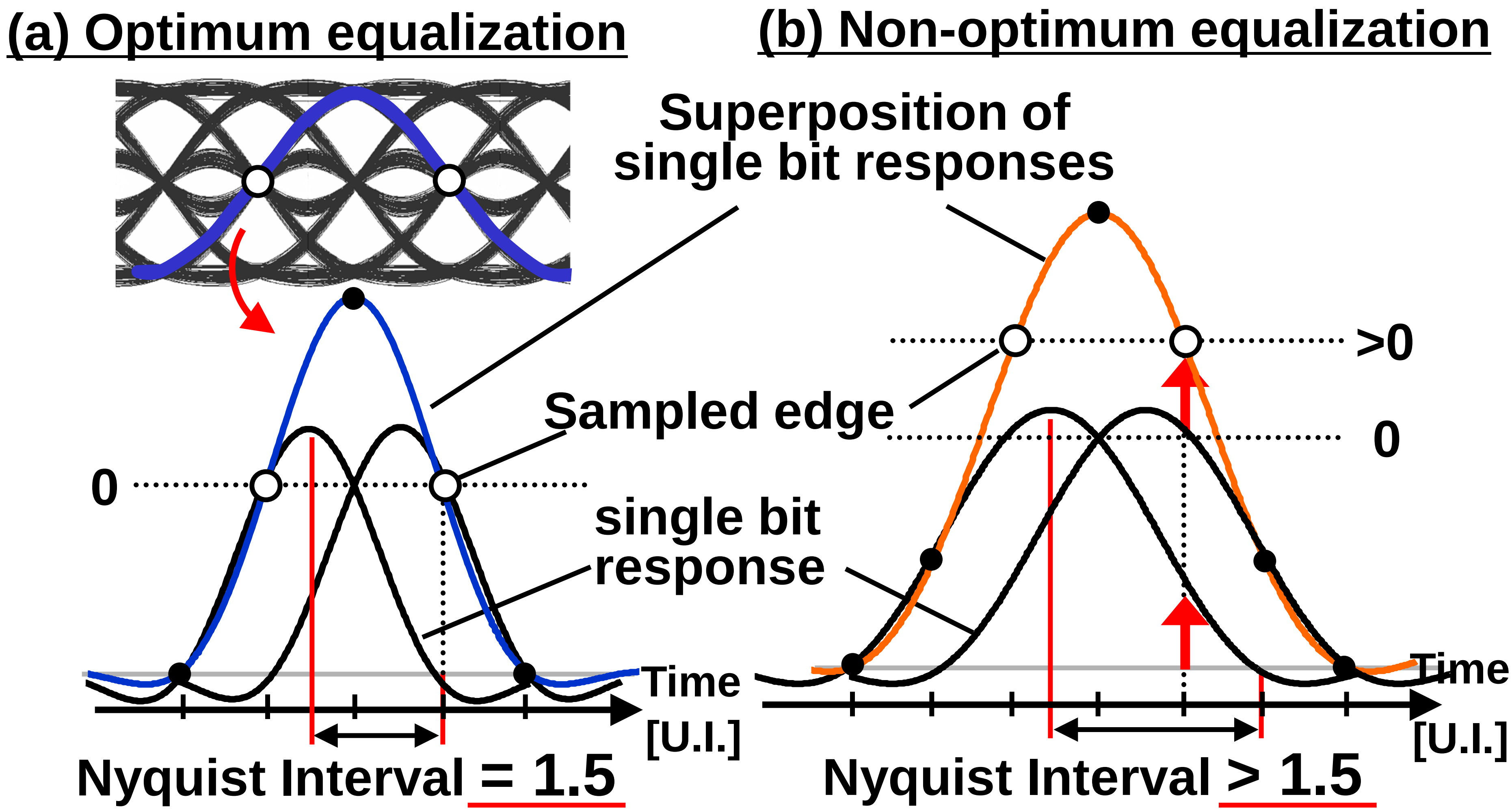
How to Optimize Equalization?

- Equalization error information is required
  - Level comparator
  - Reference voltage (expected amplitude)
- PAM-2
  - 1 reference voltage
  - 1 comparator
- Duobinary
  - 3-leveled signal
- Edge equalization



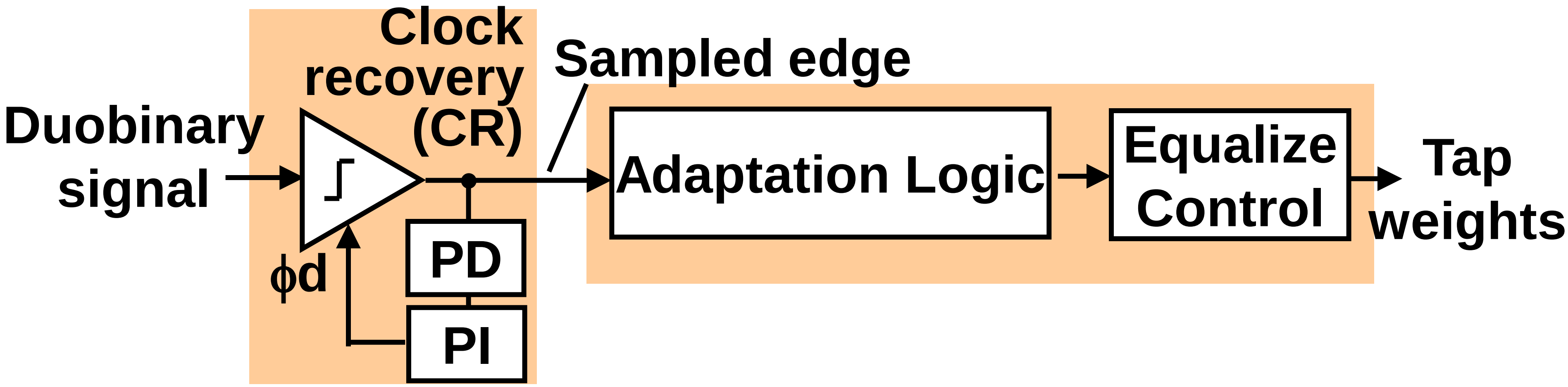
PAM-2 unequalized eye

Edge Equalization

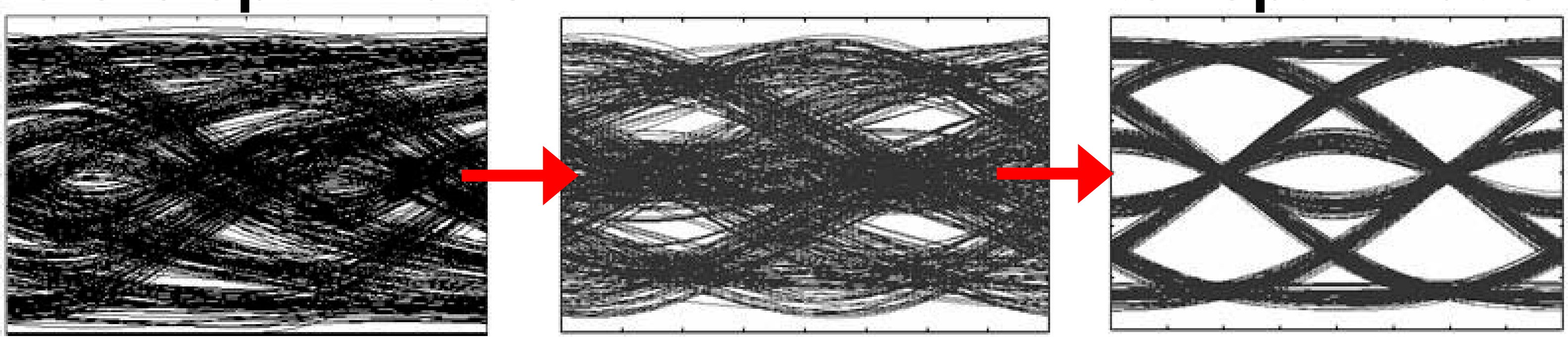


- Non-optimum eq. produces non-zero sampled edge
- Sampled edge can be used as error signal

Edge Equalization (cont.)

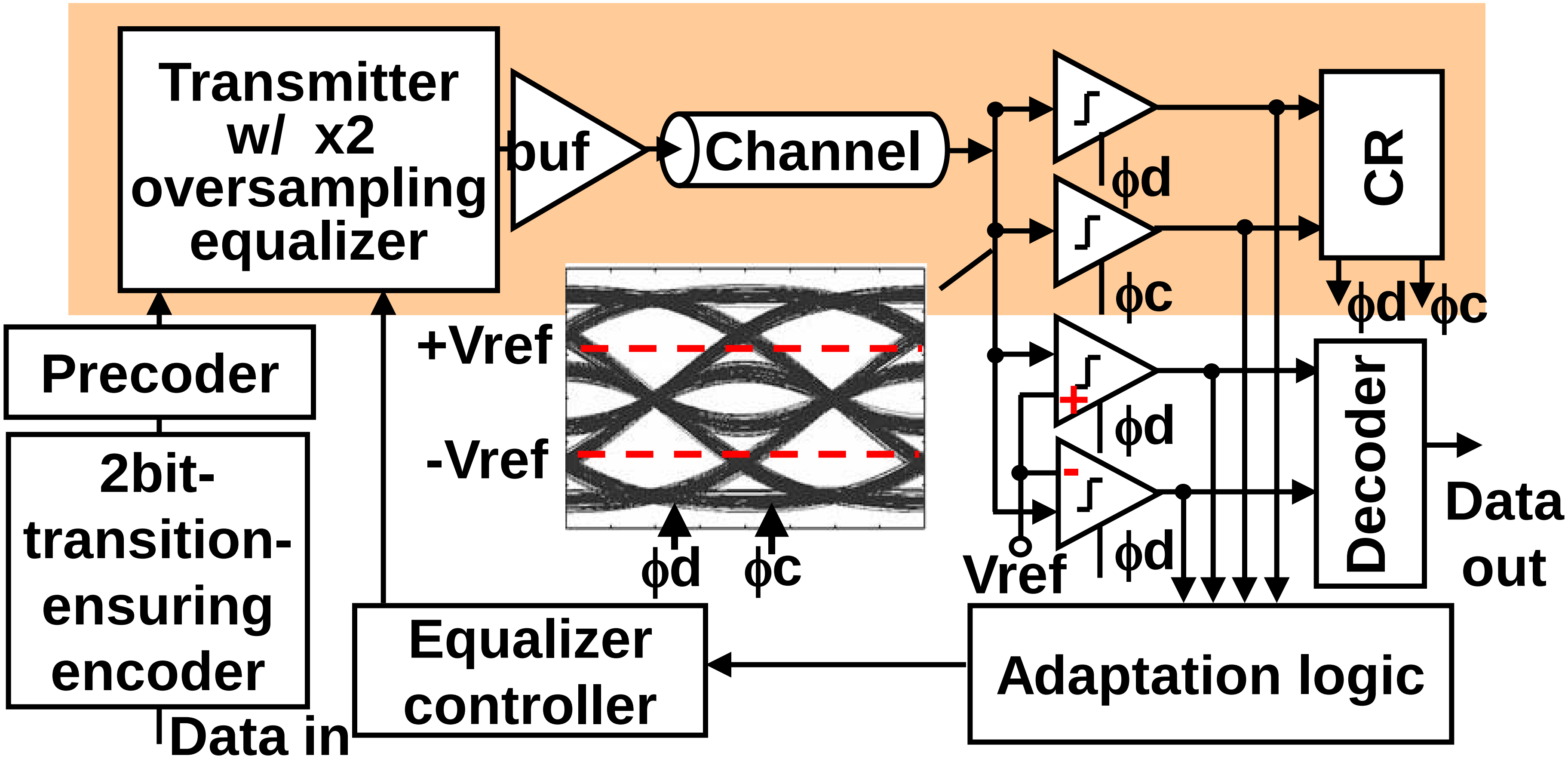


Before optimization After optimization



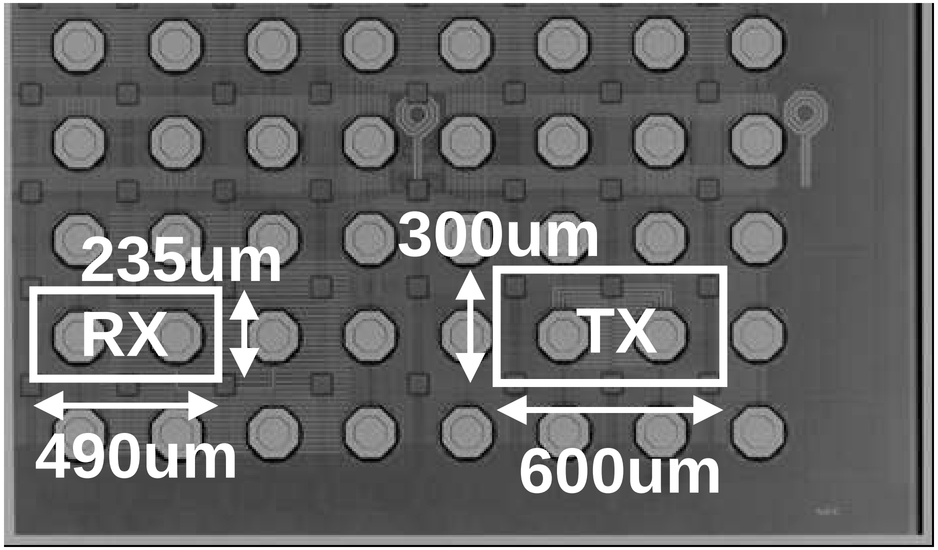
- **Sampled edge can be obtained from CR front-end**
  - **No additional component**
- **Successful optimization by edge equalization**

Duobinary Signaling System



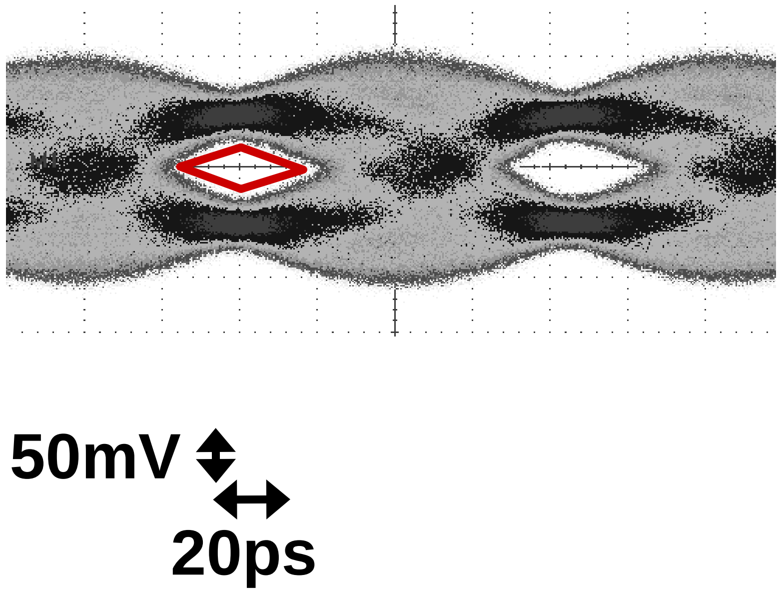
- Moderate design complexity against PAM-2
  - Equalizer, Precoder, and Data decision circuit
  - Test chip includes transmitter and clock recovery

Chip Micrograph

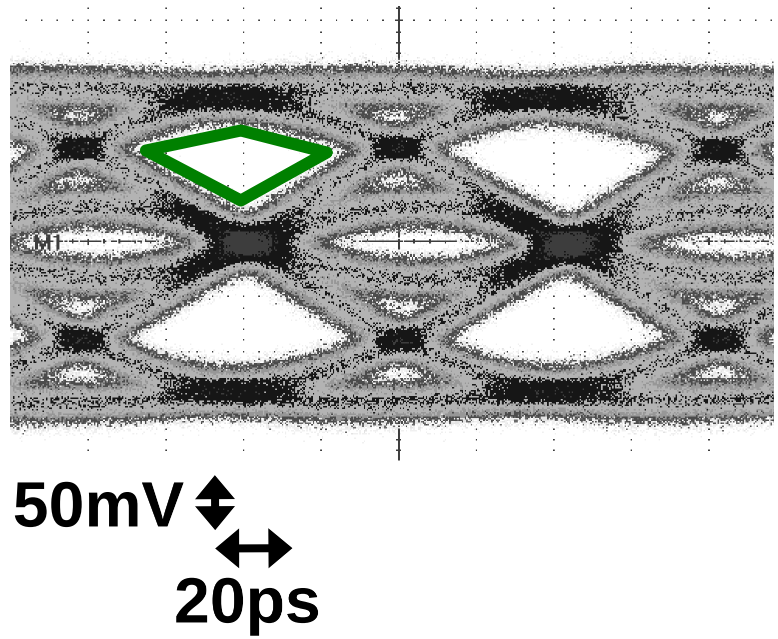


- **Features**
  - **90nm CMOS 6 Metal Layer, Vdd: 1.0V**
  - **TX: 133 mW, 0.18mm^2**
  - **RX: 97 mW, 0.055mm^2**

Eye Diagrams



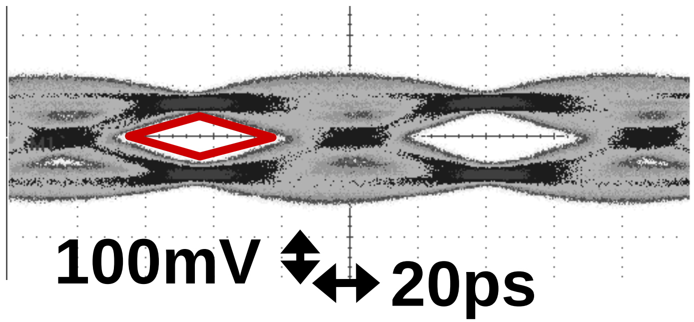
(a) PAM-2

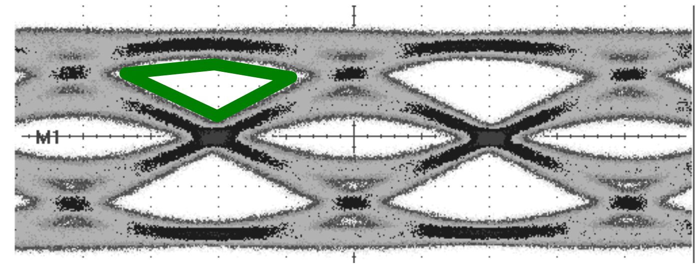


(b) Duobinary

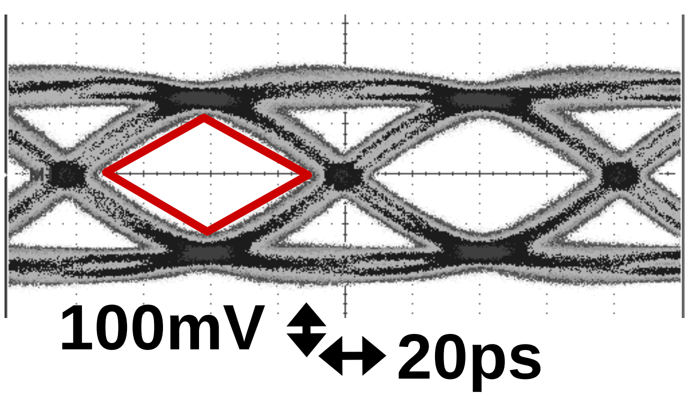
- 12Gb/s signaling over 75-cm low-ε PCB
  - 49mV x 35ps (PAM-2), 73.5mV x 52ps (Duobinary)
  - Duobinary eye height/width: 3.5 dB/1.5 times larger

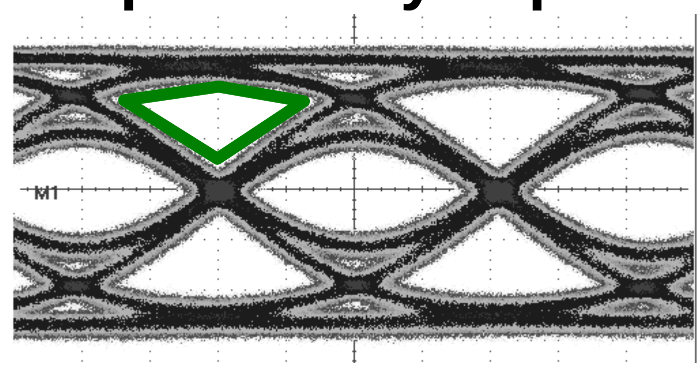
Eye Diagrams (cont.)





- 12Gb/s signaling over 50-cm low-ε PCB
- Duobinary and PAM-2 have comparable eye openings





- 12Gb/s signaling over 25-cm low-ε PCB
- PAM-2 has larger eye opening than duobinary

Conclusions

- **Duobinary signaling**
  - **Allows controlled amount of ISI to reduce signaling bandwidth**
  - **Better compatibility to PAM-2**
  - **Better crosstalk/reflection immunity**
- **Developed techniques**
  - **X2 oversampled equalization**
  - **2bit-transition-ensured coding**
  - **Edge equalization**
- **Measured results**
  - **Fabricated with 90nm CMOS**
  - **3.5dB x 1.5 times larger eye-opening than PAM-2**

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