3.6 12Gb/s Duobinary Signaling with ×2 Oversampled Edge Equalization

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In recent chip-to-chip and backplane data transfers on printed circuit boards, data-rates are limited not by the operating speeds of the circuits in the transceiver LSIs, but by the bandwidth of the transmission media. Duobinary [1] is a type of partial response signaling that can be helpful in reducing the required bandwidth, because it allows for a controlled amount of ISI to be removed afterward. Figure 3.6.1 shows the transfer function for duobinary signaling, as well as channel loss and the frequency response of the combined channel and transmitter/receiver equalizers. In duobinary signaling, the resulting ISI may be expressed in the z-domain as $1+z^{-1}$. Transmitter/receiver equalization results in binary input data (1, 0) being output as a duobinary data (2, 1, 0).

Figure 3.6.1 also shows the transfer functions of PAM-2 and PAM-4 [2], as well as the respective eye-heights of duobinary, PAM-2, and PAM-4 signals (E_{duobin}, E_{PAM-2}, and E_{PAM-4}). Each of these signals is equalized along the same channel loss curve with respect to a corresponding Nyquist frequency: f_{nyq} (PAM-2), $f_{nyq}/2$ (PAM-4) and $2f_{nyq}/3$ (duobinary), where f_{nyq} is half the symbol rate of PAM-2. The relationship between Nyquist frequency and eye-height is calculated from theoretical transfer curves for each of PAM-2/4 (cosine roll-off) and duobinary ($1+z^{-1}$). The eye-height of the PAM-4 signal is 7.4dB below the gain at $f_{nyq}/2$ due to four-level signaling. In contrast, the eye-height of a duobinary signal with three levels is only 1.6dB below the gain at $2f_{nyq}/3$. This is due to the fact that a PAM-4 signal includes the maximum transition between the lowest and the highest levels, however, the duobinary signal only includes the transitions between adjacent levels. Thus, duobinary signaling has better immunity to crosstalk/reflection than PAM-4 and that is proportional to the maximum transition.

At each Nyquist frequency, when the channel loss difference between duobinary and PAM-2 is larger than 3.7dB, duobinary eye-height will be larger than that of PAM-2. Similarly, when the difference between duobinary and PAM-4 is less than 5.8dB, duobinary eye-height will be larger than that of PAM-4. However, when the difference is larger than 5.8dB, duobinary eye-opening will be comparable to that of PAM-4; because a lower roll-off factor of the PAM-4 transfer function, caused by lower PAM-4 gain at duobinary Nyquist frequency, results in horizontal eye closure. Specifically, the duobinary eye-height is estimated to be 3dB larger than that of PAM-2/4 in 12Gb/s signaling over a 75cm trace on a low-ε PCB.

Figure 3.6.2 shows the proposed duobinary signaling system. The resulting duobinary signal is sampled by four-way decision circuits; two for data decisions and the rest for clock recovery (CR). In data decisions, duobinary signals are compared with reference voltages at the symbol rate and the comparison results are decoded into binary data.

In adaptive equalization, error information based on a comparison of expected and actual amplitudes of equalized output is indispensable to the optimization of equalizer filter coefficients. In PAM-2/4, this requires a dedicated reference voltage and an additional comparator. Neither is required in duobinary signaling, because the sampled transition-edge value used by the CR to extract the input-signal timing information can also be utilized to provide the required error information. Figure 3.6.3 shows that although superposition of a duobinary single-bit responses having an optimum Nyquist interval of $1.5T_{symbol}$ (where T_{symbol} is the symbol interval for PAM-2/duobinary) results in a zero value at the sample point, a larger Nyquist interval has a non-zero value at this point. This sample-point value can serve as the error information needed to optimize the transmitter equalizer in an iteration procedure based on the Sign-Sign-LMS algorithm.

Figure 3.6.4 shows the ×2 oversampled equalizer essential for the proposed duobinary signaling. The single-bit responses of duobinary signals have their peak values at the intermediate point between symbol-rate sampling points. To achieve this kind of single-bit response, the waveform to be transmitted has to be filtered by means of oversampled equalization. The multi-phase clock in the proposed system eliminates the need for doubling the sampling clock frequency of the filter, typically required by the oversampled equalization in an ordinary FIR filter. A test chip containing a 12Gb/s 10-tap ×2 oversampled equalizer, uses a 3GHz 8-phase clock. The equalizer itself consists of two 5-tap equalizers with shorted outputs and is used to transmit combined output through the channel. Each 5-tap equalizer uses a 4-phase clock to multiplex one-fourth-rate parallel data from its tap controller. The clock phase difference between these equalizers is 45-degrees, which corresponds to a half-width of one symbol.

Figure 3.6.5 shows CR in duobinary signaling. For high-speed operations, the CR employs conventional ×2 oversampled method, as is used in PAM-2. Unlike PAM-4, the duobinary signals have only one cross-point between symbols, which means that the circuitry required by PAM-4 to select sampled edges in order to assure accurate CR is not needed here. In CR, phase detection is performed by comparing the sampled value with respect to the center threshold at timing ϕc with the value at ϕd. However, when a 1-bit toggle data sequence is transmitted, a duobinary signal with small amplitude cannot be sampled correctly at ϕc. This means that CR may not work at all. This problem can be overcome by using a data encoder that ensures 2-bit transition in the data sequence to be transmitted. Since 2-bit transition eye-height at ϕc will be roughly the same as that of a duobinary signal at ϕd, correct sampling can be achieved. It is confirmed that 2-bit-transition-ensured 8B10B-like coding can be achieved by adding 2 bits to the input data.

Figure 3.6.6 is a micrograph of a backplane transceiver employing duobinary signaling, fabricated in a 6M 90nm CMOS process. It includes the circuit components inside the dashed box of Fig. 3.2.2. The transmitter consumes 133mW and the receiver consumes 97mW. Circuit areas are $0.18mm^2$ (transmitter) and $0.055mm^2$ (receiver). Figure 3.2.7 shows measurement results that are monitored through 75cm low-ε PCB trace. The eye-diagram at the top of Fig. 3.6.7 is for PAM-2 signaling; a 49mV × 35ps opening indicates horizontal ISI caused by steep roll-off. The eye diagram at the bottom is for duobinary signaling and shows a 73.5mV × 52ps opening, which is 2.2-times larger than that of PAM-2.

References:

[1] A. Lender, "The Duobinary Technique for High-Speed Data Transmission," *IEEE Trans. Commun. Electron*., vol. 82, pp. 214-218, May, 1963.

[2] J. L. Zerbe et al., "Equalization and Clock Recovery for a 2.5-10Gb/s 2-PAM/4-PAM Backplane Transceiver Cell", *IEEE J. Solid-State Circuits*, vol. 38, pp. 2121–2130, Dec., 2003.

 0-7803-8904-2/05/$20.00

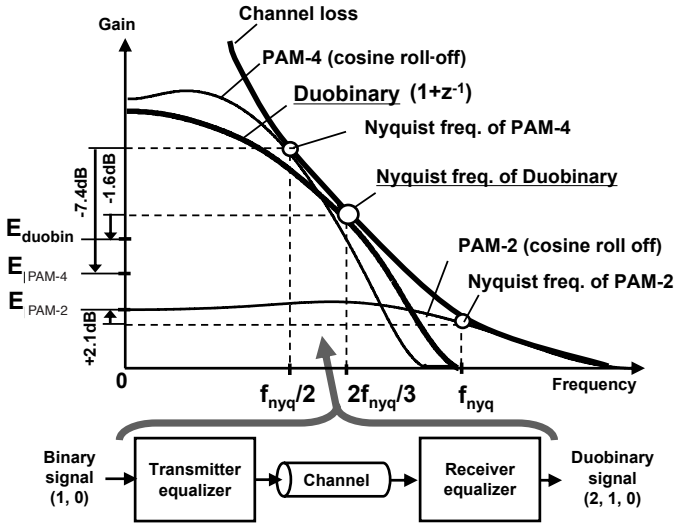

Figure 3.6.1: Transfer functions of duobinary, PAM-2, and PAM-4.

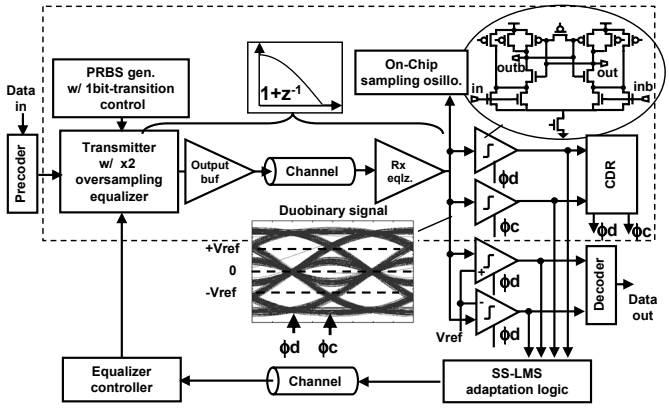

Figure 3.6.2: Block diagram of duobinary signaling system.

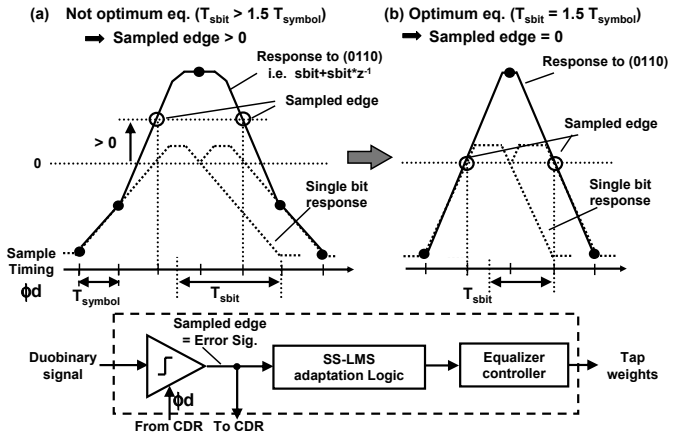

Figure 3.6.3: Edge equalization.

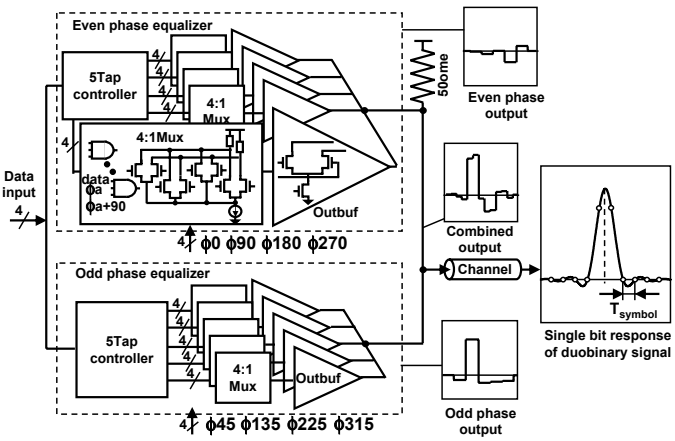

Figure 3.6.4: x2 oversampled equalizer.

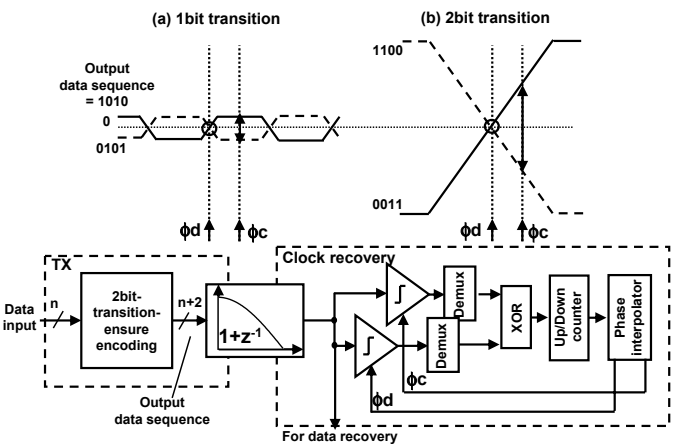

Figure 3.6.5: Clock recovery in duobinary signaling.

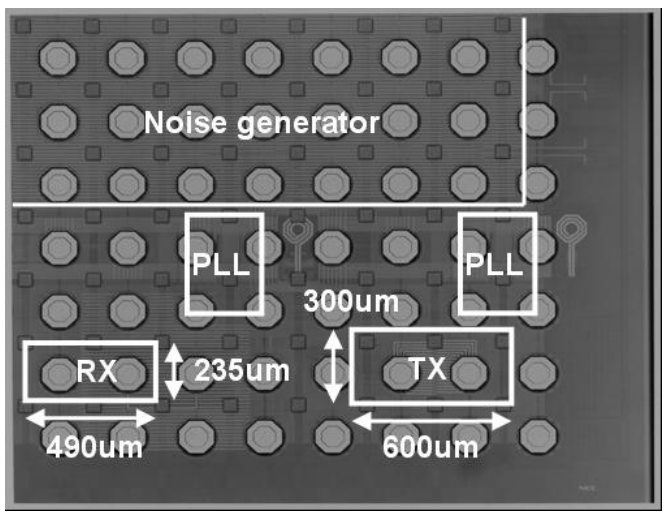

Figure 3.6.6: Chip micrograph.

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