A Low-Jitter 125–1250-MHz Process-Independent and Ripple-Poleless 0.18-μm CMOS PLL Based on a Sample–Reset Loop Filter

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***Abstract*—This paper describes a low-jitter phase-locked loop (PLL) implemented in a 0.18-μm CMOS process. A sample–reset loop filter architecture is used that averages the oscillator proportional control current which provides the feedforward zero over an entire update period and hence leads to a ripple-free control signal. The ripple-free control current eliminates the need for an additional filtering pole, leading to a nearly 90° phase margin which minimizes input jitter peaking and transient locking overshoot. The PLL damping factor is made insensitive to process variations by making it dependent only upon a bandgap voltage and ratios of circuit elements. This ensures tracking between the natural frequency and the stabilizing zero. The PLL has a frequency range of 125–1250 MHz, frequency resolution better than 500 kHz, and rms jitter less than 0.9% of the oscillator period.**

***Index Terms*—CMOS, frequency synthesizer, jitter, oscillator, phase-locked loop, sample–reset loop filter.**

I. Introduction

PHASE-LOCKED loops (PLLs) in mixed analog–digital VLSI ICs operate in a very noisy environment, often with considerable noise introduced through coupling to the supply and substrate. Low-jitter PLLs require high loop bandwidths to reject the oscillator internal noise and the substrate and supply noise [1]–[4]. Designs that are insensitive to process and environmental conditions lead to well-controlled damping factors so that PLL bandwidth can be maximized [2]. Also, adaptive-bandwidth PLLs are desirable for fast-locking applications [5], and fully differential architectures can be used to provide additional supply and substrate noise immunity [6].

Since the introduction of charge-pump PLLs, numerous architectures for PLL components (phase-frequency detectors, charge-pumps, loop filters, and oscillators) have been proposed. The phase-frequency detector (PFD) can be based on NAND/NOR gates or D flip-flops, and several dead-zone avoidance techniques have been proposed [1]–[6]. Connected to PFDs, charge-pumps can be single ended or differential, with pump control switches that are connected to the drain, gate, or source of the current mirror, or using a current steering technique [7]. Fully differential charge pumps have gained an increased interest due to their better supply and substrate noise rejection, although they require increased on-chip capacitance and extra circuitry for common-mode feedback [6].

Passive loop filters are popular for their simplicity [1], [2], [4], [5], but the control of their loop time constants lacks flexibility. A wider range of loop time constants and decreased area of on-chip capacitance can be realized by using active loop filters in conjunction with feedforward charge pumps [3], [6].

Ring oscillators can have a wide frequency range and can be single ended or differential, with voltage [1], [5] or current [2]–[4] control. Cross-coupled differential oscillators with no tail current can be used for low voltage designs [5]. Active load differential inverters are often preferred for their high signal-to-noise ratio, whereas diode clamped differential inverters are used in high-speed applications [3], [4].

Many applications require a stable 50% duty cycle PLL output. A common way of achieving a 50% duty cycle is to run the oscillator at twice the output frequency and then divide the output by two [3]. This method can consume additional power, but is very effective for deep-submicron technologies where use of differential comparators is suboptimal because of large device mismatches. More sophisticated methods of duty cycle control have been developed by using feedback or feedforward correction [5].

Most charge-pump PLLs have two major drawbacks. First, the loop filter pole position must be chosen as a compromise between the loop phase margin and the jitter performance. Second, loop damping factor variation with process requires wide margin for the natural frequency to stabilizing zero separation to keep the jitter peaking and the transient overshoot under the specified maximum value.

This paper describes a sample–reset loop filter architecture that averages the proportional control current which provides the feedforward zero over each update period, minimizing the ripple on the oscillator control signal and thus reduces the reference spurs [8]. The PLL damping factor is made insensitive to process variations by making it dependent only upon a bandgap voltage and ratios of circuit elements. This introduces a tracking mechanism between the loop natural frequency and the stabilizing zero.

II. Sample–Reset Loop Filter Technique

Charge-pump PLLs that have two poles at the origin require a zero to be introduced in the loop for stability. Common methods

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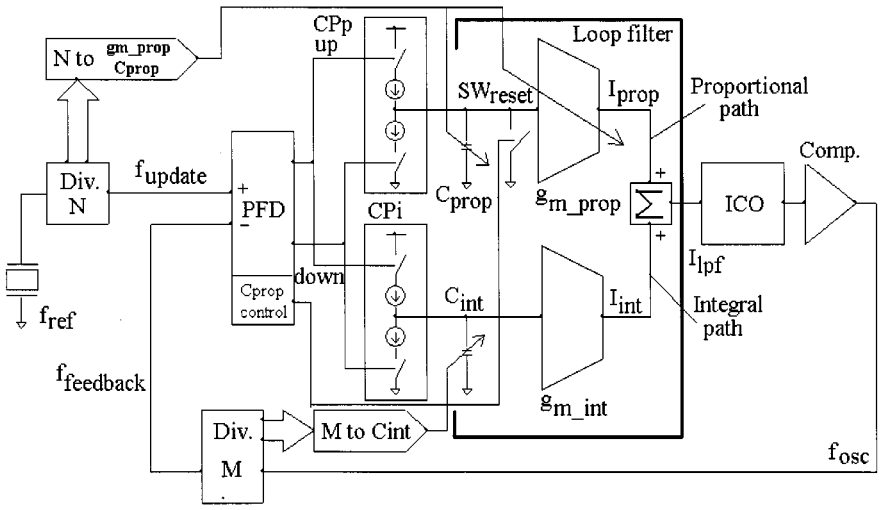

Fig. 1. Sample–reset PLL block diagram.

of adding a zero are introducing a resistor in series with the charge-pump capacitance, or using a feedforward technique. Most charge-pump PLLs use a proportional signal based on the instantaneous phase difference. This signal is characterized by narrow high-amplitude pulses that lead to an abrupt variation of the oscillator control signal and rapid frequency changes that can degrade the PLL's jitter performance. To reduce these effects and hence jitter, the oscillator control signal can be smoothed with a ripple filtering pole, which, unfortunately, degrades the PLL's phase margin.

A PLL's reference input (with frequency $f_{\rm ref}$) often passes through an input divider (N). The output of the N divider is the input to the PFD. The PFD updates its state based on the frequency at the input of the PFD, thus we will refer to this as the update frequency $f_{\rm update}$ and its corresponding period as the update period $T_{\rm update}$: $f_{\rm update} = f_{\rm ref}/N$ and $T_{\rm update} = N/f_{\rm ref}$.

Traditional feedforward charge pumps provide a periodic output current equal to $I_{\rm cp\_p}$ for the phase difference time period $\Delta\varphi$ and 0 otherwise. The average proportional current per update period $I_{\rm ave} = I_{\rm cp\_p} \cdot \Delta\varphi/(2 \cdot \pi)$ determines the position of the stabilizing zero.

The key idea of the sample–reset loop filter architecture is to generate a proportional current that is constant over the entire update period and has a value equal to the average current ($I_{\rm ave}$ as defined in the previous paragraph). This value leads to the same position of the stabilizing zero as in the standard charge-pump PLL, but generates a ripple-free oscillator control current, and thus minimizes the jitter. It can be achieved by first sampling the phase difference for each update period on a capacitor $C_{\rm prop}$ and then injecting a constant control current proportional to the sampled phase difference during the rest of the update period. At the beginning of each update period, a reset must be performed on the sampling capacitance voltage to eliminate the memory of the proportional path. This eliminates an additional pole at the origin that would otherwise make the loop unstable. The reset signal is synchronized with the update frequency and is generated by the PFD.

The major advantage of this architecture is staircase-shaped oscillator control, which does not need additional filtering, and leads to a better jitter performance. The architecture provides a type-II second-order PLL that has nearly 90° phase margin with negligible jitter peaking and transient locking overshoot.

Fig. 1 shows a block diagram of the sample–reset PLL architecture. It consists of a reference frequency generator ($f_{\rm ref}$), an input divider (N), a current controlled oscillator (ICO), a feedback divider (M), a PFD with the associated integral (CPi) and proportional (CPp) charge pumps, and the loop filter. The filter has two signal paths, the integral path consisting of the phase integration capacitance $C_{\rm int}$ and the integral transconductance stage $g_{m\_\rm int}$, and the proportional path that provides the feedforward stabilizing zero with the phase sampling capacitance $C_{\rm prop}$ and the corresponding reset switch $\rm SW_{reset}$, and the proportional transconductance stage $g_{m\_\rm prop}$.

The single sampling capacitance architecture shown in Fig. 2(a) has two shortcomings. First, the proportional control current still has some ripple due to the fact that during each update period the voltage on $C_{\rm prop}$ samples, holds, and finally resets. Second, the reset needs to be very short (less than a few percent of the period). This results in difficult constraints for the reset circuitry. These problems are solved by separating the sample and reset phases from the holding phase with a double capacitance architecture shown in Fig. 2(b). One capacitor is reset, and then samples the phase difference, while the other capacitor is in hold mode and generates the proportional current. The differential single and double sampling capacitance architectures presented in Fig. 2(c) and (d) result in better jitter performance due to higher supply and substrate noise rejection.

A comparison between the proportional path current used in standard charge-pump PLLs and the sample–reset PLL is shown in Fig. 3. The standard charge-pump PLL proportional path output is based on instantaneous phase difference. The sample–reset proportional path output is based on the average phase difference for each update period.

Open loop gain and therefore damping factor varies with the modulus of the feedback divider (M). A nearly constant damping factor is obtained by switching additional capacitance

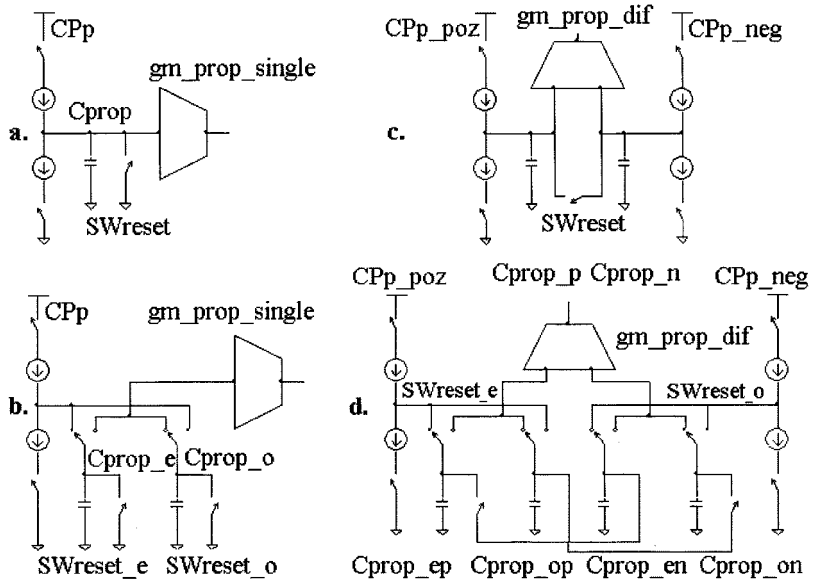

Fig. 2. Single ended/differential and single/double sampling capacitance sample–reset proportional path architectures.

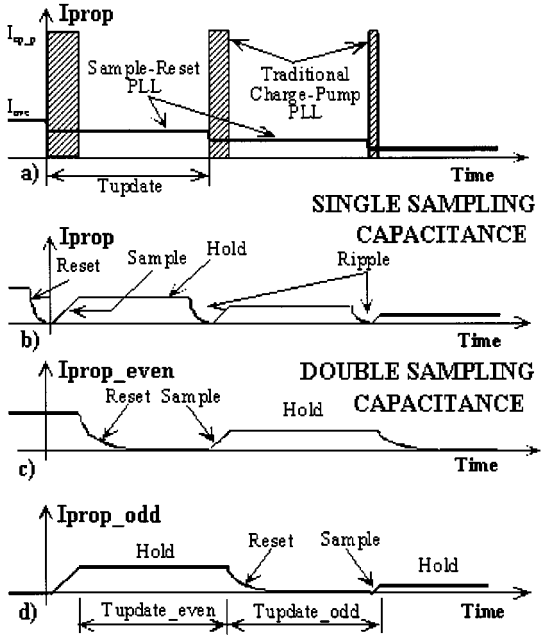

Fig. 3. Sample–reset versus standard PLL proportional current.

$C_{\rm int}$ into the output of the integral path charge pump as the M divider increases. A tradeoff between the amount of $C_{\rm int}$ capacitance switching and the maximum damping factor variation over a given range of M divider modulus must be done. The $C_{\rm int}$ capacitance is tuned dynamically by a digital decoder that converts the M divider value into the appropriate digital control signals to the $C_{\rm int}$ capacitance switches. The proportional path current is averaged over each update period. Changing N changes the update period and therefore the position of the stabilizing zero. The position of the zero is inversely proportional to the update period multiplied by the proportional path gain. The proportional path gain $(g_{m\_\rm prop}/C_{\rm prop})$ can be varied as a function of the update frequency to minimize the variation of the zero frequency. A tunable capacitance $C_{\rm prop}$ combined with a programmable $g_{m\_\rm prop}$ transconductance minimizes the area of on-chip capacitance for a given power consumption in the proportional path. A second digital decoder is used to generate the control signals for the proportional path transconductance and capacitance switches.

III. Stability of the Sample–Reset PLL

The closed-loop small-signal model of the sample–reset PLL is shown in Fig. 4. Key components are the input divider $(1/N)$, PFD $(K_{\rm pfd} = 1/2\pi)$, the integral $(I_{\rm cp\_i})$ and proportional $(I_{\rm cp\_p})$ charge pumps, the loop filter with the integral $(K_{\rm int}/s = g_{m\_\rm int}/(C_{\rm int} \cdot s))$ and proportional $(K_{\rm prop} = (T_{\rm update} \cdot g_{m\_\rm prop})/C_{\rm prop})$ paths, the current controlled oscillator $(K_{\rm ico}/s)$, and the feedback divider $(1/M)$.

The total current supplied by the sample–reset loop filter $I_{\rm lpf}$ is the sum of the integral $I_{\rm int}$ and proportional $I_{\rm prop}$ path currents:

$$\begin{aligned} I_{\rm lpf}(s) &= I_{\rm int}(s) + I_{\rm prop}(s) \\ &= \frac{I_{\rm cp\_i}}{2\pi} \cdot \frac{1}{sC_{\rm int}} \cdot g_{m\_\rm int} + \frac{I_{\rm cp\_p}}{2\pi} \cdot \frac{T_{\rm update}}{C_{\rm prop}} \cdot g_{m\_\rm prop}. \end{aligned} \tag{1}$$

The open loop transfer function and the natural frequency (square root of the dc gain $K_{\rm DC}$) are

$$\begin{aligned} H_{\rm open}(s) = \frac{I_{\rm cp\_i}}{2\pi} \cdot \frac{g_{m\_\rm int}}{sC_{\rm int}} \\ \cdot \left[\frac{I_{\rm cp\_p}}{I_{\rm cp\_i}} \cdot \frac{C_{\rm int}}{C_{\rm prop}} \cdot \frac{1}{f_{\rm update}} \cdot \frac{g_{m\_\rm prop}}{g_{m\_\rm int}} \cdot s + 1\right] \\ \cdot \frac{K_{\rm ico}}{s} \cdot \frac{1}{M} \end{aligned} \tag{2}$$

$$\omega_n = \sqrt{K_{\rm DC}} = \sqrt{\frac{K_{\rm ico} \cdot I_{\rm cp\_i} \cdot g_{m\_\rm int}}{2\pi \cdot C_{\rm int} \cdot M}}. \tag{3}$$

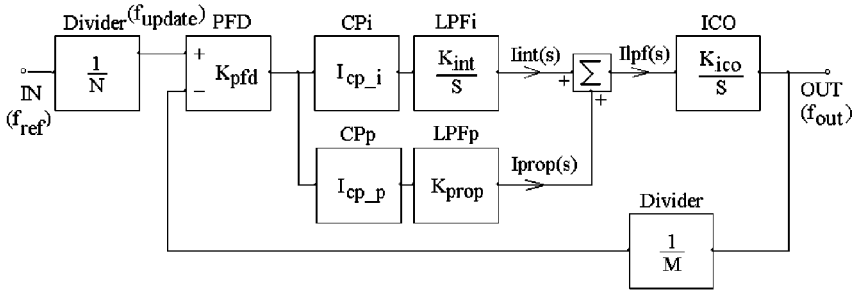

Fig. 4. Sample–reset PLL small-signal model.

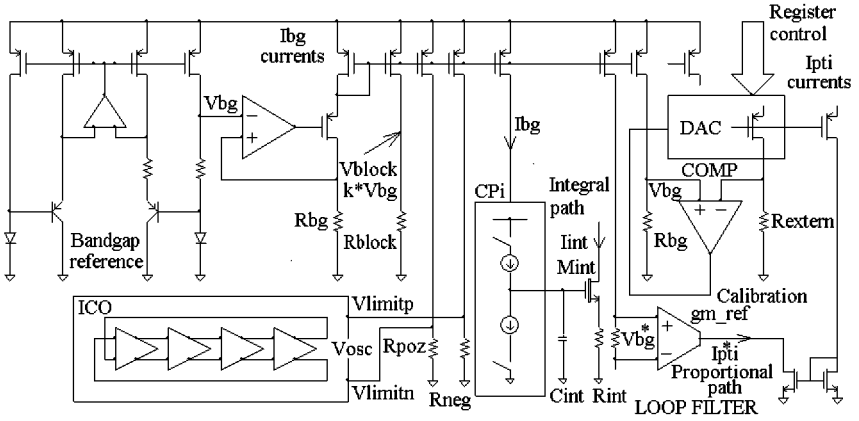

Fig. 5. PLL architecture for process-independent damping factor.

The resulting expression for the stabilizing zero ωz is shown in (4). It is important to note that the zero position is $f_{\rm update}$ times a ratio of currents, times a ratio of capacitances, times a ratio of transconductances, that with proper design and layout will exhibit very low process variation:

$$\omega_z = f_{\rm update} \cdot \frac{I_{\rm cp\_i}}{I_{\rm cp\_p}} \cdot \frac{C_{\rm prop}}{C_{\rm int}} \cdot \frac{g_{m\_\rm int}}{g_{m\_\rm prop}}. \tag{4}$$

The damping factor ξ of type-II second-order PLLs is equal to half the natural frequency divided by the stabilizing zero:

$$\xi = \frac{1}{2} \cdot \frac{\omega_n}{\omega_z} = \frac{1}{2} \cdot \sqrt{\frac{K_{\rm ico} \cdot I_{\rm cp\_i} \cdot C_{\rm int}}{2\pi \cdot M \cdot g_{m\_\rm int}}} \cdot \frac{I_{\rm cp\_p}}{I_{\rm cp\_i}} \cdot \frac{1}{C_{\rm prop}} \cdot \frac{g_{m\_\rm prop}}{f_{\rm update}}. \tag{5}$$

A tracking mechanism between the PLL's natural frequency and stabilizing zero ensures process independence of the damping factor. A bandgap voltage $V_{\rm bg}$ is used to generate all the on-chip biasing currents and reference voltages (see Fig. 5). There are two types of bias currents used throughout the chip. The first current, $I_{\rm bg} = V_{\rm bg}/R_{\rm bg}$, is obtained by imposing the bandgap voltage across an internal polysilicon resistor $R_{\rm bg}$, which results in a current inversely proportional to that resistance. Mirroring the $I_{\rm bg}$ current into resistors ($R_{\rm block} = K \cdot R_{\rm bg}$) that are carefully matched with the bandgap resistor $R_{\rm bg}$ provides a technique of replicating a fraction of the process-independent bandgap voltage within the different circuit blocks in the IC ($V_{\rm block} = K \cdot R_{\rm bg} \cdot I_{\rm bg} = K \cdot V_{\rm bg}$). The second bias current ($I_{\rm pti} = V_{\rm bg}/R_{\rm extern}$) is obtained by calibrating a temperature-compensated replica of the $I_{\rm bg}$ current to an external high-precision resistor $R_{\rm extern}$. An onboard digital-to-analog converter (DAC) and control circuit performs the calibration, resulting in a process and temperature independent current $I_{\rm pti}$.

The most significant contribution to the damping factor process variation [see (5)] is due to the proportional path transconductance $g_{m\_\rm prop}$. This can be canceled out by first generating a reference process-independent transconductance $g_{m\_\rm ref}$ and then deriving $g_{m\_\rm prop}$ as a weighted version of $g_{m\_\rm ref}$. The $g_{m\_\rm ref}$ transconductance is generated using a differential amplifier with its input signal set to a fraction $V^*_{\rm bg}$ of the bandgap voltage, and its output current set to a fraction $I^*_{\rm pti}$ of the process-independent bandgap trimmed current. Feedback is used to tune the tail current, so the resulting transconductance $g_{m\_\rm ref} = I^*_{\rm pti}/V^*_{\rm bg}$ is virtually process independent.

The next major contribution is from the term $I_{\rm cp\_i}/g_{m\_\rm int} \approx I_{\rm cp\_i} \cdot R_{\rm int}$ that can be canceled out by mirroring $I_{\rm bg}$ to be used as charge-pump currents and carefully matching the integral path resistor $R_{\rm int}$ with the bandgap resistor $R_{\rm bg}$, as shown in Fig. 5. Thus $I_{\rm cp\_i} \cdot R_{\rm int} = V_{\rm bg} \cdot R_{\rm int}/R_{\rm bg}$ is a fraction of the bandgap voltage, and is process independent.

Finally, the supply and process variation of the oscillator gain ($K_{\rm ico}\alpha 1/V_{\rm osc}$) is reduced by clamping the amplitude of oscillation $V_{\rm osc}$ to a fraction of the bandgap voltage. The damping levels are given by $V_{\rm limitp} = R_{\rm poz} \cdot I_{\rm bg} = K_1 \cdot V_{\rm bg}$ and $V_{\rm limitn} = R_{\rm neg} \cdot I_{\rm bg} = K_2 \cdot V_{\rm bg}$.

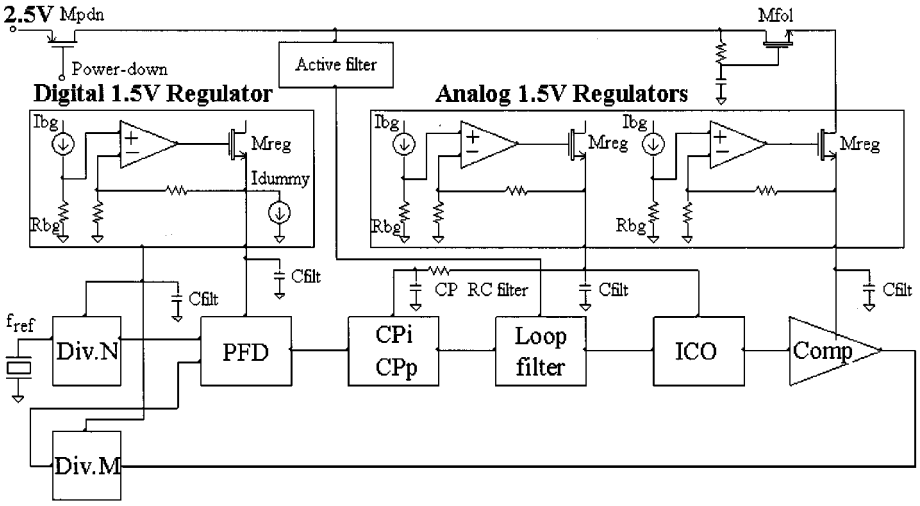

Fig. 6. Power supply circuitry for low-jitter operation.

The natural frequency process variation [see (3)] is given by the integral charge-pump current $I_{\text{cp\_i}} = V_{\text{bg}}/R_{\text{bg}}$ and the integral path transconductance $g_{m\_\text{int}} \approx 1/R_{\text{int}}$, resulting in a process variation inversely proportional to the polysilicon bandgap resistor ($\omega_n \propto \sqrt{1/R_{\text{bg}} \cdot 1/R_{\text{int}}} \propto 1/R_{\text{bg}}$). The stabilizing zero process variation [see (4)] is mainly influenced by the integral path transconductance ($g_{m\_\text{int}} = 1/R_{\text{int}}$) which is also inverse to polysilicon resistance (assuming g_{m_prop} is process independent and $I_{\text{cp\_i}}/I_{\text{cp\_p}}$ and $C_{\text{prop}}/C_{\text{int}}$ have very low process dependence). Thus, both the natural frequency and stabilizing zero are process dependent, but they track each other, yielding a process-independent damping factor.

To avoid granularity effects, sampling ratios (S = update frequency f_{update} divided by loop bandwidth B) greater than 10 are required [2]. It is desirable to have sampling ratios with low process variation and invariance to the divider's modulus (M, N). The sampling ratio varies with $\sqrt{M}$ over a given frequency range. Reducing its variation requires the division of the frequency range into multiple subranges with low $M_{\max}/M_{\min}$ ratios:

$$\begin{aligned} S &= \frac{f_{\text{update}}}{B} \\ &= \frac{f_{\text{out}}}{M} \cdot \frac{1}{\sqrt{1+2\cdot\xi^2+\sqrt{2+4\cdot\xi^2+4\cdot\xi^4}}\cdot f_n} \\ &= \frac{f_{\text{out}}}{\text{func}(\xi)} \cdot \sqrt{\frac{2\pi C_{\text{int}} \cdot R_{\text{int}}}{K_{\text{ico}} \cdot I_{\text{cp\_i}} \cdot M}}. \end{aligned} \tag{6}$$

IV. Power Supply Strategy for Low-Jitter Operation

PLLs operating in large mixed analog–digital chips are subject to noise injection from the power supply, ground, and substrate. This degrades the overall jitter performance significantly. Therefore, low-jitter operation requires a careful design of the power supply for the PLL building blocks. Fig. 6 is a diagram of the PLL power supply circuitry.

A high power-supply rejection ratio (PSRR) regulator is used to separate the supply of the ICO from the rest of the PLL [1]–[5]. A further reduction of the supply-injected noise is achieved by separating the drain of the regulator's serial transistor M_{reg} from the rail with a source follower M_{fol}. The 1.5-V supplies are filtered with local bypass capacitors C_{filt}.

The differential to single-ended converter (comparator) needs to generate sharp edges to maintain a precise 50% duty cycle. The sharp edges cause significant supply ripple. Thus, the comparator's supply needs to be separated from the ring oscillator supply.

The charge pump is one of the PLL components that is most sensitive to supply noise. *RC* filtering is used to isolate the charge pump from the other elements in its supply domain.

The loop filter is biased from the 2.5-V analog chip supply through an active filter. The 2.5-V supply voltage is necessary to provide proper headroom in the loop filter.

An optimum power management methodology in large mixed analog–digital chips requires an ability to power down the PLL. A large area PFET (M_{pdn}) is used as serial switch to cut or pass the supply current to the PLL.

V. Sample–Reset PLL Building Blocks

A. Phase-Frequency Detector

Fig. 7 shows the PFD and the block that generates the control signals for the proportional capacitance switches. The PFD uses the standard seven NAND gates architecture [1]–[4]. Generating two synchronous narrow pulses during each update period for both pump-up and pump-down charge-pump signals eliminates the dead zone at small phase differences. A oneshot circuit triggered by the PFD reset signal is used. Pass gates are added at the UP and DOWN outputs to match the propagation time of the inverters from the UPb and DOWNb outputs.

The PFD also generates the control signals for the proportional path switches, which select between the even and odd capacitors and determine the sample, hold, and reset phases. A flag for even and odd update periods is generated by dividing the frequency of the dead-zone avoidance oneshot circuit by two. Nonoverlapping control signals are used to connect the proportional capacitors alternately to the charge pump and the propor-

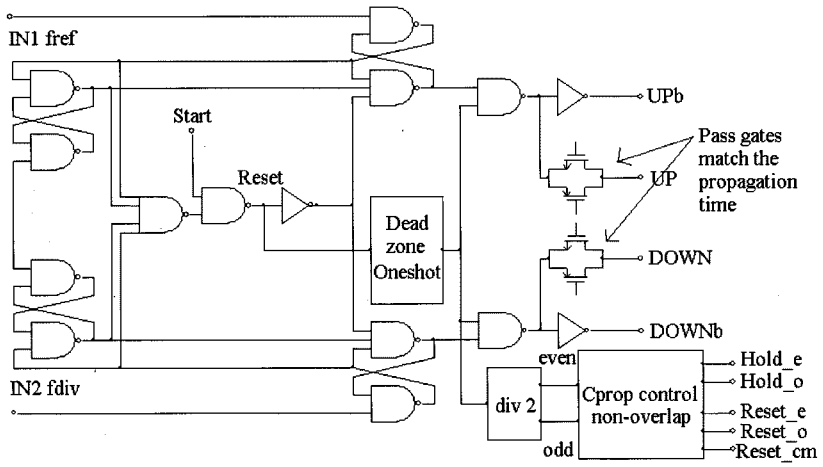

Fig. 7. Phase-frequency detector and $C_{\rm prop}$ switches control block.

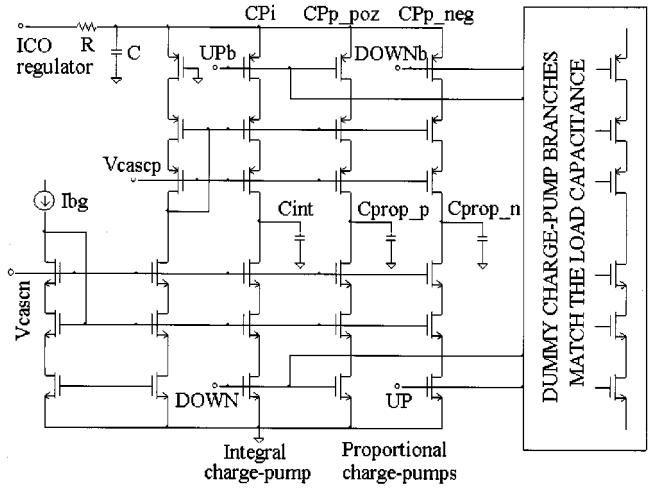

Fig. 8. Integral and proportional charge pumps.

tional transconductance (Hold_e, Hold_o). There are also signals for charge-sharing reset on the proportional capacitor (Reset_e, Reset_o) and a proportional transconductance common-mode reset (Reset_cm).

B. Charge Pumps

Fast-locking PLLs require wide bandwidth. They also require the PFD and charge pumps to operate at high update frequencies. It is important to have low clock feedthrough and charge sharing effects. The source switch architecture of the charge pump is shown in Fig. 8. This architecture ensures high speed since all internal nodes are low impedance. Clock feedthrough is also low because the drains of the switches are separated from the high-impedance output node. Dummy switches are added to compensate for charge sharing. Each PFD output sees the same number of nMOS and pMOS switches, leading to a matched switching time.

C. Sample–Reset Loop Filter

Fig. 9 shows a detailed schematic of the sample–reset loop filter. The single ended integral path is a voltage-to-current (V–I) converter onto a capacitor $C_{\rm int}$. The transistor $M_{\rm int}$ and a source degeneration resistor $R_{\rm int}$ has a transconductance $g_{m\_\rm int} = g_m/(1 + g_m \cdot R_{\rm int}) \approx 1/R_{\rm int}$. The transconductance is set by $R_{\rm int}$ and will not depend upon $M_{\rm int}$ transistor g_m. Care was taken to Kelvin connect the $C_{\rm int}$ and $R_{\rm int}$ ground connections.

The proportional path is more susceptible to substrate and supply noise and therefore uses a fully differential architecture. There are three subcircuits: a reference transconductance stage $g_{m\_\rm ref}$ that provides a process-independent transconductance, a programmable transconductance stage $g_{m\_\rm prop}$, and a switching block $\rm SW\_cprop$. The programmable g_m stage generates a binarily weighted replica of the reference transconductance to produce the proportional path control current. The voltage sampled on the capacitor $C_{\rm prop}$ controls the current in the programmable g_m stage. The switching block successively connects the proportional capacitors first to the proportional charge pumps ($\rm CP_{p\_poz}, CP_{p\_neg}$), then to the programmable transconductance stage, and finally to the reset voltage $V_{\rm cm\_reset}$. The size of $C_{\rm int}$ and $C_{\rm prop}$ capacitors is chosen so that the contribution of kT/C noise is negligible.

The process-independent reference transconductance stage is a differential pair (M_{rg_m+} and M_{rg_m-}) tuned to a constant g_m by a feedback circuit that regulates its tail current. The differential pair input is a fraction of the bandgap voltage generated locally by injecting a replica of the bandgap current $I_{\rm bg}$ into a resistor $R_{\rm in}$ which matches the bandgap resistor $R_{\rm bg}$. A trimmed bandgap current $I_{\rm pti}$ is summed into the drains of the differential pair. The resulting transconductance ($g_{m\_\rm ref} \propto I_{\rm pti}/V_{\rm bg}$) is virtually process, temperature, and supply independent.

This circuit has both positive and negative feedback. Connecting a large compensation capacitor C_c to the high impedance output of the differential pair ensures stable operation. The resulting dominant pole is at a very low frequency and the reference g_m circuit has a long settling time. Therefore, the reference stage must be isolated from any major source of ripple, particularly the steps due to the switching of the proportional capacitors.

The tail current of the reference g_m stage is mirrored into several replica g_m stages that are binarily weighted versions

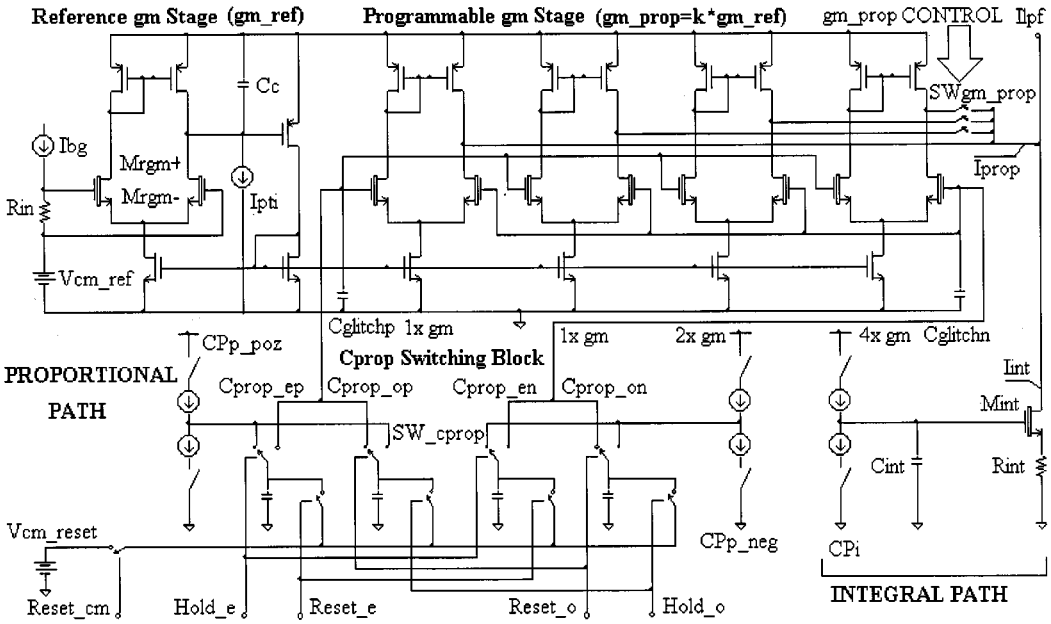

Fig. 9. Current-mode sample–reset loop filter.

of the reference. The currents from the binarily weighted g_m stages are delivered to a set of switches $\mathrm{SW}_{g_m\_\mathrm{prop}}$. The state of the switches determines the transconductance ($g_{m\_\mathrm{prop}} = f(\mathrm{SW}_{g_m\_\mathrm{prop}}) \cdot g_{m\_\mathrm{ref}}$). This variable g_m is used in conjunction with the capacitor C_{prop} to tune the value of the stabilizing zero as a function of the loop update frequency.

The differential architecture of the programmable g_m stage requires two pairs of proportional path capacitors, even ($C_{\mathrm{prop\_ep}}/C_{\mathrm{prop\_en}}$) and odd ($C_{\mathrm{prop\_op}}/C_{\mathrm{prop\_on}}$) pairs, and two proportional charge pumps ($\mathrm{CP}_{\mathrm{p\_poz}}$ and $\mathrm{CP}_{\mathrm{p\_neg}}$). Differential charging significantly simplifies the reset circuit. Fast reset is achieved through charge sharing between the two capacitors within a pair. $C_{\mathrm{prop\_ep}}$ shares with $C_{\mathrm{prop\_en}}$, and $C_{\mathrm{prop\_op}}$ shares with $C_{\mathrm{prop\_on}}$.

During the even update period, the even capacitor pair is first reset to the common-mode voltage $V_{\mathrm{cm\_reset}}$ and then connected to the proportional charge pumps ($\mathrm{CP}_{\mathrm{p\_poz}}$ and $\mathrm{CP}_{\mathrm{p\_neg}}$). Then the pair samples the current phase difference. Meanwhile, the odd capacitor pair that has sampled the previous phase difference is connected to the programmable g_m stage to generate a proportional path current. During the odd update period, the odd capacitor pair is first reset and then connected to the proportional charge pumps to sample the phase difference. Meanwhile, the even capacitor pair is connected to the programmable g_m stage [see waveforms in Fig. 3(c), (d)]. Two sets of reset switches are used. The first switches (controlled by Reset_e and Reset_o) connect the positive and negative capacitors within a pair to form a coarse charge-sharing reset. The second switches (controlled by Reset_cm) connect the two shorted capacitors to a reference voltage to prevent common-mode voltage drift.

The matching of the even and odd switches is critical for the proper operation of the sample–reset loop filter. Two small capacitances ($C_{\mathrm{glitchp}}, C_{\mathrm{glitchn}}$) are permanently connected at the input of the programmable g_m stage. These capacitances prevent glitching on the proportional path by keeping the g_m stage from floating when neither the even nor the odd capacitances are connected at the input.

The phase margin of the sample–reset PLL is sensitive to any additional delay in the loop, particularly from the proportional path. Reducing the delay in the proportional path to nearly zero is accomplished by connecting the proportional capacitors to the g_{m_prop} stage immediately after the sampling phase. Dead-zone avoidance pulses that appear after the phase difference time period ends trigger the hold signals (Hold_e, Hold_o).

D. Controlled Oscillator

Maximizing loop bandwidth and minimizing oscillator phase noise minimizes jitter. Variation of oscillator gain directly influences the loop damping factor [see (5)]. Therefore, a process, temperature, frequency, and supply independent gain leads to a larger potential phase margin and better linearity of the PLL. Fig. 10 shows a diagram of the ICO.

The ring oscillator uses differential inverters to improve supply rejection and reduce substrate noise effects. Symmetric active load provides high oscillation amplitude and therefore good signal-to-noise ratio.

A simplified model of the ICO is a relaxation oscillator where the output capacitor is charged and discharged between two threshold levels by a constant current. The resulting gain is inversely proportional to the capacitance at the output of each ring oscillator stage (C_{out}) and the amplitude of oscillation (V_{osc}): $K_{\mathrm{ico}} \propto 1/(C_{\mathrm{out}} \cdot V_{\mathrm{osc}})$.

A process and supply independent gain is achieved by clamping ring element amplitude to a fraction of the bandgap voltage. The positive and negative clamping voltages are generated locally by injecting two I_{bg}-based currents ($I_{\mathrm{bgp}}, I_{\mathrm{bgm}}$)

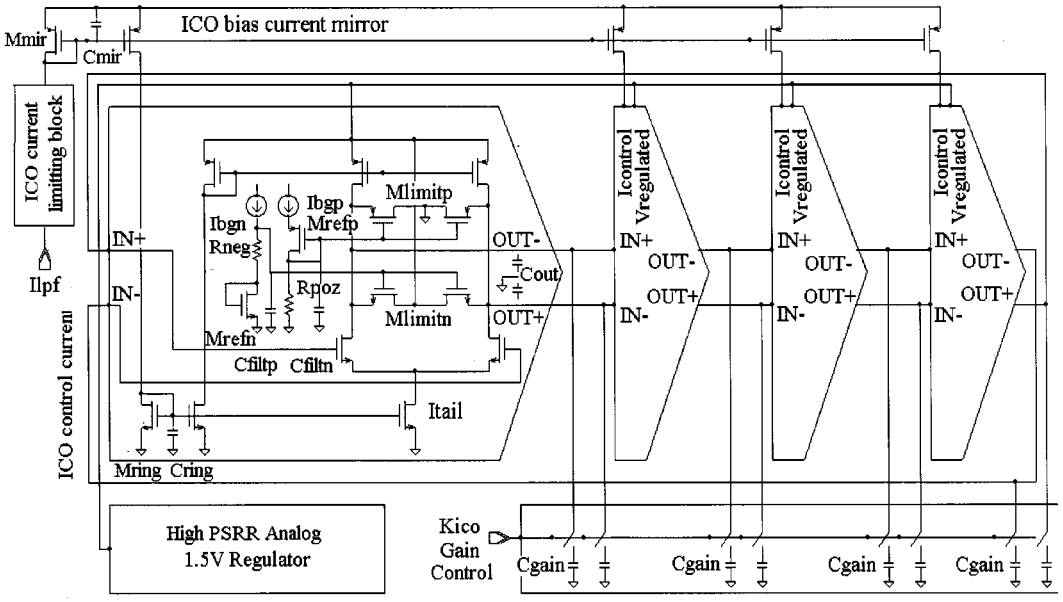

Fig. 10. ICO with process-independent output amplitude.

into two resistors $(R_{\rm poz}, R_{\rm mg})$ matched to the bandgap resistor. Two diode connected devices $(M_{\rm refp}, M_{\rm refn})$ are connected inseries with $R_{\rm poz}$ and $R_{\rm mg}$. Careful matching of $M_{\rm refp}$ and $M_{\rm refn}$ to clamping devices $M_{\rm limitp}$ and $M_{\rm limitn}$ help cancel the $V_{\rm GS}$ component in the positive and negative limiting voltages. Soft clamping is used, where the limiting devices are ON for a very small fraction of the oscillator period. Therefore, the process dependent input impedance of the limiting devices has a negligible influence on the oscillator period. Additional filtering at the positive and negative limiting nodes $(C_{\rm filtp}, C_{\rm filtn})$ significantly improves the ring element PSRR.

The loop has no ripple filtering pole. The most significant high-order parasitic poles are those of the current mirror that biases the four ring elements $(g_m(M_{\rm mir})/C_{\rm mir})$ and of the ring elements $(g_m(M_{\rm ring})/C_{\rm ring})$ (see Fig. 10). Both poles are at least two decades higher than the stabilizing zero and have a negligible effect on loop phase margin.

To improve oscillator linearity and provide wide frequency range, the ICO has several subranges where additional capacitance $C_{\rm gain}$ is gradually switched onto the output of each ring element as needed to reduce frequency. The oscillator is thus required to operate on only a narrow region of a nonlinear $f(I)$ curve, ensuring a fairly constant gain. This increases oscillator linearity but reduces PLL open-loop gain. To compensate for this reduction in gain, the integral path capacitor $C_{\rm int}$ is increased, to keep the $K_{\rm ico} \cdot C_{\rm int}$ term in the damping factor expression constant (5).

During the nonlinear locking process the transient overshoot can drive the oscillator to an output frequency higher than the maximum operating frequency of the divider. This can cause a catastrophic divider failure, and the PLL can fail to lock, and can also fail to recover. To prevent this, a current limiting circuit is introduced into the ICO. The circuit limits the maximum control current so that the ICO frequency cannot exceed the maximum divider frequency.

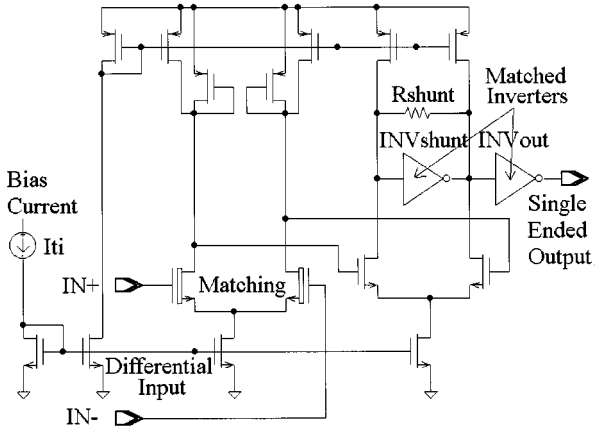

Fig. 11. Differential-to-single-ended converter.

E. Output Comparator

A differential-to-single-ended converter (comparator) must be used to drive the feedback divider. The comparator should not significantly load the ring oscillator.

A critical parameter in many systems is a well-controlled 50% duty cycle over process, temperature, operating frequency, and supply voltage variations. This circuit uses a feedback architecture that closely matches the trip point of the comparator decision stage with that of the output buffer.

Differential comparators in deep-submicron technologies often have duty cycle control limited by the matching of the comparator input devices. Native (zero VT) devices are used due to their better threshold voltage matching [9], which can be explained by their lower channel doping (no threshold adjustment implant).

The differential-to-single-ended converter is shown in Fig. 11. The first stage is a wide-bandwidth diode-load differential-gain stage that presents a very low input capacitance. The decision stage is a differential pair with feedback. Feedback is

TABLE I
SAMPLE–RESET PLL PERFORMANCE SUMMARY

Technology	0.18μm CMOS
Frequency range	125-1250 MHz
Frequency resolution	500 kHz
Analog supply voltage	2.5 V
Digital supply voltage	1.5 V
RMS jitter	Less than 0.9% of oscillator period
Power consumption	90 mW from 2.5V supply
Die area (2 PLLs, supply regulators, and bandgap)	300 μm x 800 μm

accomplished with a resistor R_{shunt} that restricts the output swing to within several hundred millivolts of the output inverter trip point. Additional feedback is implemented by inverter $\text{INV}_{\text{shunt}}$ that is carefully matched to the output inverter INV_{out}. $\text{INV}_{\text{shunt}}$ ensures a precise tracking between the trip point of the decision stage and the output buffer. This produces a well-controlled 50% duty cycle over process, temperature, frequency, and supply voltage variation. To obtain high-speed operation, tail currents of several milliamperes are used.

F. Dividers

The feedback and input variable modulus dividers are designed using a pulse swallower architecture. The speed is increased with a divide by two prescalar followed by a synchronous variable modulus divider. The jitter introduced by the feedback divider is reduced with an output flip-flop synchronized at the oscillator output frequency.

VI. INCREASING FREQUENCY RESOLUTION WITH CASCADED PLL CONFIGURATION

The resolution of the output frequency ($f_{\text{out}} = f_{\text{ref}} \cdot M/N$) is given by the feedback (M) and/or input (N) divider modulus ranges. The M divider is included in the feedback loop and therefore directly influences the loop stability. The N divider, though not in the loop, does influence stability through the update period over which the averaging of the proportional path current is performed. A compromise between the high resolution and the high loop bandwidth is achieved by cascading two PLLs.

In magnetic read-channel applications, there are typically two PLLs, a low-resolution servo PLL and a high-resolution data PLL. Boosting the frequency at the input of the high-resolution data PLL up to the maximum output frequency (1.25 GHz) and then dividing it down by the input N divider ensures a wide range for the N divider while maintaining high update frequencies. Operating at high update frequencies allows a high loop bandwidth which minimizes the jitter introduced by the internal oscillators.

Bandwidths of the two PLLs must be carefully selected to minimize overall output jitter. Input jitter gain is related to the ratio of output and input frequencies. Single PLL and cascaded PLL architectures have similar input jitter transfer, if jitter peaking of the two cascaded PLLs does not overlap.

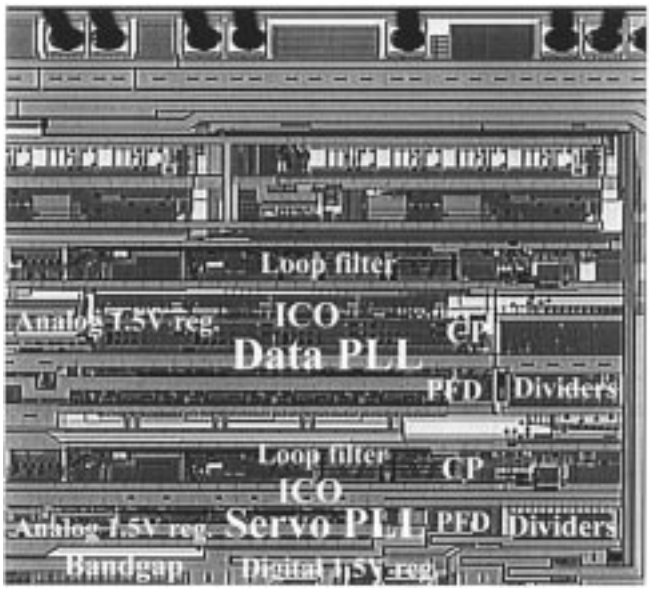

Fig. 12. 0.18-μm CMOS read-channel die photo (PLL detail).

The bandwidth of the high-resolution PLL is designed to be less than or equal to the bandwidth of the low-resolution frequency-boosting PLL. A good choice is to select the two PLL bandwidths to be equal. This choice should not significantly degrade the system jitter transfer performance since the sample–reset architecture provides negligible jitter peaking.

VII. EXPERIMENTAL RESULTS

This sample–reset PLL has been fabricated in a five-metal-layer 0.18-μm CMOS bulk process. Fig. 12 shows a portion of a die photo of the magnetic read-channel chip that uses the sample–reset PLL architecture. Table I summarizes the performance of the sample–reset PLLs.

Fig. 13 shows the simulated transient locking waveforms (integral, proportional, and total oscillator control current) for the sample–reset PLL operating at 1.25 GHz with $B \approx 2$ MHz and $\xi \approx 0.9$ [Fig. 13(a)], in comparison with the waveforms of a standard charge-pump PLL operated at 600 MHz with $B \approx 1$ MHz, natural frequency to stabilizing zero separation of

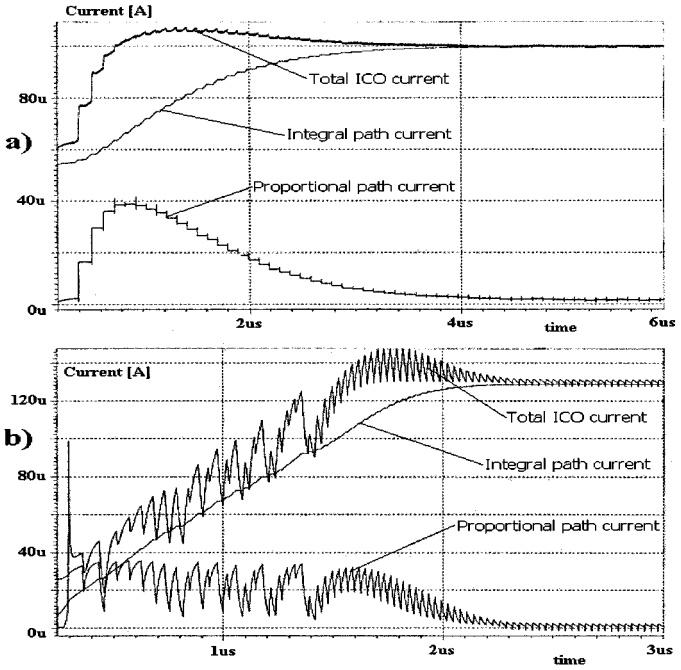

Fig. 13. Transient locking waveforms. (a) Sample–reset PLL. (b) Standard charge-pump PLL.

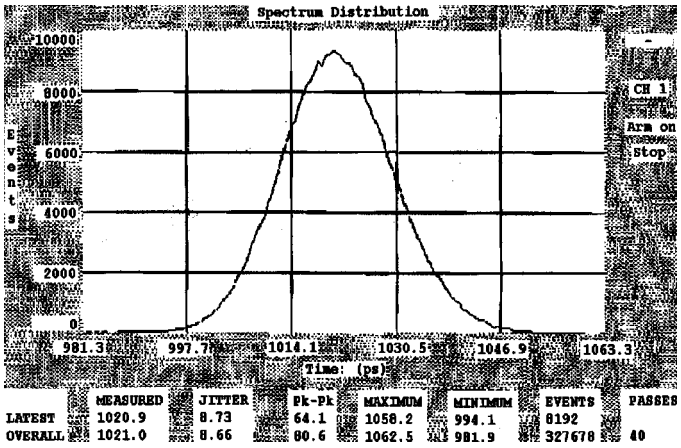

Fig. 14. Measured output jitter for cascaded PLL configuration.

1.8, and a pole-to-zero separation of 25 ($\xi \approx 0.9$) [Fig. 13(b)] used in a previous part. The sample–reset architecture has eliminated the high-amplitude ripple from the proportional current.

Fig. 14 shows the experimentally measured rms jitter of less than 9 ps, for a 1-GHz output for two PLLs connected in cascade, operating in conjunction with noisy digital circuitry ($\approx$100 mV_{pp} supply noise). The measured output jitter of a single sample–reset PLL is comparable with that of two cascaded PLLs. This confirms our initial assumption that the output jitter is dominated by the reference spurs and the supply and substrate injected noise. The jitter improvement is equally contributed by the sample–reset architecture that minimizes the reference spurs and the high PSRR regulators that minimizes the supply-injected noise.

Using native devices with lower substrate transconductance in the signal path and of accumulation capacitors in the loop filter minimizes the substrate injected noise.

The absence of the ripple filtering pole and the high PLL bandwidth (low time constants in the loop filter) lead to smaller on-chip capacitance, reducing the die size of the sample–reset PLL.

VIII. Conclusion

A charge-pump PLL with a sample–reset loop filter has been described. This architecture averages the proportional control current of the oscillator over each update period. Time averaging employs an additional charge pump and a sampling capacitor to generate a constant proportional path current for the entire update period. The major advantage of the sample–reset architecture is the ripple-free staircase shape of the proportional control signal. The control signal does not need additional filtering for low-jitter operation. The PLL is type II with a single stabilizing zero and nearly 90° phase margin. As a consequence, the transient locking has no overshoot, and the input jitter peaking is negligible.

The PLL damping factor is made insensitive to process variations by making it dependent only upon a bandgap voltage and ratios of circuit elements. This ensures tracking between the natural frequency and the stabilizing zero. The stable damping factor and the high update frequency lead to the maximization of the loop bandwidth and low settling time with good rejection of the internal oscillator noise.

To improve jitter performance, several high PSRR regulators are used to bias the different PLL building blocks, and *RC* supply filtering is provided for the blocks with high supply-noise sensitivity.

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