October 31, 2024

ECEN-620: Broadband Circuit Design

Course Projects

Project teams can consist of 1-3 students.
Preliminary report: Due on November 14, 2024
Final report: Due on December 2, 2024

For all projects discussed below, you may use behavioral models for some parts, but critical components (discussed with the professor) must be simulated at transistor level. As a graduate student, you must be able to explain very well the main issues in your project, and what the contributions are.

Suggestions:

Project #1: Design of a 3.2GHz Frequency Synthesizer for Wireless Communications with spurs under -70 dBc
The main specs are:
Frequency step = 8 MHz
VCO continuous tuning range > 5%
Phase noise < -110 dBc at 1 MHz offset
Note: An advanced PLL architecture (advanced PFD/CP interface, loop filter, frac-N synthesizer with Σ–Δ modulation, etc…) must be used to achieve the target spur performance. Just designing an optimized charge pump will most likely not meet the spur specification.

Project #2: Frequency Synthesizer for DTV with channels spread in a 800MHz bandwidth.
The main specs are:
Frequency step = 6 MHz
Frequency range of operation ={50MHz-850 MHz}
Phase noise < -120 dBc at 3 MHz offset

Project #3: High-Performance Quadrature Clock Generator
Frequency = 1 GHz
Quadrature outputs with phase error less than 1°
Jitter < 1 ps_{rms}
Spurs under -50 dBc
Minimize power consumption
Load impedance = 2.5 pF

Project #4: 10Gb/s Clock Generator Data Recovery System
Your choice of sampling clock frequency (1.25GHz – 10GHz)
Compliant with OC-192 mask
Minimize power consumption

Project #5: 10Gb/s Limiting Amplifier
Small-Signal Gain ≥ 50dB
Small-Signal Bandwidth ≥ 10GHz
Integrated Input Referred Noise ≤ 0.5mV_{rms}
Include offset correction
Minimize power
Show eye diagrams before and after limiting amplifier

Project #6: 33Gb/s Multi-Channel Forwarded-Clock Optical Transceiver Design

This project involves the design of the circuits for a high-density multi-channel forwarded-clock optical transceiver. The transmitter should perform an 8:1 serialization operation and drive a ring resonator modulator (RRM) that requires a minimum $1.3V_{ppd}$ swing to achieve a 10dB extinction ratio. The RRMs can be modeled electrically as a 15fF capacitor. The receiver should perform a 1:8 deserialization operation and interface with a photodetector that has 0.8A/W responsivity and 14fF total capacitance. The receiver should achieve -20dBm sensitivity for a BER=10^{-12}. Either global or local clocking circuitry should be designed to produce the necessary CMOS-level clocks at each transmitter channel. At the receive side, a clock channel receives a -20dBm 8.25GHz optical clock signal and must amplify and distribute this again to 31 receiver channels spaced at a 20µm pitch. Either global or local clocking circuitry should be designed to produce the necessary CMOS-level clocks to drive the receiver samplers.

Project #7: 64Gb/s Simultaneous Bidirectional Die-to-Die Multi-Channel Transceiver

This project involves the design of a multi-channel die-to-die transceiver that communicates over a silicon interposer channel with simultaneous bidirectional signaling. The transceiver should be architected as a 13-wire system, with 11 single-ended wires for data transmission at 64Gb/s simultaneous bidirectional and 2 wires for unidirectional $1/8^{th}$-rate forwarded clocks. The transceiver should include 16:1 serialization at the transmitter and 1:16 deserialization at the receiver, along with the transmit driver, receiver front-end, and hybrid circuitry to separate the inbound and outbound signals. The necessary transmit and receive clock generation, distribution, and per-channel deskew circuitry should also be designed.

Project #8: Any other suggestion is more than welcome.

Preliminary Report Required Sections

1. Motivation and Project Overview
2. Literature Survey
3. Proposed Architecture
    a. This can change for the final report
4. Initial Simulation Results
5. Plan of Work
    a. A description of what will be completed for the final report

Final Report Required Sections

1. Motivation and Project Overview
2. Literature Survey
3. Architecture
4. Simulation Results
    a. This section must include a Table comparing your design with current references
5. Conclusion