ECEN620: Network Theory Broadband Circuit Design Fall 2023

Lecture 8: Divider Circuits



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Announcements

• HW3 due Oct 31

Agenda

- Divider Basics
- CML Divider
- Asynchronous vs Synchronous Dividers
- Dual-Modulus Prescalers
- Injection-Locked Dividers

References

- Design of Integrated Circuits for Optical Communications, B. Razavi, McGraw-Hill, 2003.
- Divider papers posted on the website

Analog Charge-Pump PLL Circuits

- Phase Detector
- Charge-Pump
- Loop Filter
- VCO
- Divider



Loop Divider



• Time-domain model

$$\omega_{fb}(t) = \frac{1}{N} \omega_{out}(t)$$

$$\phi_{fb}(t) = \int \frac{1}{N} \omega_{out}(t) dt = \frac{1}{N} \phi_{out}(t)$$

 The loop divider is dimension-less in the PLL linear model

Basic Divide-by-2



- Divide-by-2 can be realized by a flip-flip in "negative feedback"
- Divider should operate correctly up to the maximum output clock frequency of interest PLUS some margin



Divide-by-2 with TSPC FF

True Single Phase Clock Flip-Flop



- Advantages

CLK

OUT

Divider Equivalent Circuit

CLK

Note: output inverter not in left schematic

CLK

- uvantages
- Reasonably fast, compact size, and no static power
- Requires only one phase of the clock
- Disadvantages
 - Signal needs to propagate through three gates per input cycle
 - Need full swing CMOS inputs
 - Dynamic flip-flop can fail at low frequency (test mode) due to leakage, as various nodes are floating during different CLK phases & output states
 - Ex: Q_bar is floating during when CLK is low

CLK 2

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Divide-by-2 with CML FF



- Advantages
 - Signal only propagates through two CML gates per input cycle
 - Accepts CML input levels
- Disadvantages
 - Larger size and dissipates static power
 - Requires differential input
 - Need tail current biasing
- Additional speedup (>50%) can be achieved with shunt peaking inductors

CML Latch



- When the clock is high (M5 on), the input pair (M1 & M2) tracks (linearly amplifies) the input
- When the clock is low (M6 on), the regenerative pair (M3 & M4) latches (with positive feedback) the state

CML Latch



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- When the clock is low (M6 on), the regenerative pair (M3 & M4) latches (with positive feedback) the state
- This regenerative pair continues to provide gain in the store mode, allowing for short cycle operation
- The minimum cross-coupled pair gain to hold the state is $g_{m3,4}R_D > 1$

Optimized CML FF for High-Speed Dividers



- The cross-coupled pair gate and drain capacitances slow down the latch/flip-flop
- If the flip-flop is switching at high-speed, the regenerative pair gain can actually have a loop gain less than unity due to the short hold state
- One way to achieve this is by using a different current in the track state (I_{SS1}) and the hold state (I_{SS2}), allowing for smaller regeneration transistors when $I_{SS2} < I_{SS1}$

CML Latch Swing Control



- If suitable resistors are not available in a certain process, the PMOS triode-region loads can be used
- Due to PVT variations, feedback control is generally required to maintain the desired CML logic swing level
- A replica circuit produces the required PMOS gate bias to insure the desired CML logic swing for a given I_{ss}
- Note, triode PMOS loads will generally have more parasitic capacitance than linear resistors, resulting in a slower circuit

CML Latch with PMOS Diode Loads



- PMOS diode loads may allow for simpler biasing over PVT variations
- One issue with this is the large headroom (|VTP|+VOD) required to turn-on the PMOS diode
 - NMOS source followers can allow for similar headroom as with triode loads

CML Latch with PMOS Diode Loads



- PMOS diode loads may allow for simpler biasing over PVT variations
- One issue with this is the large headroom (|VTP|+VOD) required to turn-on the PMOS diode
 - NMOS source followers can allow for similar headroom as with triode loads
- Another issue stems from the highly non-linear effective resistance which can introduce inter-symbol interference for random data
 - Note, this is not an issue for periodic switching divider applications

CML Divider Clock Swing vs Frequency



- Interestingly, the divider minimum required clock swing can actually decrease with frequency
- This is due to the feedback configuration of the divider yielding an effective ring oscillator topology that will naturally oscillate at certain frequency
- Near this frequency, the input clock amplitude can be very low
- For frequencies above this natural oscillation frequency, the minimum clock input amplitude increases

Divider Circuit Style Partitioning



- CML dividers operate at the highest speed, but their static power consumption reduces efficiency at lower speeds
- For large divide ratios, a mixture of CML and static CMOS dividers are often used
- The first fastest fixed dividers (prescalers) are CML, while the following lower frequency dividers are static CMOS

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Binary Dividers: Asynchronous vs Synchronous

Asynchronous Divider



- Advantages
 - Each stage runs at lower frequency, resulting in reduced power
 - Reduced high frequency clock loading
- Disadvantage
 - Jitter accumulation
- Advantage
 - Reduced jitter
- Disadvantage
 - All flip-flops work at maximum frequency, resulting in high power
 - Large loading on high frequency clock

Synchronous Divider



Jitter in Asynchronous vs Synchronous Dividers

Asynchronous



- Jitter accumulates with the clock-to-Q delays through the divider
- Extra divider delay can also degrade PLL phase margin

Synchronous



- Divider output is "sampled" with high frequency clock
- Jitter on divider clock is similar to VCO output
- Minimal divider delay

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Dual Modulus Prescalers



 For /15, first prescaler circuit divides by 3 once and 4 three times during the 15 cycles

÷128/129 Dual-Modulus Prescaler



- For /129, first prescaler circuit divides by 5 once and 4 thirty-one times during the 129 cycles
- The synchronous ÷4/5 block with the extra NAND logic limits the maximum operating frequency and has 3 flip-flops operating at the maximum speed

Phase-Switching Dual-Modulus Prescaler



- In order to ÷129, instead of adding an extra highfrequency cycle in a ÷4/5 block, simply delay the phase of the ÷4 signal by 90°
- Allows for a fully-asynchronous design with only 1 flip-flop operating at the maximum speed
- Needs quadrature phase outputs at the ÷4 outputs

Adding an Extra Cycle with a 90° Shift

- A differential Master/Slave flip-flop provides quadrature signals at the latch outputs
- Every 128 cycles, delay the ÷4 signal by 90° to yield a divide by 129 output



[Craninckx JSSC 1996]



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Watch Out For Glitches!

- There is the potential for glitches at the output of the phase selector during lowfrequency operation, causing the divider to fail
- This is solved by insuring a minimum rise time (slowing down C0), such that the block selects a signal when it has a sufficient high value





÷128/129 Phase-Switching Dual-Modulus Prescaler

[Craninckx JSSC 1996]





Time [500psec/div] Dual modulus division

- In a 0.7um CMOS process achieved
 - 2.65GHz operation with 5V power supply
 - 1.75GHz operation with 3V power supply

Improved Glitch Robustness Using ÷8 Signals



- Using ÷8 signals and switching 45° allows for improved glitch robustness
- Requires two parallel ÷2 blocks
- Careful! These two ÷2 blocks have two possible phase relationships
- Need to detect this relationship to determine the appropriate phase switching order



[Shu JSSC 2003]

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Injection-Locked Frequency Dividers



Ring-oscillator type (/3)



[Verma JSSC 2003, Rategh JSSC 1999]

[Lo CICC 2009]

- Superharmonic injection-locked oscillators (ILOs) can realize frequency dividers
- Faster and lower power than flip-flop based dividers
- Injection locking range can be limited

LC-Oscillator-Based ILFDs

- Advantages
 - Better noise performance (LC filtering)
 - Low power consumption
 - Very high operation frequency (~ f_{max})
- Disadvantages
 - Smaller locking range (LC limited)
 - Unwanted harmonics
 - Large silicon area due to L and C
 - Very difficult to provide multiple phases or large divisor number in one LC oscillator stage (area penalty)
 - Difficult to find an excellent source to inject signal

Ring-Oscillator-Based ILFDs

Advantages

- Smaller area
- Wide locking range
- Small power consumption

Disadvantages

- Inferior phase noise to LC ILFDs (Still decent)
- Worse unwanted harmonics (No LC resonant filtering)
- False locking

Complementary Injection-Locked Frequency Divider

- Large odd-modulus
- Only dynamic power consumption
- 100% frequency locking range
- Differential input/output
- 50% duty cycle
- Small area

/3,5,7,...



Complementary Injection Scheme



- Complementary injection reinforces the injection strength to widen the frequency locking range
- Only when the inverter transits state the tail transistors inject current
- Independent tail injection to each stage avoids the interference between each stage

Locking Range (Input Sensitivity)

Divide-by-3 operation

Divide-by-15 operation



 Over 100% locking range (Post-layout simulation in 0.18 µm CMOS technology)

Power Consumption & Phase Noise

- Power consumption
 - One ring-oscillator stage:
 - **CILFD:** $P_{Total} \cong 2CV_{DD}^2 f_{Inj}$

$$P_{Stage} \cong CV_{DD}^2 f_{Inj} \left(\frac{1}{2n+1}\right)$$

- Power consumption is independent of the division modulus (number of delay elements)
- CILFD phase noise is mainly determined by the injection signal phase noise



From top to bottom:(1) free running CILFD(2) incident signal(3) locked CILFD

Conclusion

- Divider should operate correctly up to the maximum output clock frequency of interest plus some margin
- TSPC flip-flop dividers require only one clock phase, are compact, consume no static power, and are reasonably fast
- CML flip-flop dividers can achieve higher speed at the cost of static power consumption and higher area
- Dividers are often partitioned into CML/CMOS and synchronous/asynchronous
- Injection-locked dividers achieve the highest operating frequencies, but have a limited locking range

Next Time

• Digital PLLs