

# ECEN620: Network Theory Broadband Circuit Design Fall 2024

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## Lecture 4: Phase Detector Circuits



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# Announcements

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- HW1 due Sept 12, 11:59PM
  - Turn in via Canvas

# Agenda

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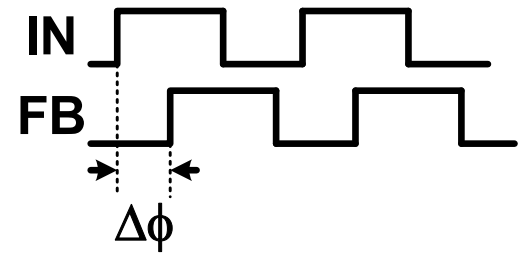
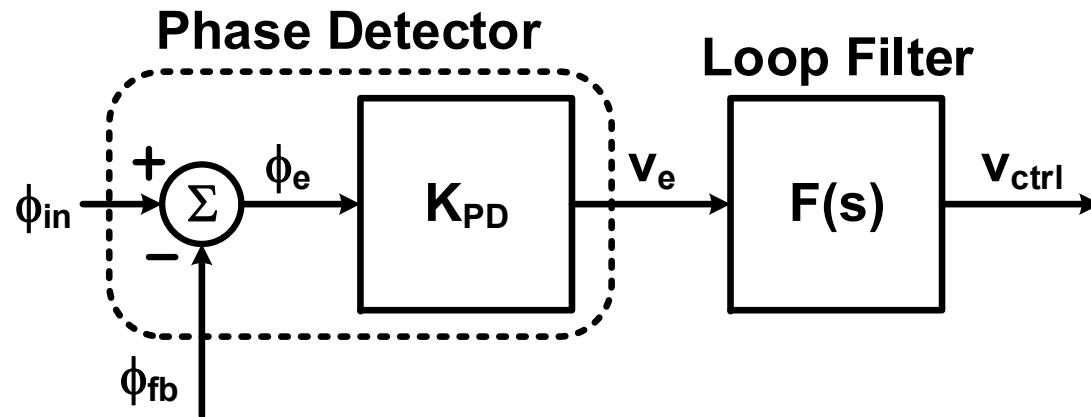
- Phase Detector Circuits
  - Mixer PD
  - XOR PD
  - J-K Flip-Flop PD
  - Phase-Frequency Detector (PFD)

# References

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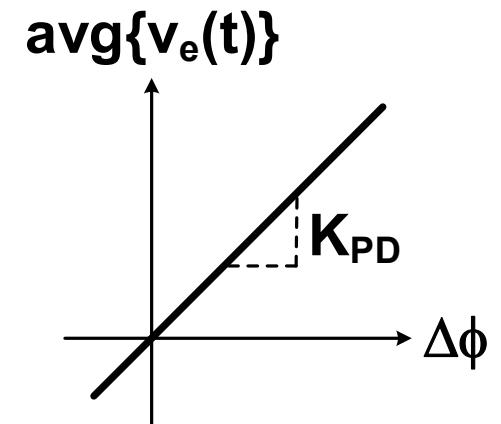
- *RF Microelectronics*, B. Razavi, Prentice Hall, 1998.
- *Design of Integrated Circuits for Optical Communications*, B. Razavi, McGraw-Hill, 2003.
- *Monolithic Phase-Locked Loops and Clock Recovery Circuits*, B. Razavi, Wiley, 1996.
- M. Perrott, *High Speed Communication Circuits and Systems Course*, MIT Open Courseware

# Phase Detector



$$\text{avg}\{v_e(t)\} = K_{PD}\Delta\phi$$

- Detects phase difference between feedback clock and reference clock
- The loop filter will filter the phase detector output, thus to characterize phase detector gain, extract average output voltage
- The  $K_{PD}$  factor can change depending on the specific phase detector circuit

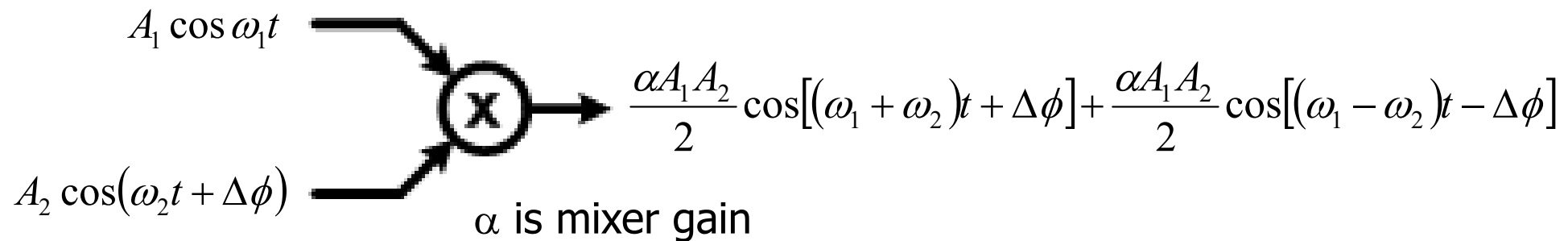


$K_{PD}$  units are V/rad when used with a dimension - less filter

$K_{PD}$  units are  $\text{rad}^{-1}$  (averaged) or A/rad when combined with the charge - pump

when used with a impedance filter

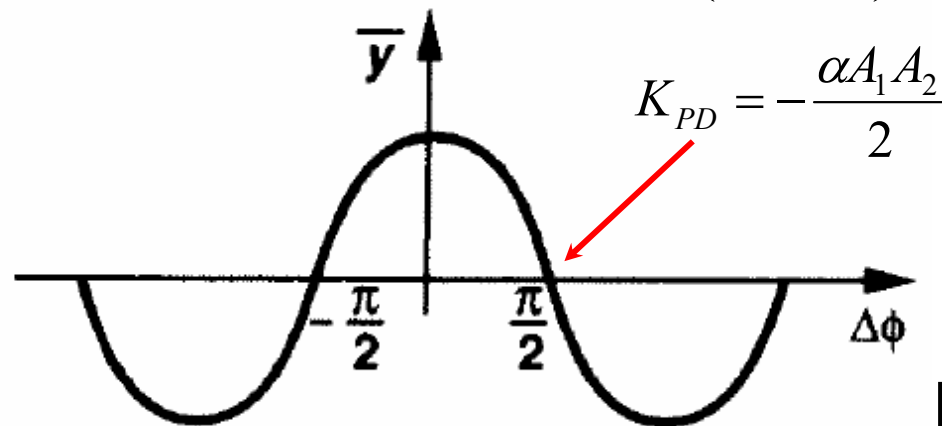
# Analog Multiplier Phase Detector



- If  $\omega_1 = \omega_2$  and filtering out high-frequency term

$$\overline{y(t)} = \frac{\alpha A_1 A_2}{2} \cos \Delta\phi$$

- Near  $\Delta\phi$  lock region of  $\pi/2$ :  $\overline{y(t)} \approx \frac{\alpha A_1 A_2}{2} \left( \frac{\pi}{2} - \Delta\phi \right)$



[Razavi]

# Analog Mixer PD Properties

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- The nominal lock point (zero frequency offset or Type-2) with a mixer PD is a  $90^\circ$  static phase shift
  - For many applications this is unimportant or can be cancelled elsewhere
- The mixer cannot serve as a frequency detector, as on average the output will be zero for a frequency difference
- $K_{PD}$  is a function of the input amplitude, which is not desired

# Mixer Circuits

## Active Mixers

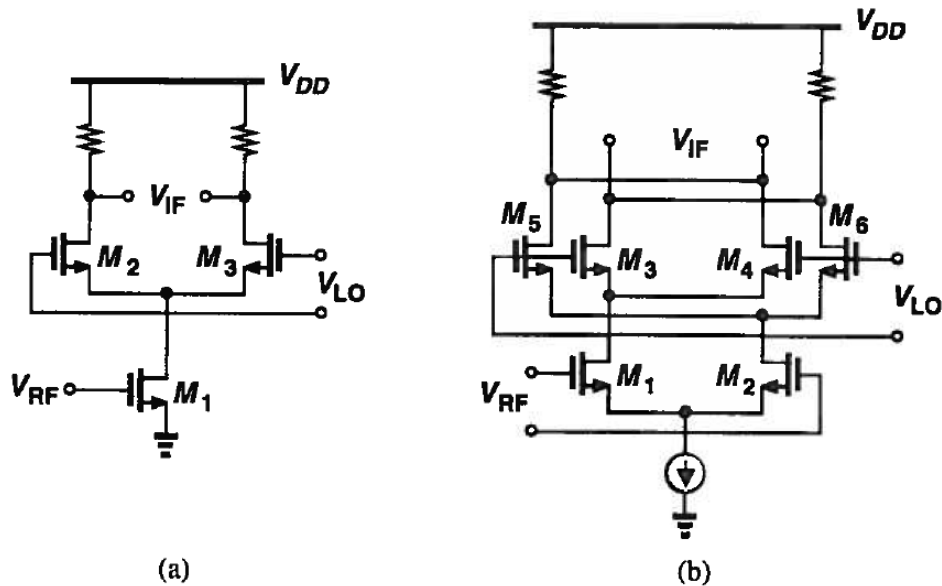
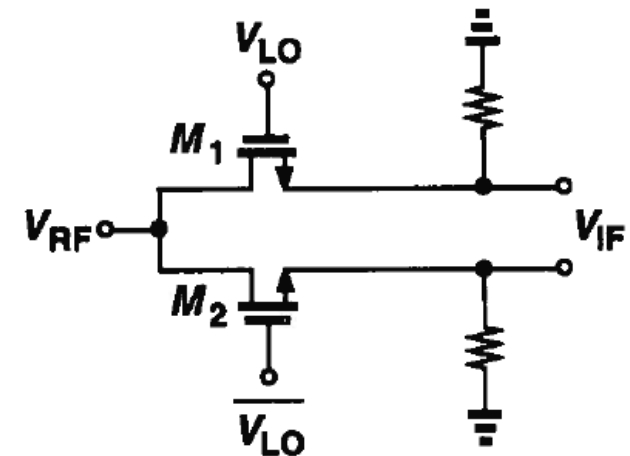


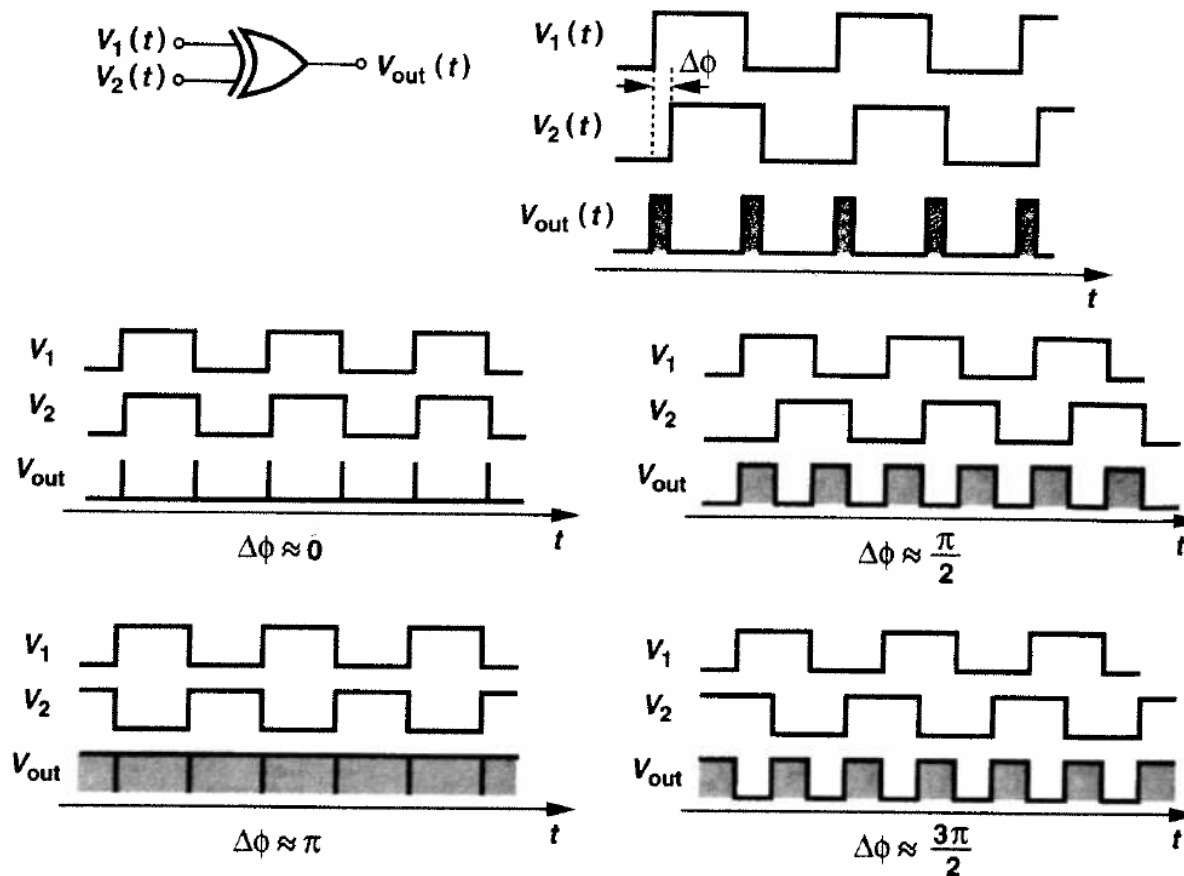
Figure 6.19 (a) Single-balanced mixer, (b) double-balanced mixer.

## Passive Mixer





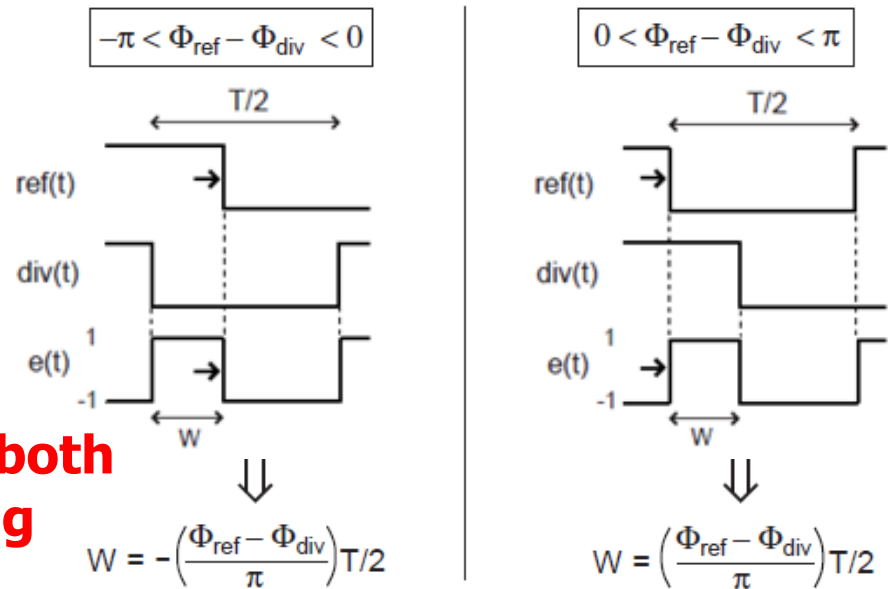
# XOR Phase Detector



[Razavi]

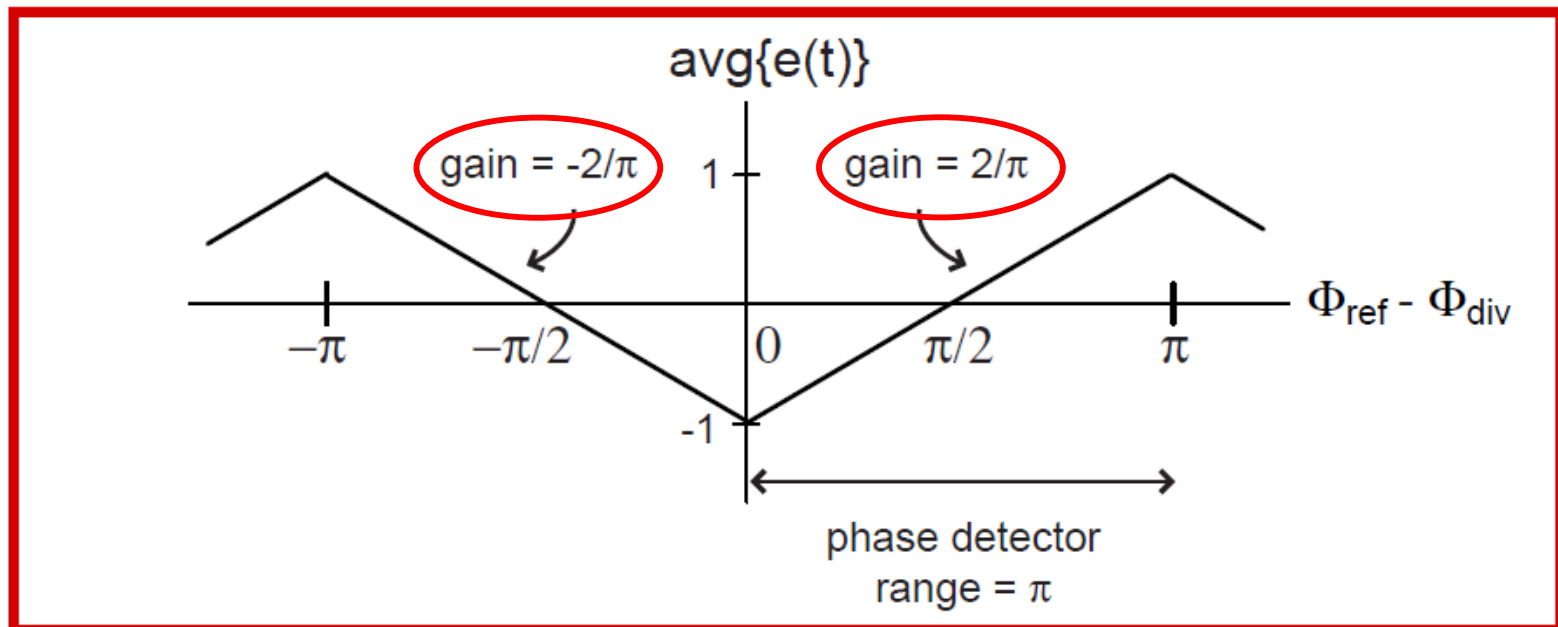
- Assuming logic 1="+1" and 0="-1", the XOR PD will lock when the average output is 0
  - Generally,  $\pi/2$  is a stable lock point and  $-\pi/2$  is a metastable point
- Sensitive to clock duty cycle

# XOR Phase Detector

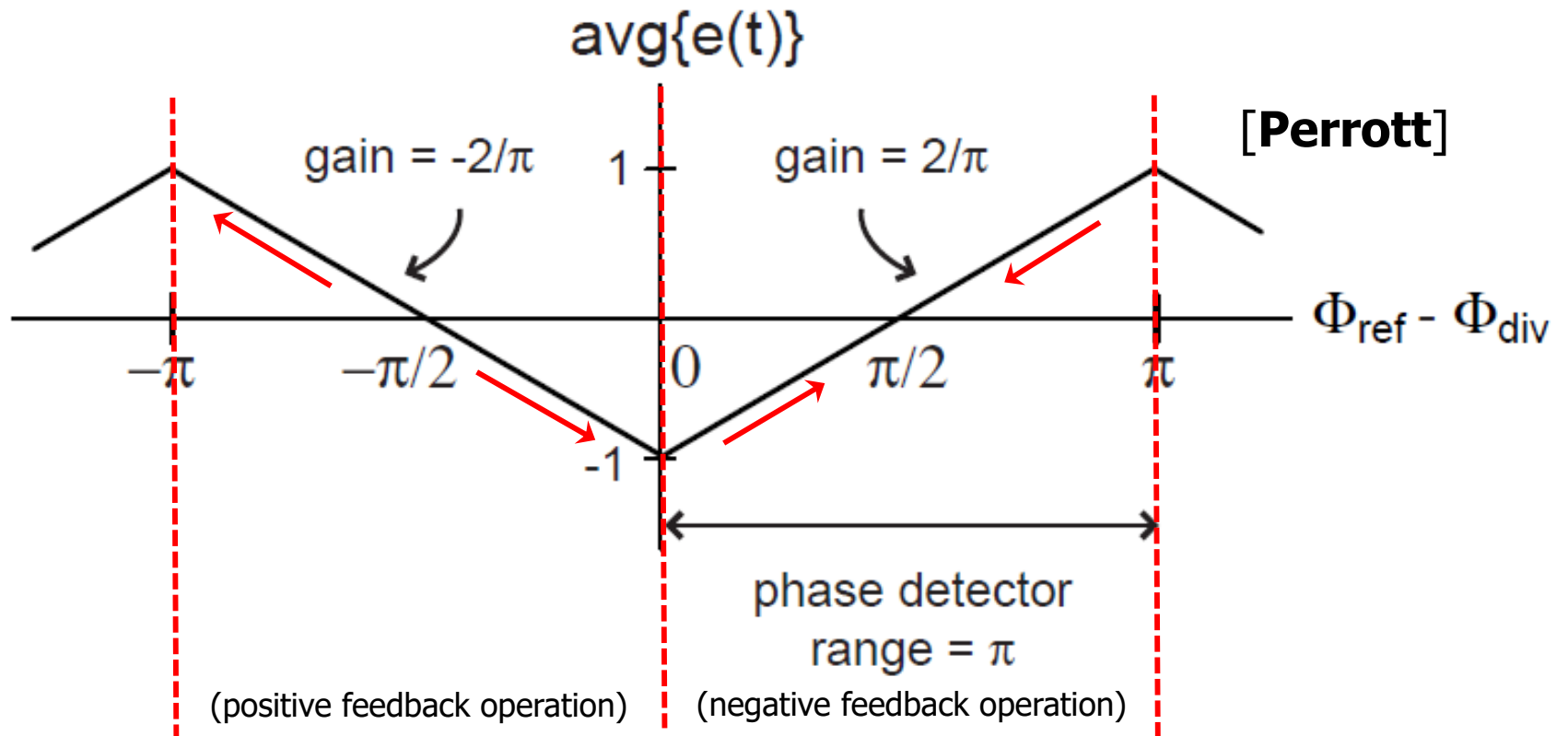


**Width is same for both leading and lagging phase difference!**

**[Perrott]**



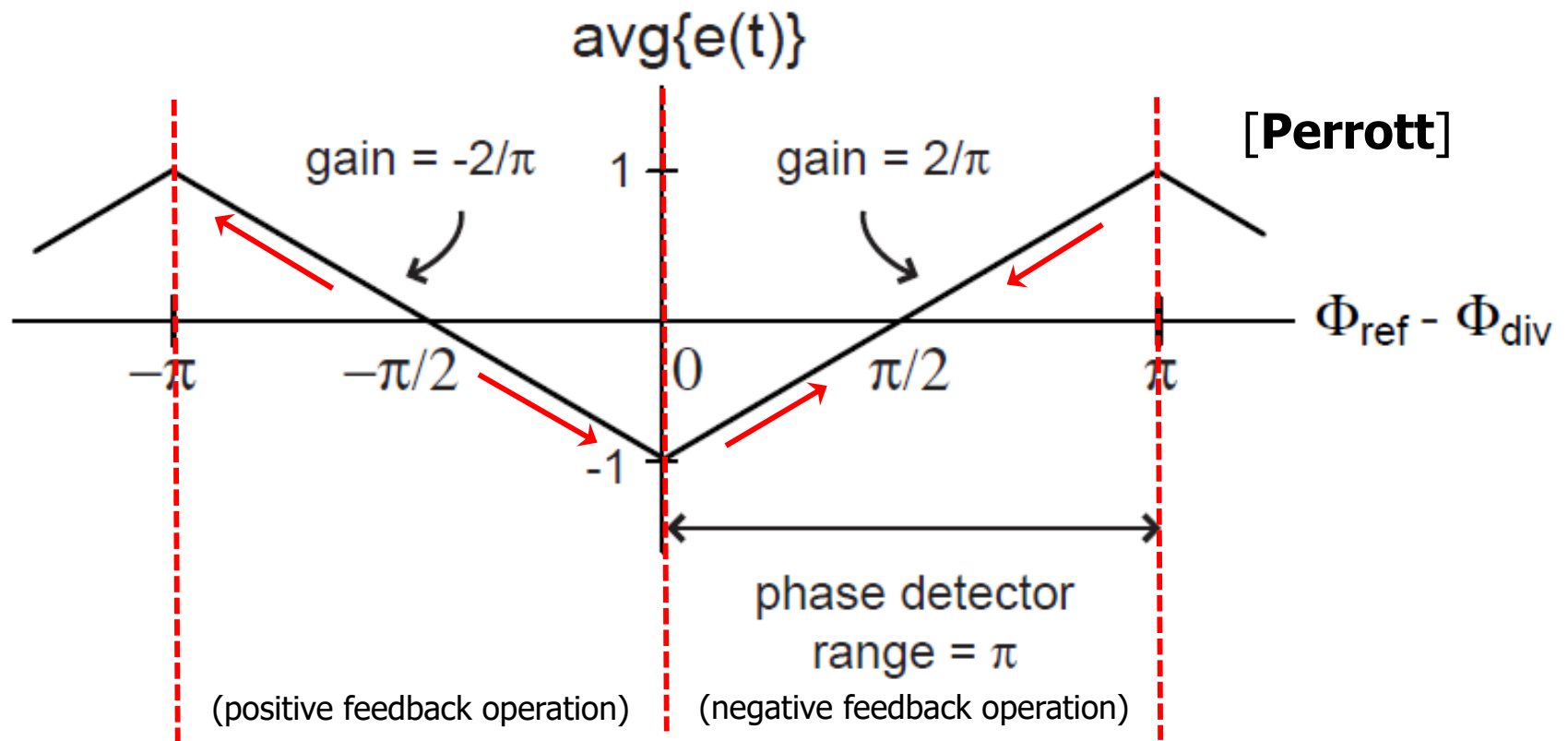
# Stable vs Metastable Lock Point



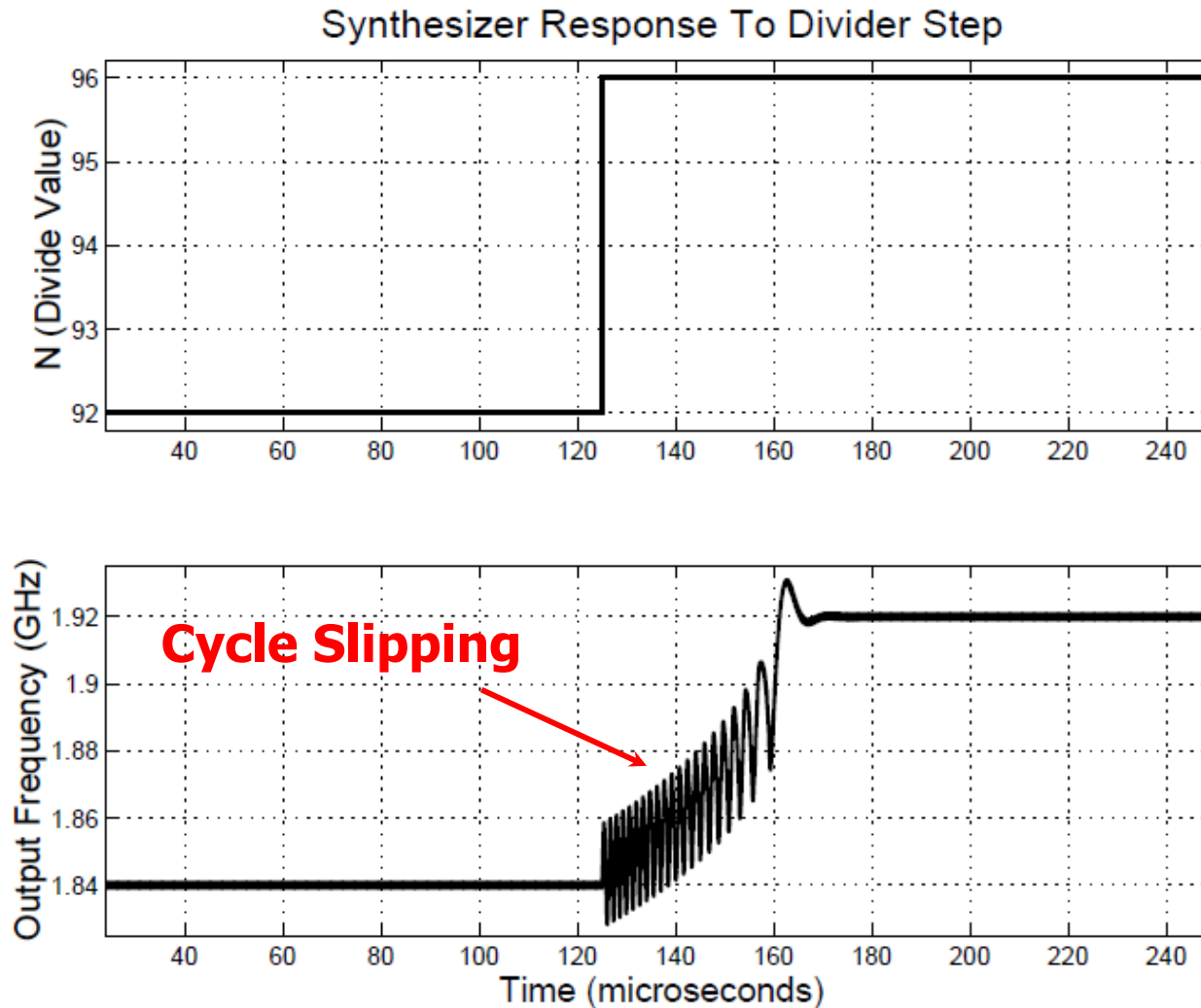
- The PLL should be configured in negative feedback based on the phase detector gain
- However, the phase detector gain varies as a function of the phase error
- Generally, the PLL is designed to have a stable lock point with a  $\pi/2$  phase offset
  - $-\pi/2$  is a metastable lock point because it is in a positive feedback operation range

# Cycle Slipping

- If there is a frequency difference between the input reference and PLL feedback signals the phase detector can jump between regions of different gain
  - PLL is no longer acting as a linear system



# Cycle Slipping



[Perrott]

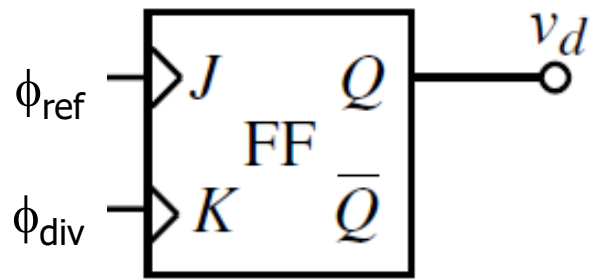
- If frequency difference is too large the PLL may not lock

# XOR PD Properties

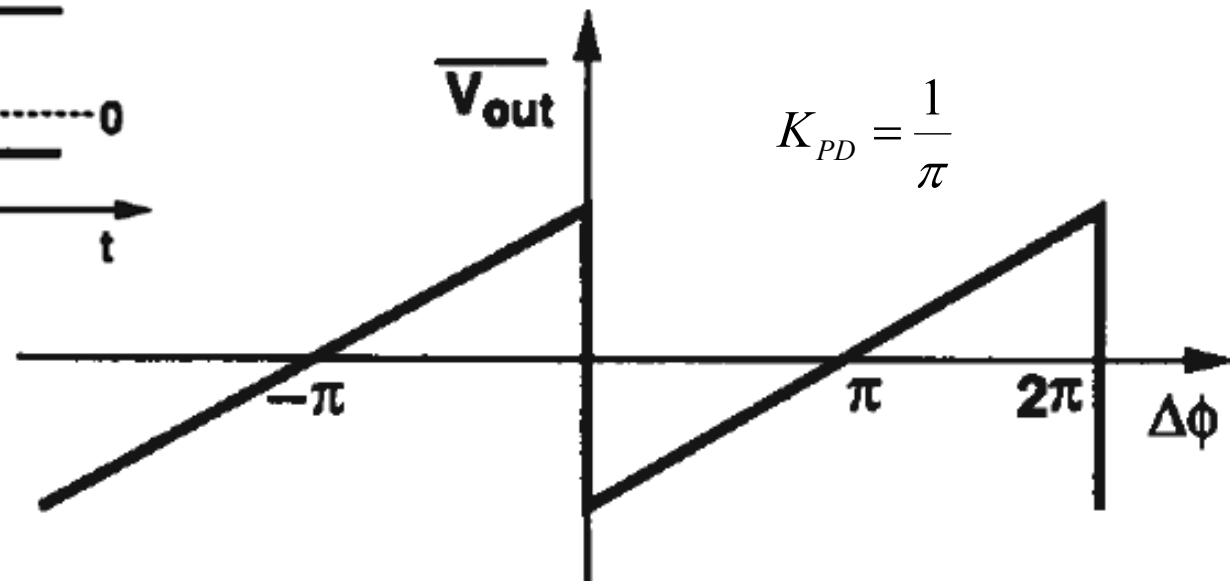
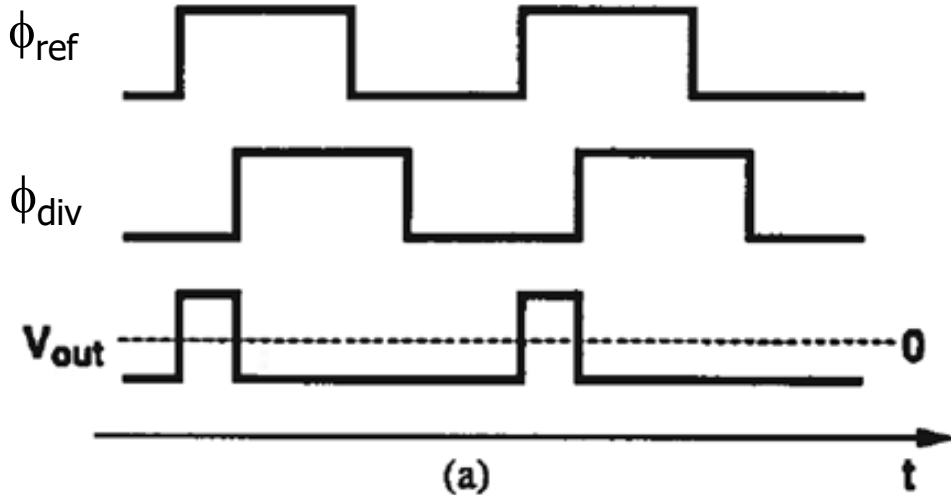
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- The nominal lock point with an XOR PD is also a  $90^\circ$  static phase shift
- Unlike the analog mixer,  $K_{PD}$  is independent of input amplitude and constant over a  $\pi$  phase range
- The XOR PD is sensitive to input duty cycle, and will lock with a phase error if the input duty cycles are not 50%

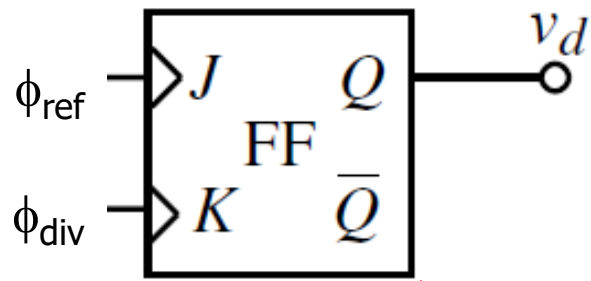
# J-K Flip-Flop Phase Detector



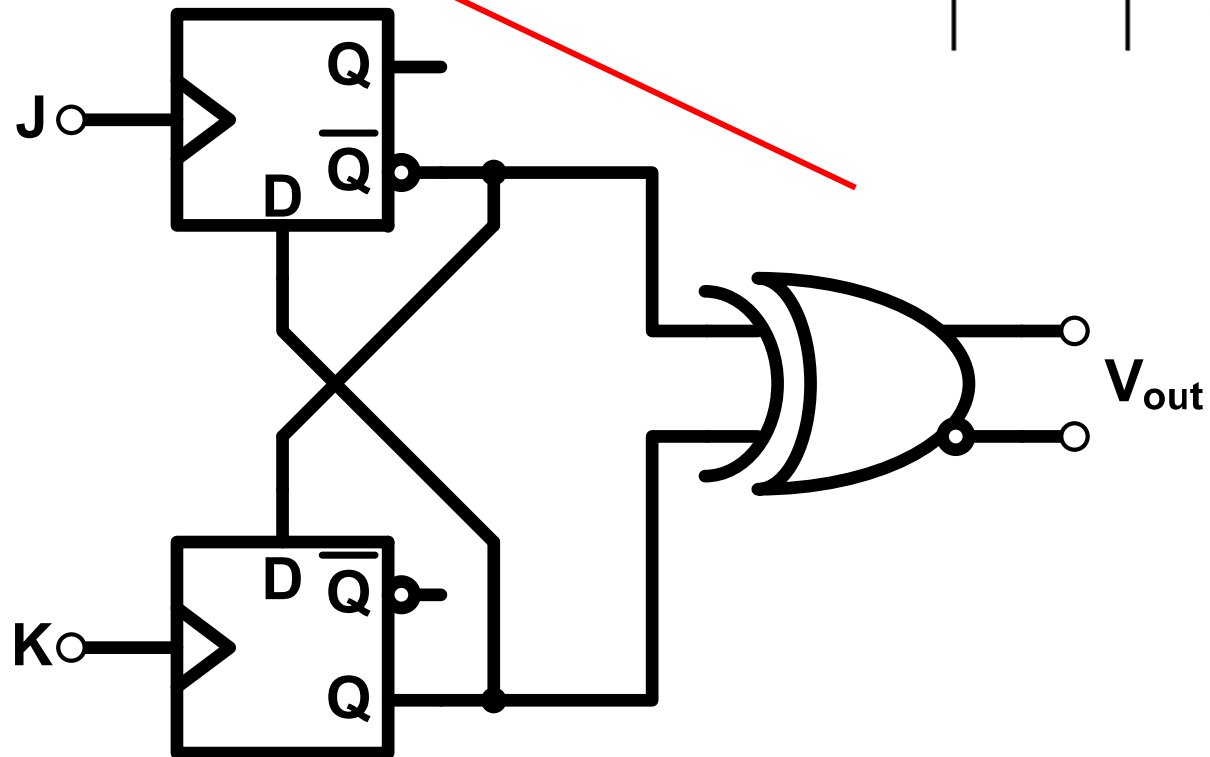
J	K	$Q_{n+1}$
0	0	$Q_n$
0	1	0
1	0	1
1	1	$\overline{Q_n}$



# J-K Flip-Flop Details



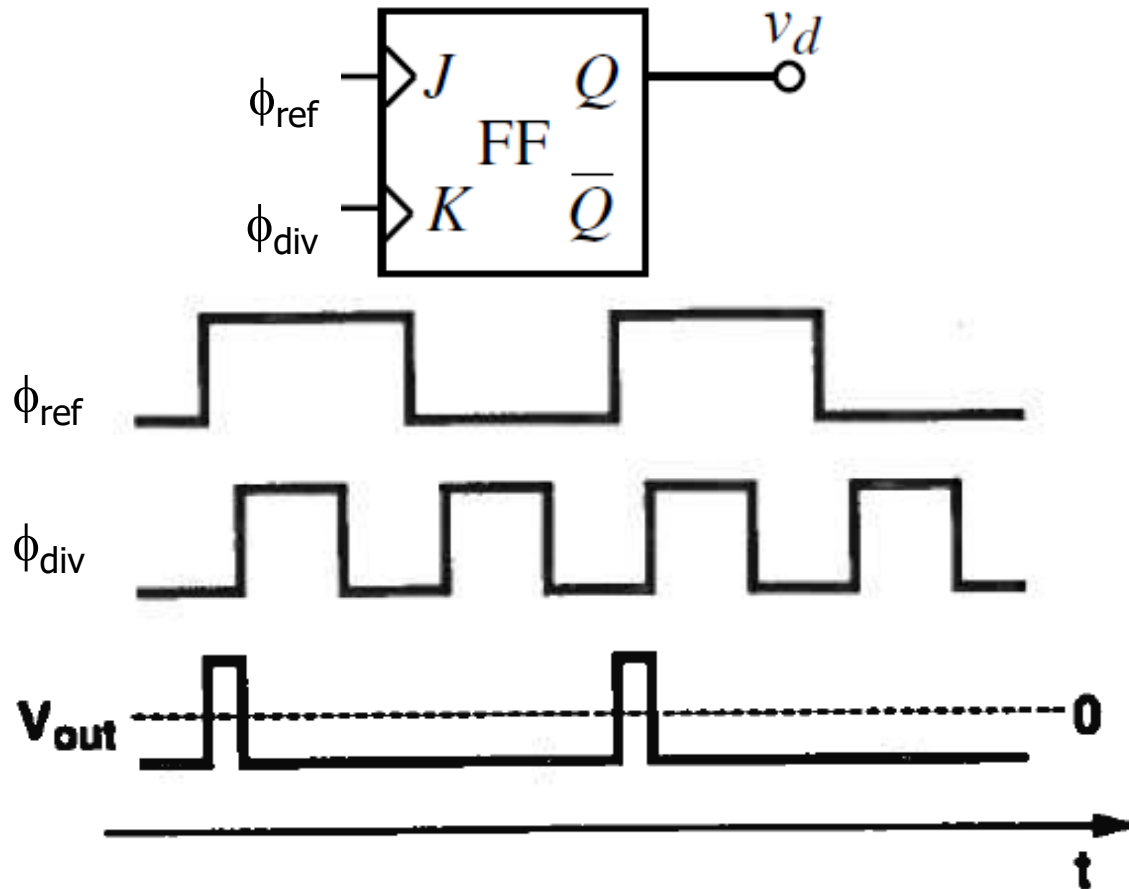
J	K	$Q_{n+1}$
0	0	$Q_n$
0	1	0
1	0	1
1	1	$\overline{Q_n}$





# J-K Flip-Flop Phase Detector Harmonic Locking

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- Harmonic signals can display the same DC output, leading to potential locking to harmonics

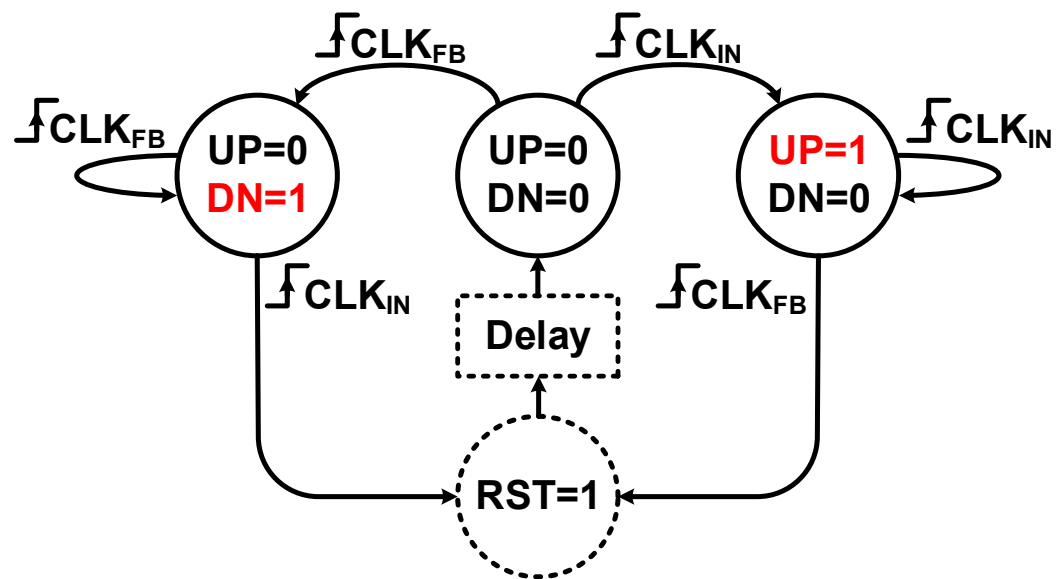
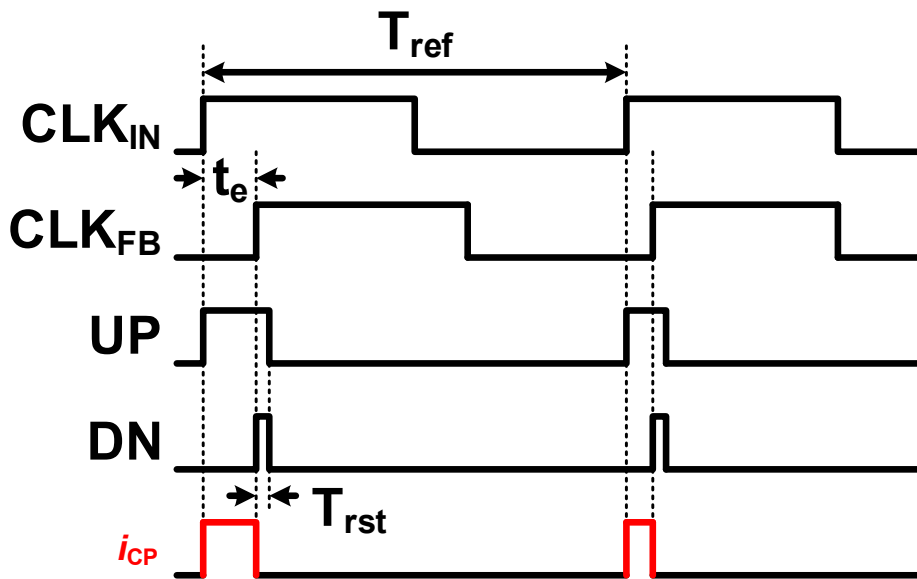
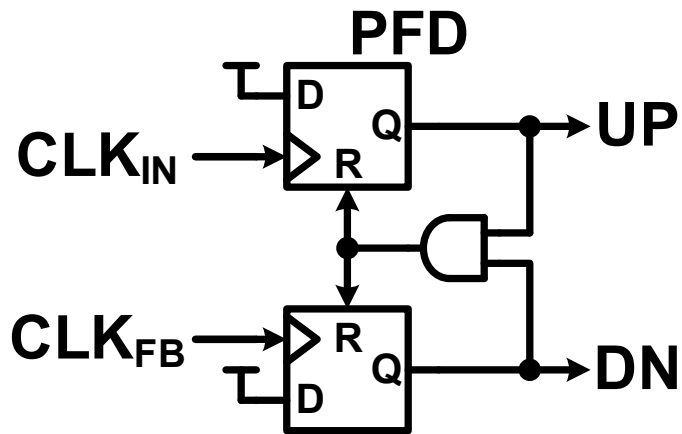
# J-K Flip-Flop PD Properties

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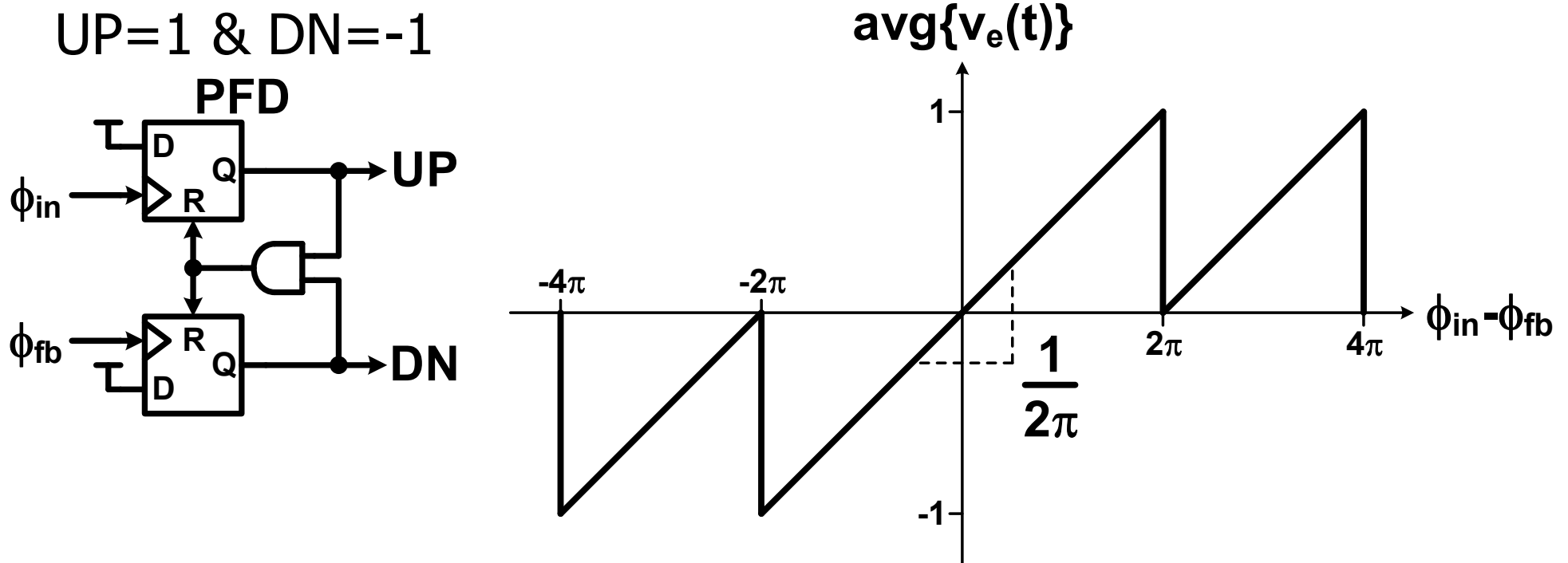
- The nominal lock point with an J-K Flip-Flop PD is a  $180^\circ$  static phase shift
- The J-K Flip-Flop PD is not sensitive to input duty cycle
- The J-K Flip-Flop displays a constant KPD over a  $2\pi$  range
- There is the potential to lock to harmonics of the reference clock

# Phase Frequency Detector (PFD)

- Phase Frequency Detector allows for wide frequency locking range, potentially entire VCO tuning range
- 3-stage operation w/ UP & DN outputs
- Rising edge-triggered results in duty cycle insensitivity

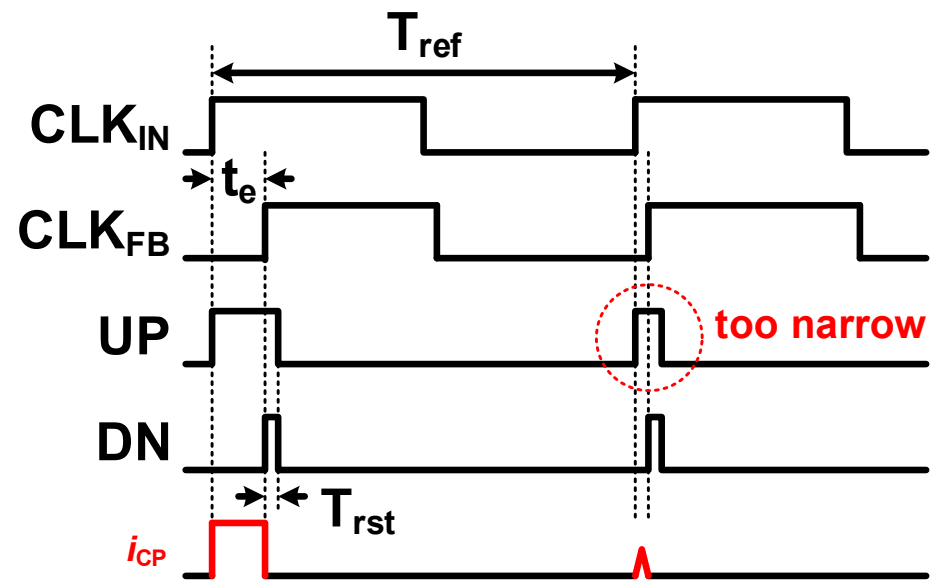
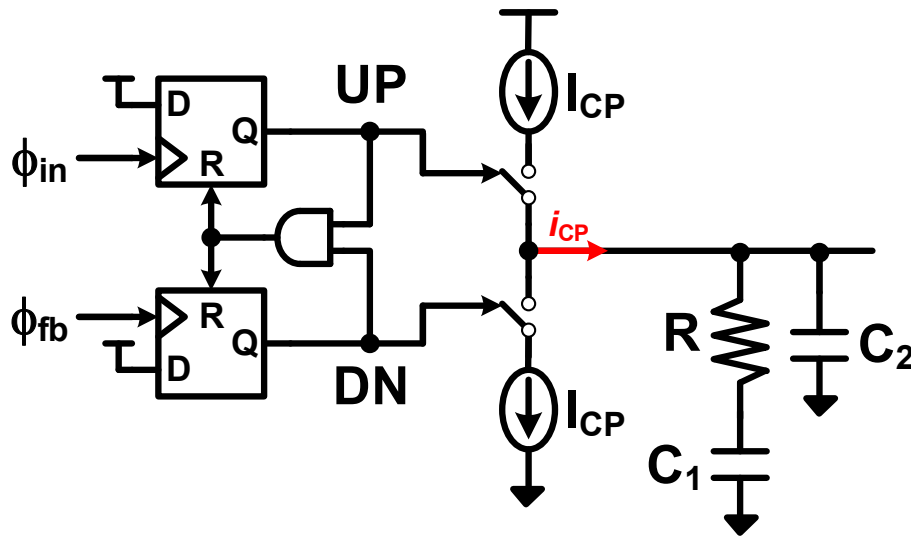


# Averaged PFD Transfer Characteristic

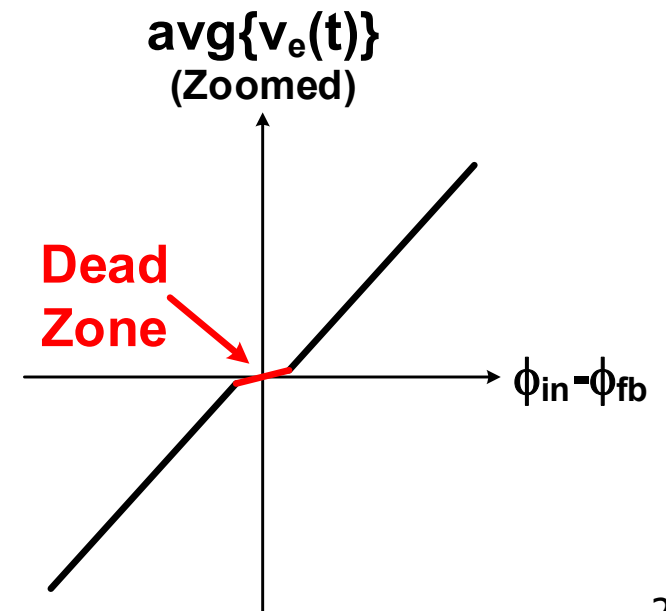


- Constant slope and polarity asymmetry about zero phase allows for wide frequency range operation
- The averaged PFD gain is  $1/(2\pi)$  with units of  $\text{rad}^{-1}$

# PFD Deadzone

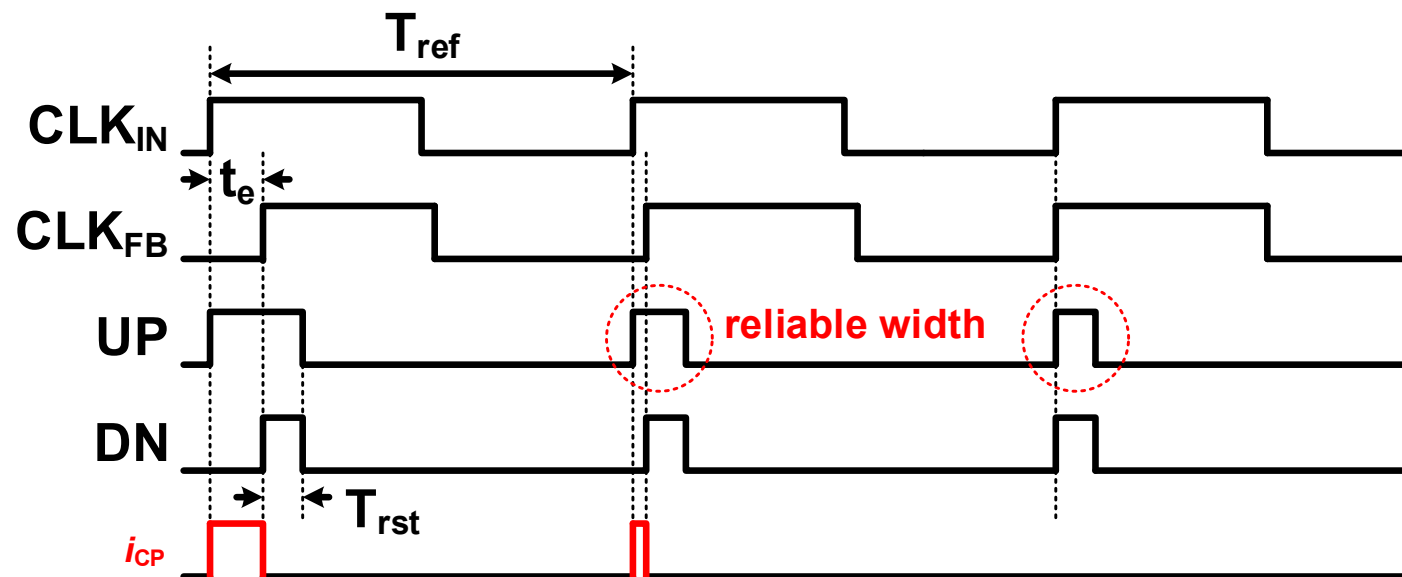
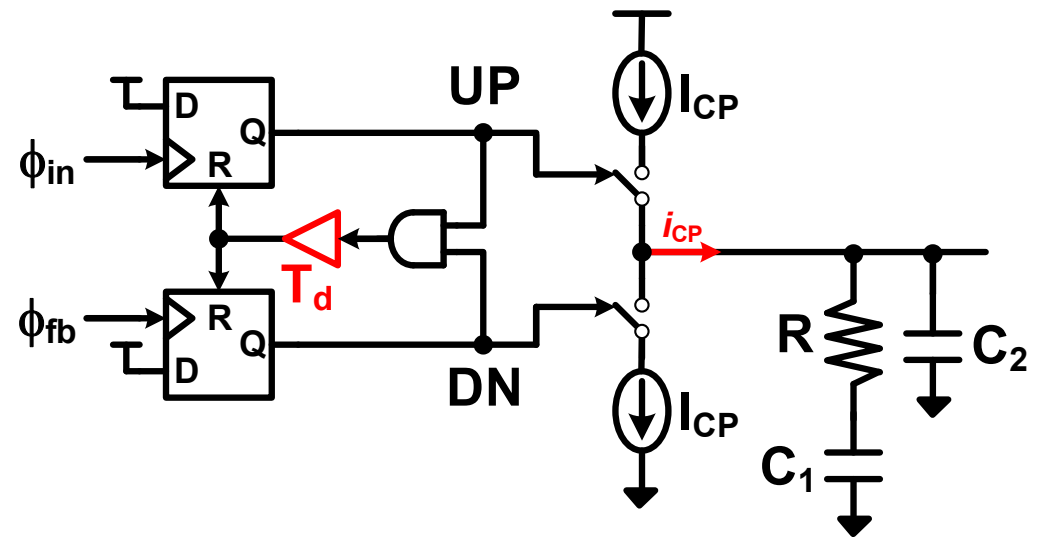


- If phase error is small, then short output pulses are produced by PFD
- Cannot effectively propagate these pulses to switch charge pump
- Results in phase detector "dead zone" which causes low loop gain and increased jitter



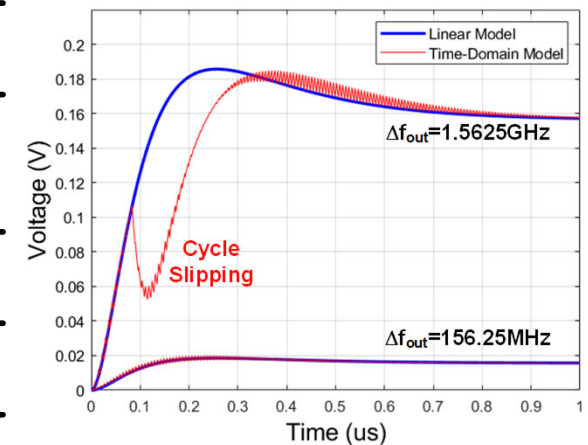
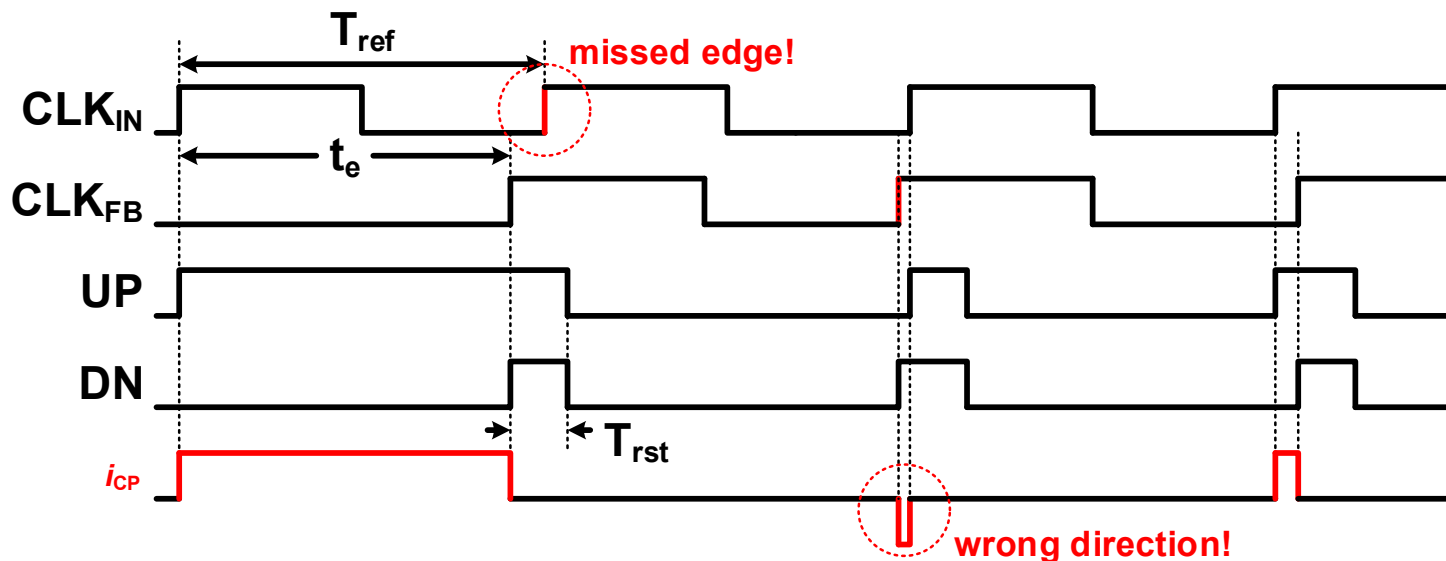
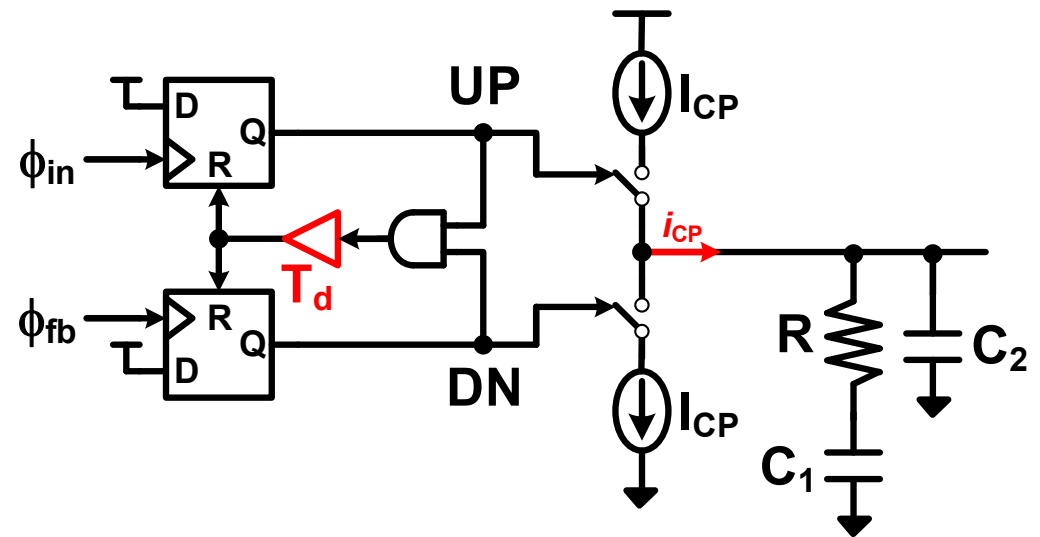
# PFD Operation w/ Reset Delay

- Solution is to add delay in PFD reset path to force a minimum UP and DN pulse length
- In locked state both UP and DN current sources are on for  $T_{rst}$  but ideally no net current is delivered to loop filter

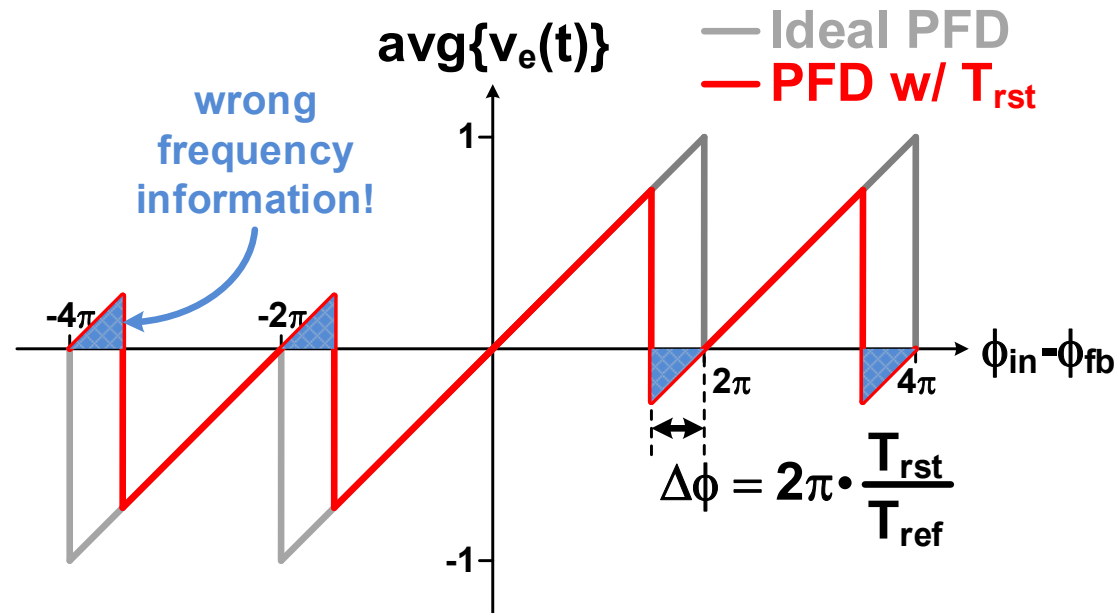


# Problems Near $2\pi$

- PFD cannot react to input rising edges during reset
- This can result in the next rising edge driving the loop in the wrong direction
- Reset delay can increase acquisition time and sets a max PFD operating frequency



# PFD Transfer Characteristic w/ Reset Delay



- PFD reset delay generates wrong frequency information
- If this becomes a large percentage of the reference cycle, then the PFD can fail to acquire frequency lock

$$\text{Max } T_{rst} = \frac{T_{ref}}{2}$$

$$\text{Max PFD Frequency} = \frac{1}{2T_{rst}}$$

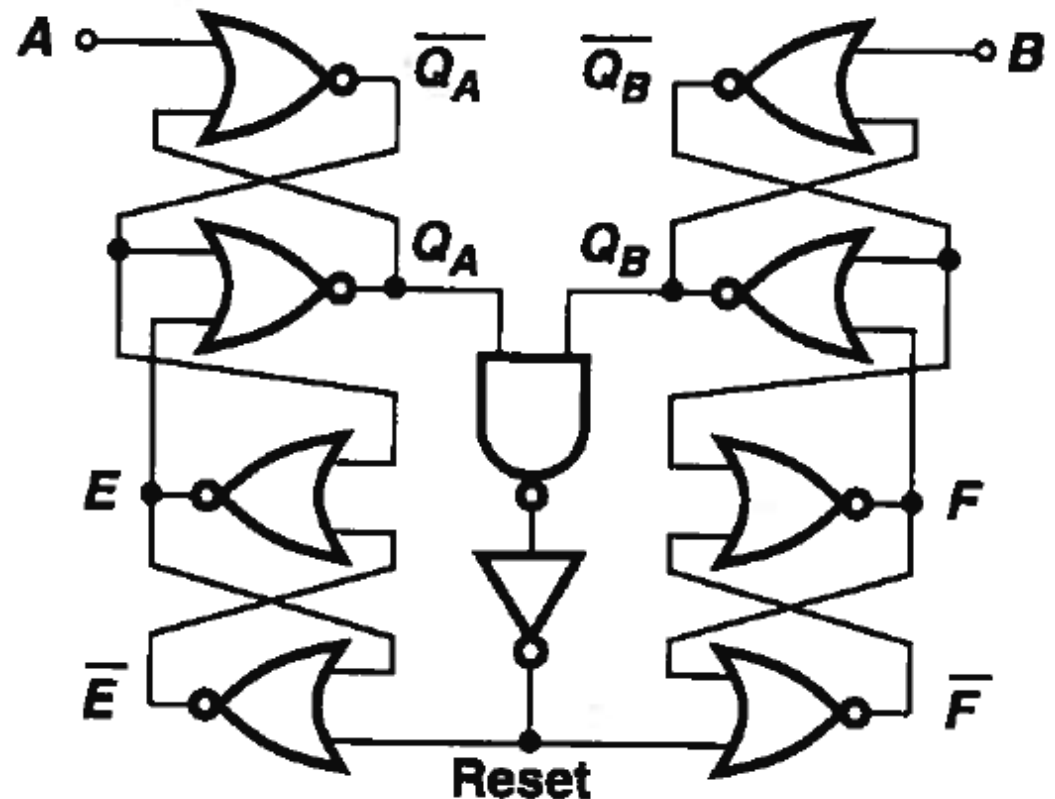
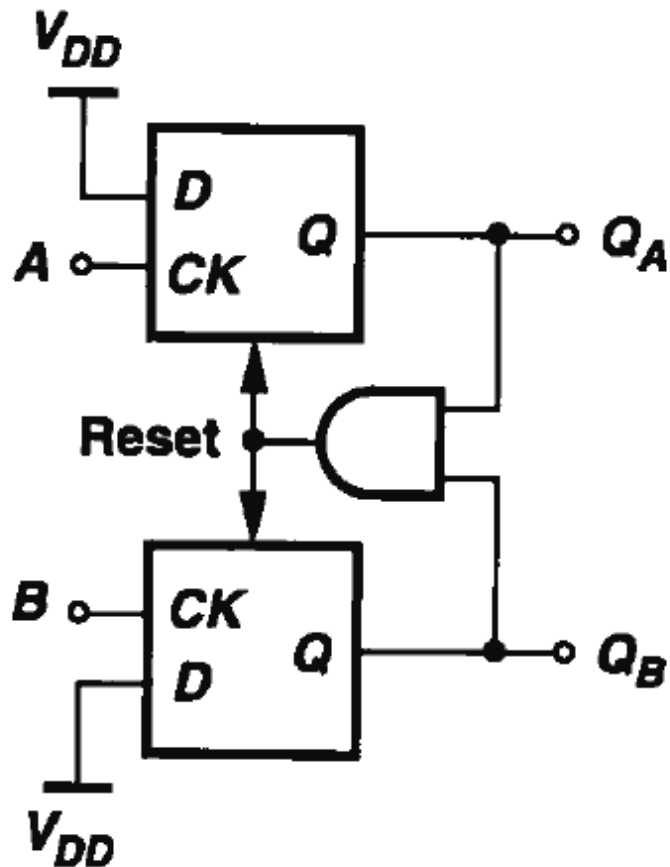


# PFD Properties

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- The nominal lock point with a PFD is  $0^\circ$
- The PFD is not sensitive to input duty cycle
- The PFD outputs "UP" and "DN" are not complementary and stay high until reset by the other, allowing for efficient frequency detection
- Near lock, the propagation of narrow pulses to switch the charge pump can cause a phase detector "dead zone"
  - To prevent this, extra delay is generally inserted in the PFD reset path

# Detailed Optimized PFD Schematic



- Because the flip-flop data input is always "1", the logic can be optimized for higher speed operation

# Next Time

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- Charge Pump Circuits