ECEN620: Network Theory
Broadband Circuit Design
Fall 2014

Lecture 3: PLL Analysis

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Agenda & Reading

- PLL Overview & Applications
- PLL Linear Model
- Phase & Frequency Relationships
- PLL Transfer Functions
- PLL Order & Type

- Reading
  - Chapter 2, 3, 5, & 12 of *Phaselock Techniques,* F. Gardner, John Wiley & Sons, 2005.

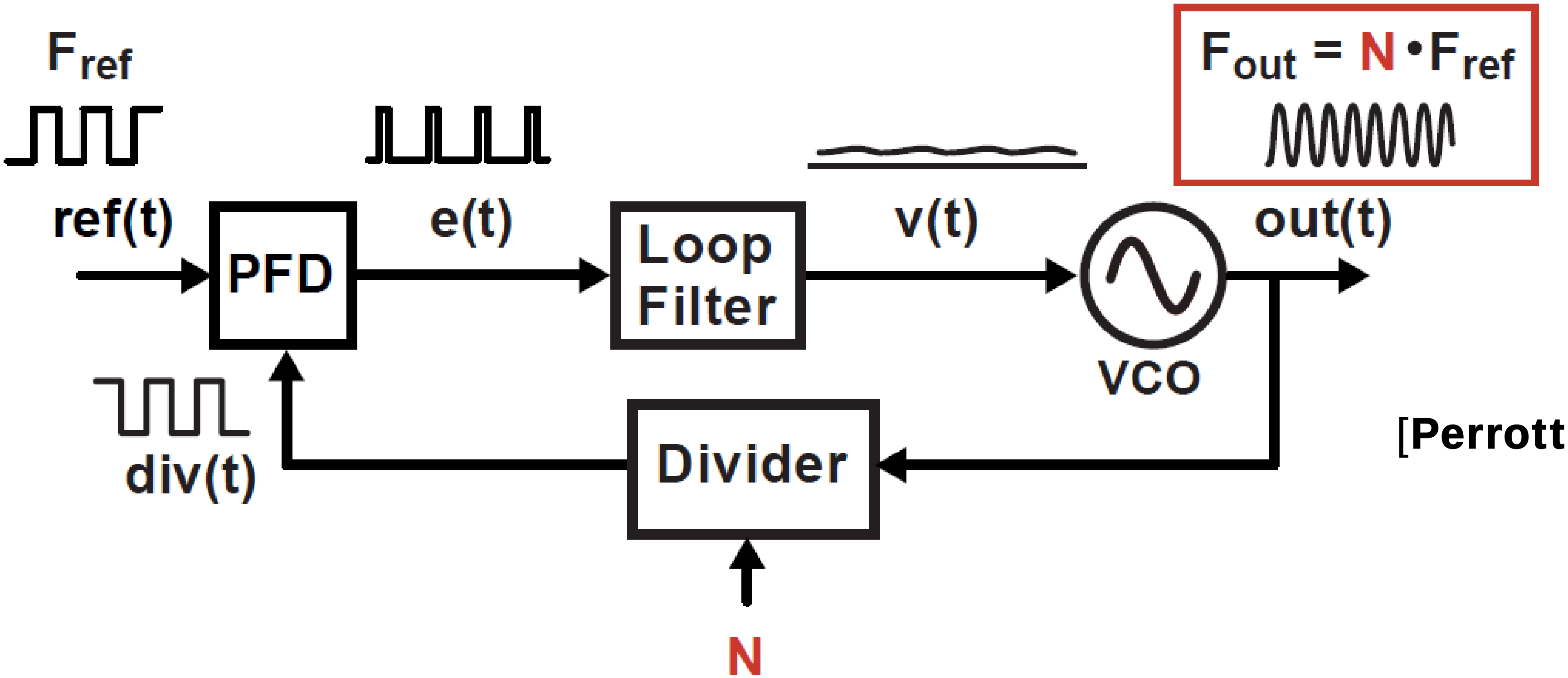
References

- M. Perrott, *High Speed Communication Circuits and Systems Course*, MIT Open Courseware

- Chapter 2 of *Phase-Locked Loops, 3rd Ed.,* R. Best, McGraw-Hill, 1997.

- Chapter 2, 3, 5, & 12 of *Phaselock Techniques,* F. Gardner, John Wiley & Sons, 2005.

PLL Block Diagram

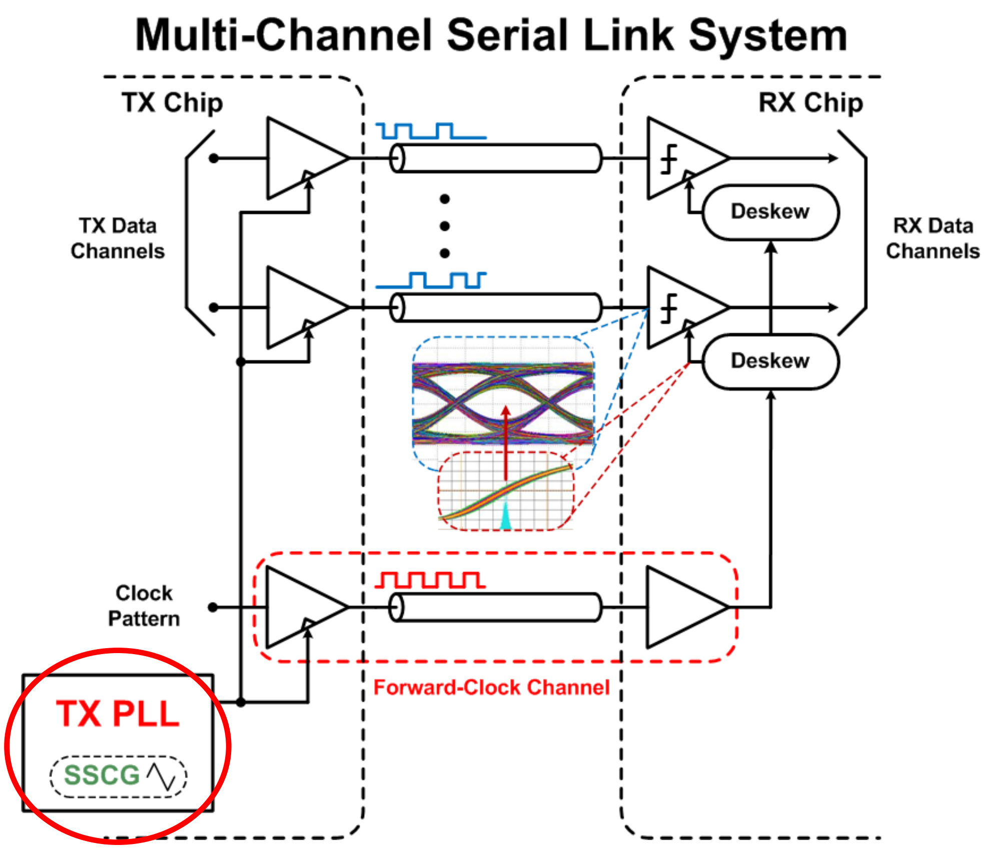


- A phase-locked loop (PLL) is a negative feedback system where an oscillator-generated signal is phase AND frequency locked to a reference signal

PLL Applications

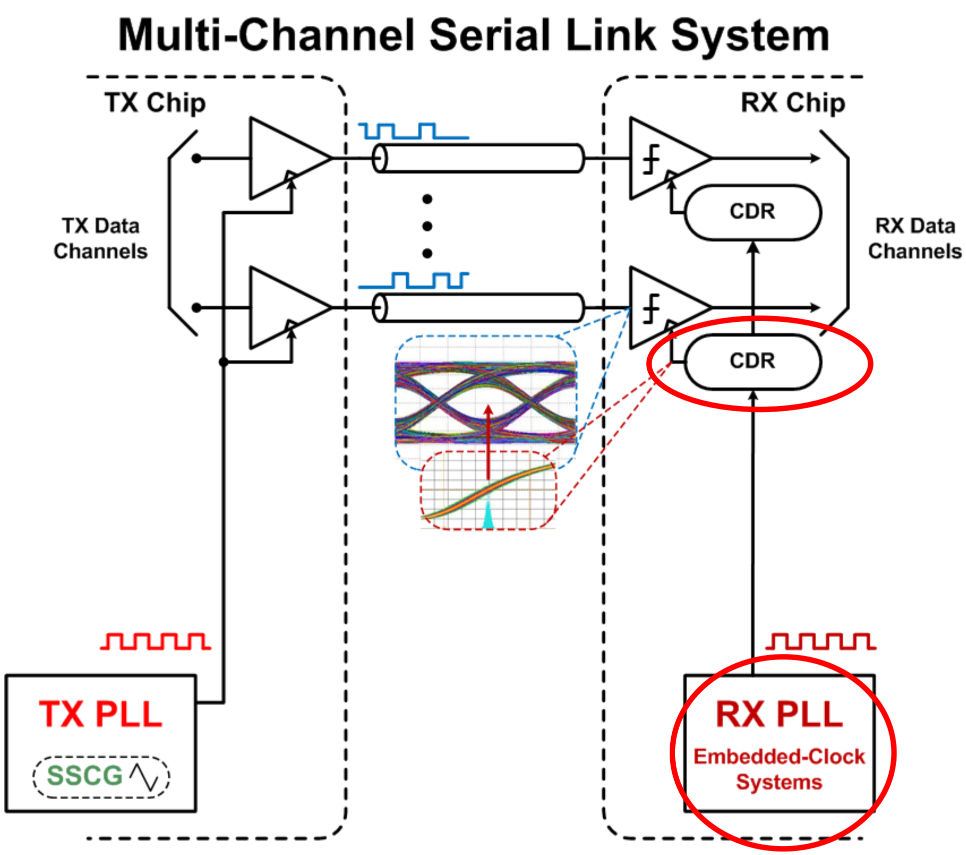
- PLLs applications
  - Frequency synthesis
    - Multiplying a 100MHz reference clock to 10GHz
  - Skew cancellation
    - Phase aligning an internal clock to an I/O clock
  - Clock recovery
    - Extract from incoming data stream the clock frequency and optimum phase of high-speed sampling clocks
  - Modulation/De-modulation
    - Wireless systems
    - Spread-spectrum clocking

Forward Clock I/O Circuits



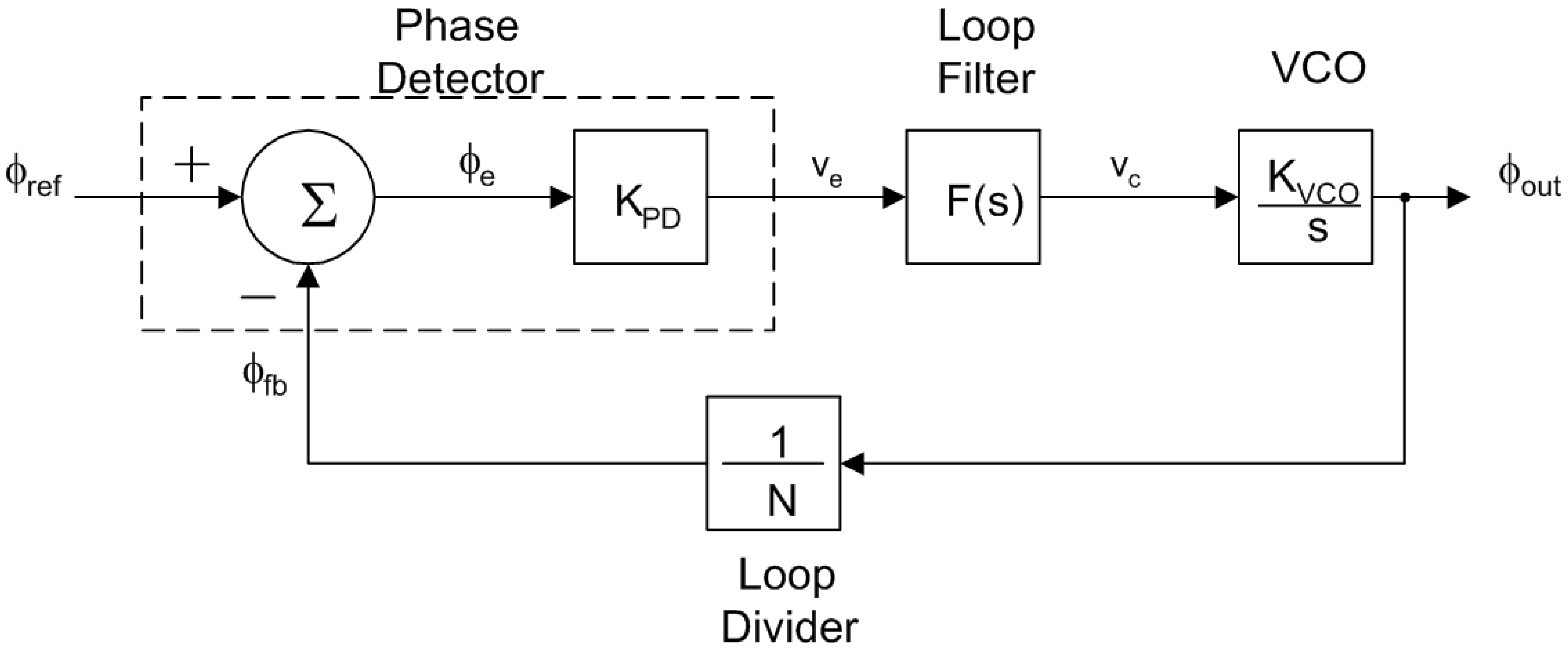
- TX PLL
- TX Clock Distribution
- Replica TX Clock Driver
- Channel
- Forward Clock Amplifier
- RX Clock Distribution
- De-Skew Circuit
  - DLL/PI
  - Injection-Locked Oscillator

Embedded Clock I/O Circuits



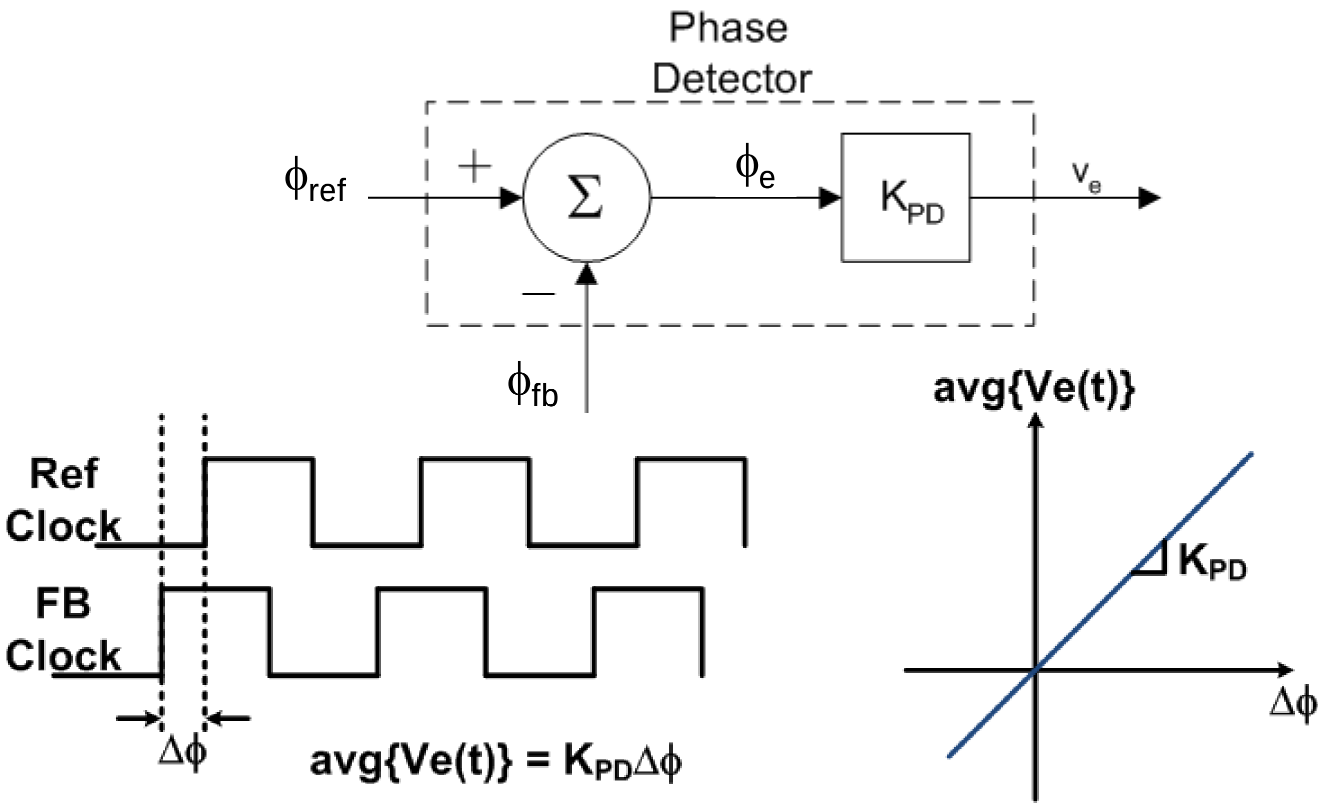
- TX PLL
- TX Clock Distribution
- CDR
  - Per-channel PLL-based
  - Dual-loop w/ Global PLL &
    - Local DLL/PI
    - Local Phase-Rotator PLLs
    - Global PLL requires RX clock distribution to individual channels

Linear PLL Model



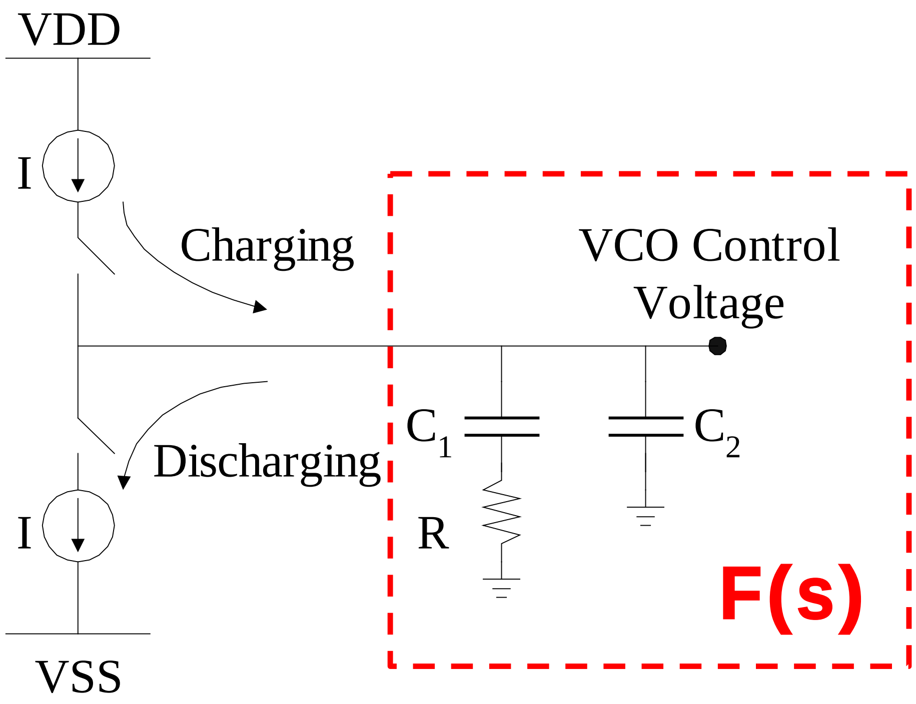
- Phase is generally the key variable of interest
- Linear "small-signal" analysis is useful for understand PLL dynamics if
  - PLL is locked (or near lock)
  - Input phase deviation amplitude is small enough to maintain operation in lock range

Phase Detector



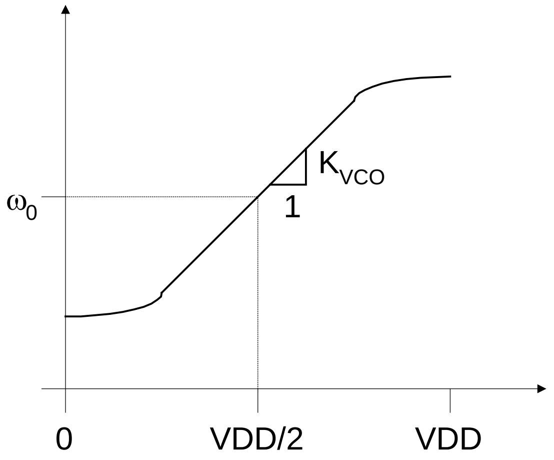
- Detects phase difference between feedback clock and reference clock
- The loop filter will filter the phase detector output, thus to characterize phase detector gain, extract average output voltage (or current for charge-pump PLLs)

Loop Filter



- Lowpass filter extracts average of phase detector error pulses

Voltage-Controlled Oscillator

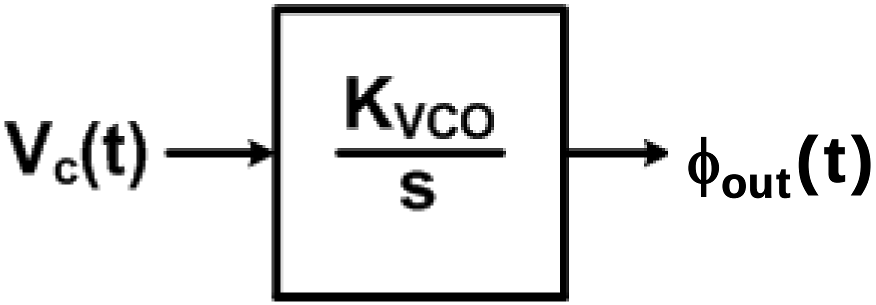


$$\omega_{out}(t) = \omega_0 + \Delta\omega_{out}(t) = \omega_0 + K_{VCO} v_c(t)$$

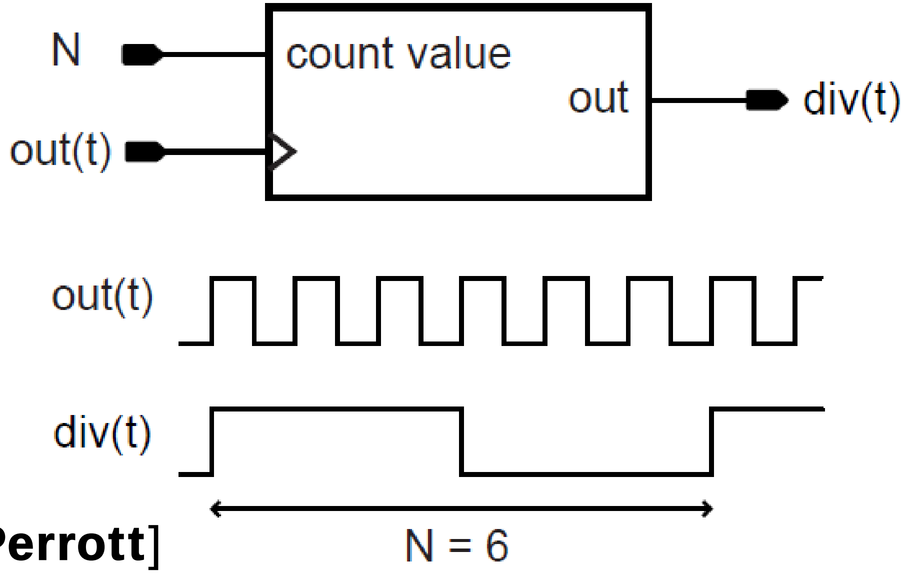
- Time-domain phase relationship

$$\phi_{out}(t) = \int \Delta\omega_{out}(t)\mathrm{dt} = K_{VCO}\int v_c(t)\mathrm{dt}$$

Laplace Domain Model



Loop Divider



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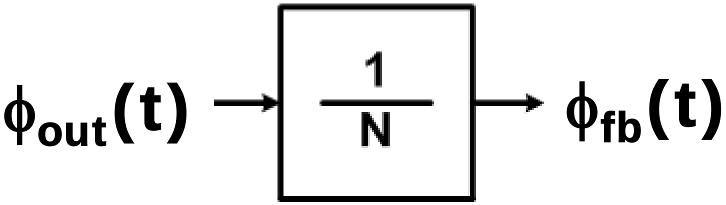


- Time-domain model

$$\omega_{fb}(t) = \frac{1}{N}\omega_{out}(t)$$

$$\phi_{fb}(t) = \int \frac{1}{N}\omega_{out}(t)\mathrm{dt} = \frac{1}{N}\phi_{out}(t)$$

Phase & Frequency Relationships

Angular Frequency is the first derivative (rate of change vs time) of phase

$$\frac{d\phi(t)}{dt} = \omega(t)$$

$$\phi(t) = \int_{o}^{t} \omega(\tau) d\tau$$

Consider a sinusoid $u_1(t)$ with angular frequency $\omega_1(t)$ and phase $\phi_1(t)$

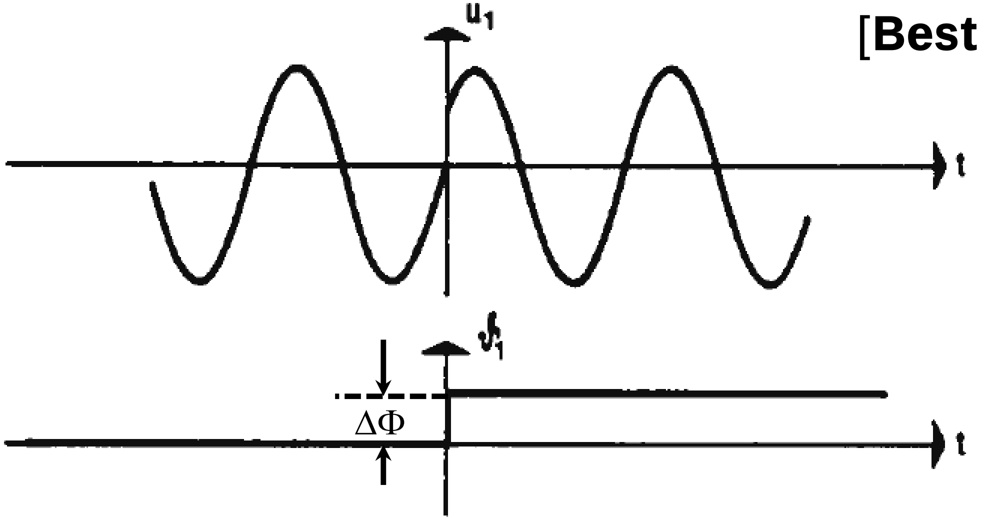
$$u_1(t) = \sin(\omega_1(t)t + \phi_1(t))$$

- Phase Step

$$\phi_1(t) = \Delta\Phi u(t)$$

$$u_1(t) = \sin(\omega_1(t) + \Delta\Phi u(t))$$

No change in frequency



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Phase & Frequency Relationships

- Frequency Step

$$\omega_1(t) = \omega_0 + \Delta\omega$$

$$u_1(t) = \sin(\omega_0 t + \Delta\omega t) = \sin(\omega_0 t + \phi_1(t))$$

$$\text{where } \phi_1(t) = \Delta\omega t$$

A frequency step produces a ramp in phase

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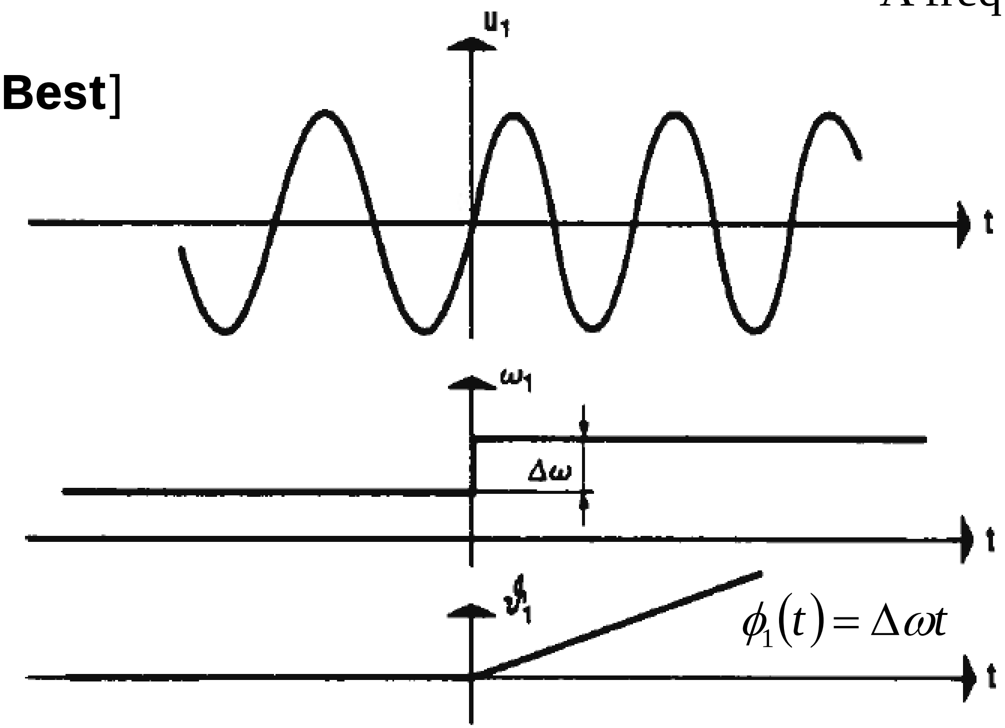

Phase & Frequency Relationships

- Frequency Ramp

$$\omega_1(t) = \omega_0 + \Delta\dot{\omega}t$$

$$u_1(t) = \sin\left(\int_0^t \left(\omega_0 + \Delta\dot{\omega}\tau\right)d\tau\right) = \sin\left(\omega_0 t + \frac{\Delta\dot{\omega}}{2}t^2\right) = \sin\left(\omega_0 t + \phi_1(t)\right)$$

$$\text{where } \phi_1(t) = \frac{\Delta\dot{\omega}}{2}t^2$$

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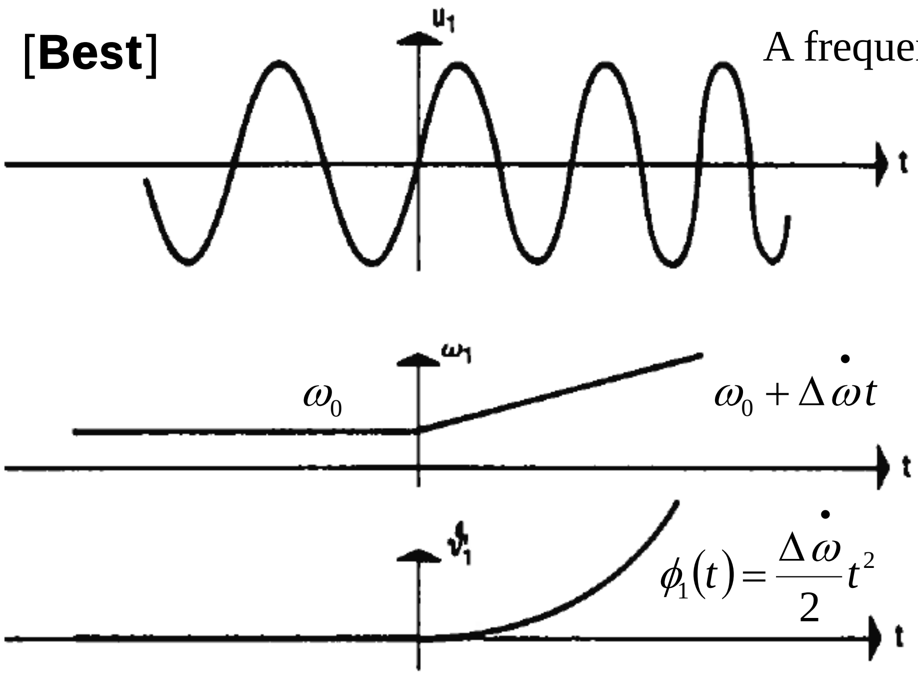
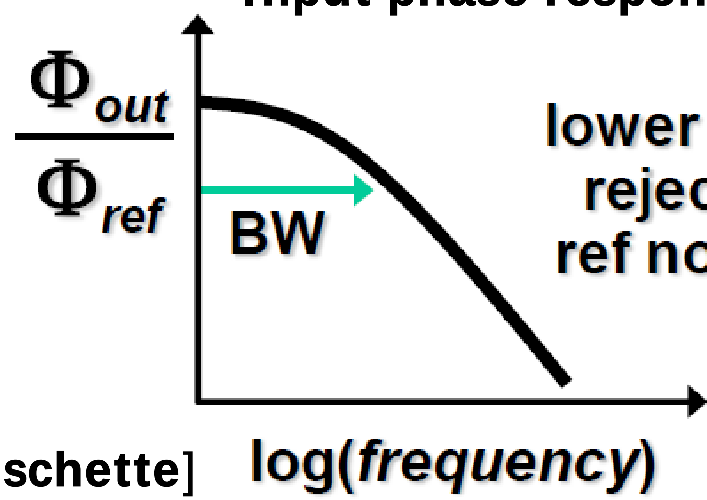


A frequency ramp produces a quadratic change in phase

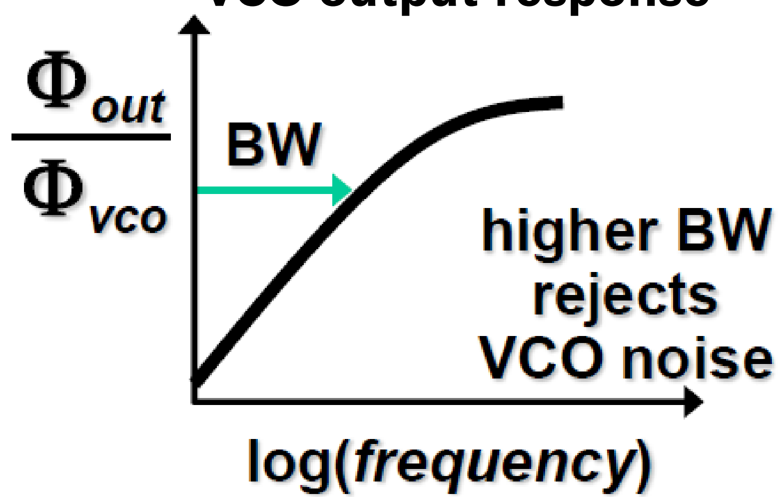
Understanding PLL Frequency Response

- Linear "small-signal" analysis is useful for understand PLL dynamics if
  - PLL is locked (or near lock)
  - Input phase deviation amplitude is small enough to maintain operation in lock range
- Frequency domain analysis can tell us how well the PLL tracks the input phase as it changes at a certain frequency
- PLL transfer function is different depending on which point in the loop the output is responding to

Input phase response



VCO output response



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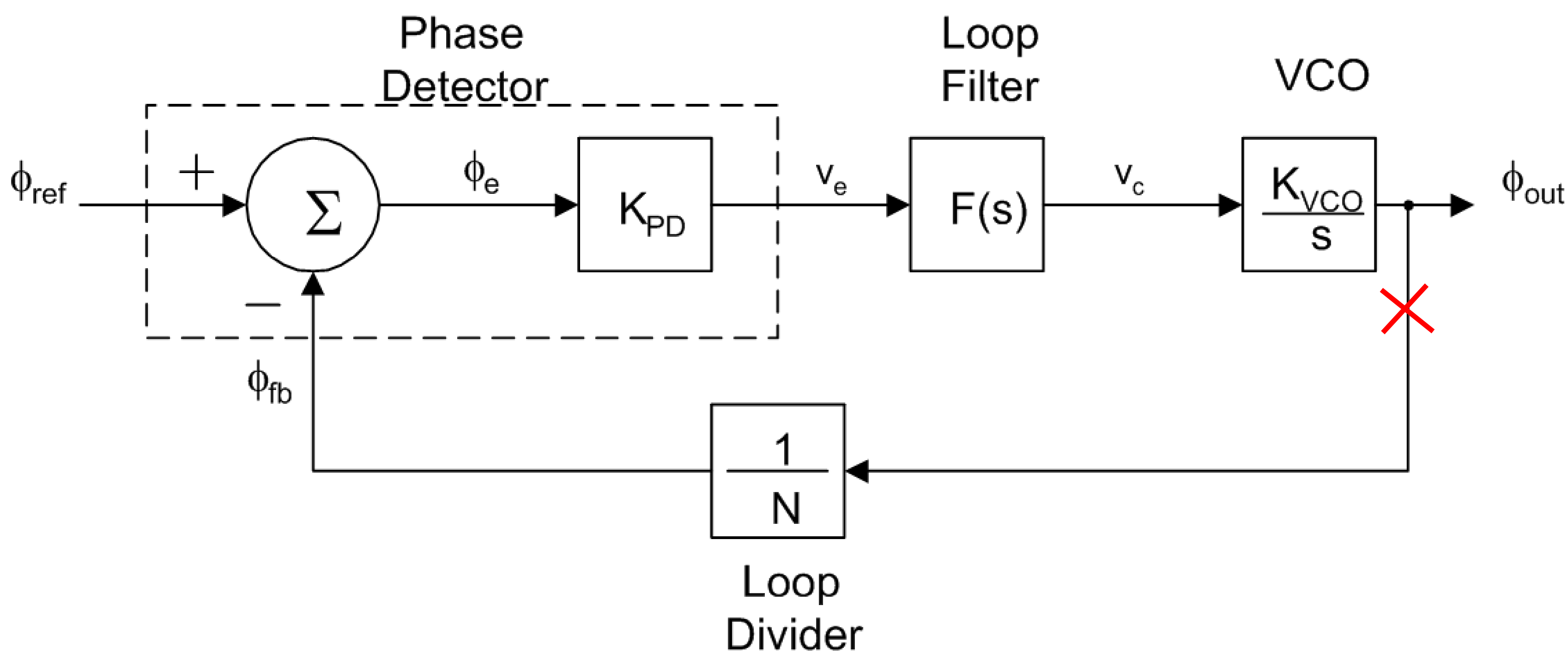
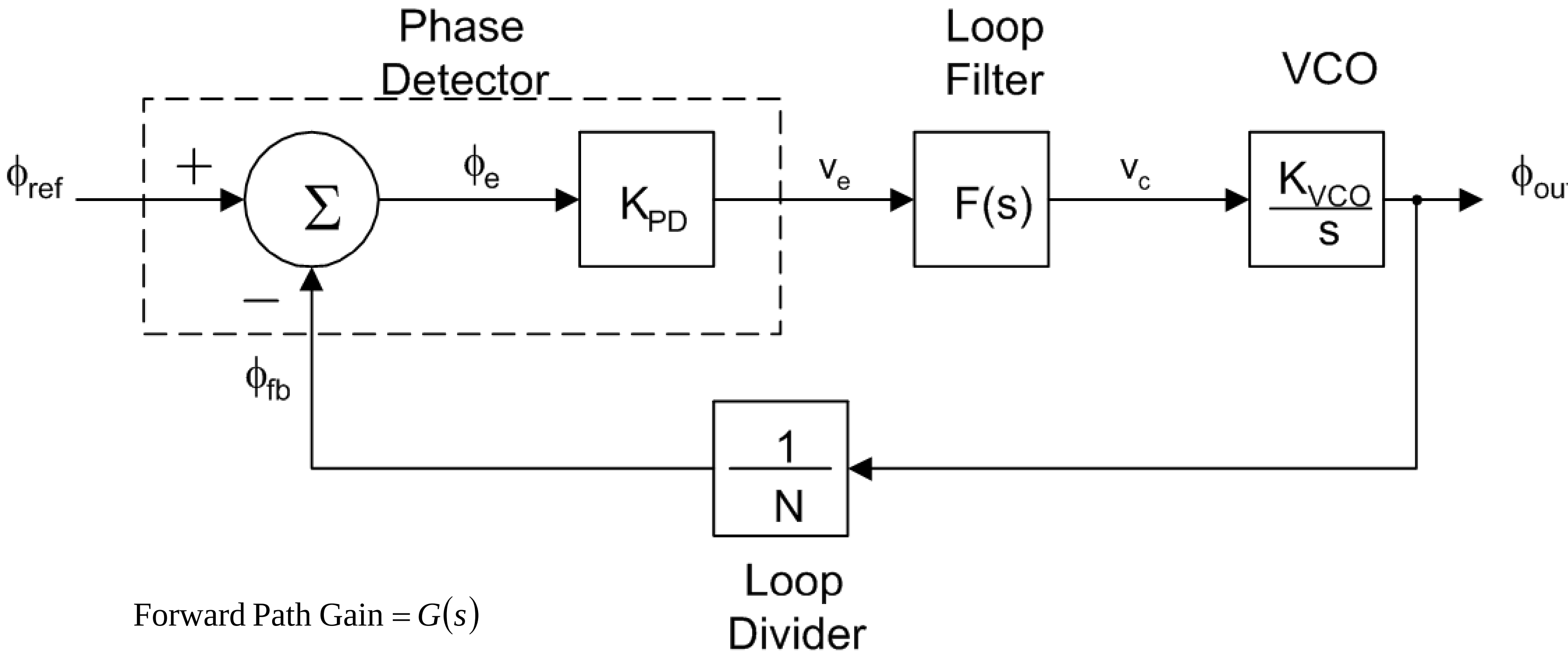
Open-Loop PLL Transfer Function



$$G(s)=\frac{\Phi_{out}(s)}{\Phi_e(s)}=\frac{K_{PD}K_{VCO}F(s)}{s}$$

- Open-loop response generally decreases with frequency

Closed-Loop PLL Transfer Function



$$\text{Forward Path Gain} = G(s)$$

Loop Gain

$$l_1 = -\frac{K_{PD}K_{VCO}F(s)}{sN} = -\frac{G(s)}{N}$$

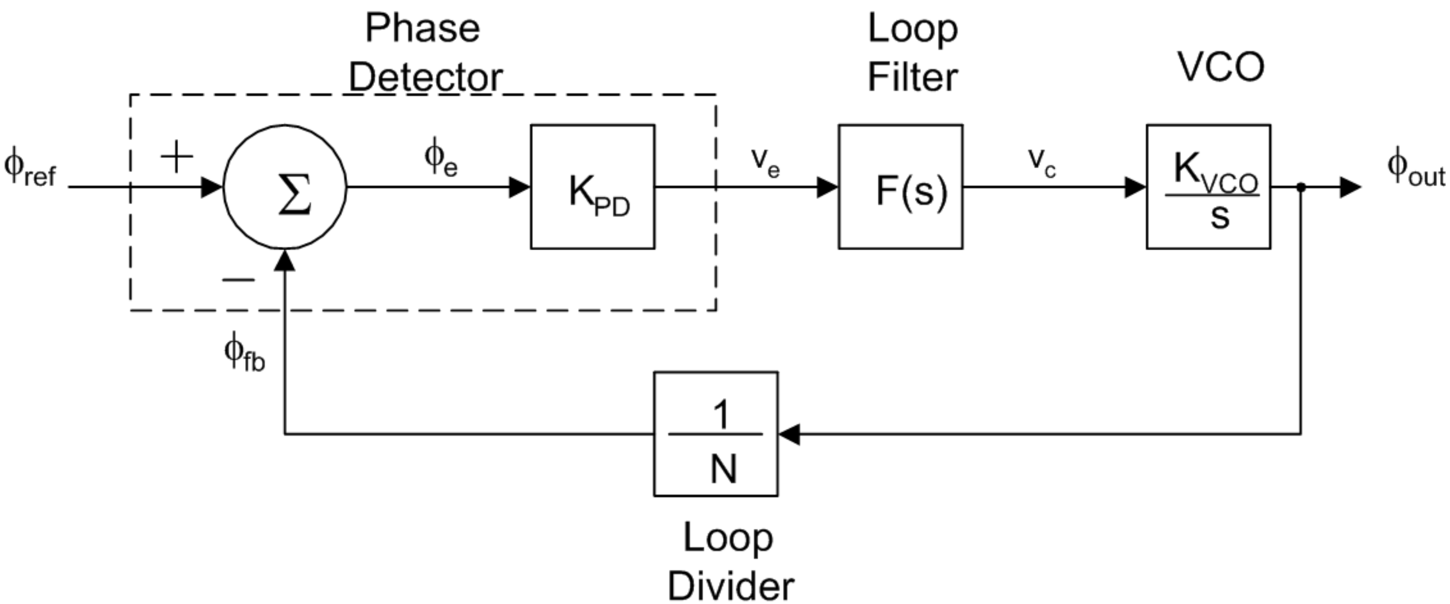
$$\text{Forward Path Determinant} \quad \Delta_1 = 1 - 0 = 1$$

$$\text{System Determinant} \quad \Delta = 1 - \left(-\frac{G(s)}{N}\right) + 0 = 1 + \frac{G(s)}{N}$$

$$H(s) = \frac{\Phi_{out}(s)}{\Phi_{ref}(s)} = \frac{G(s)}{1 + \frac{G(s)}{N}} = \frac{K_{PD}K_{VCO}F(s)}{s + \frac{K_{PD}K_{VCO}F(s)}{N}}$$

- Low-pass response whose overall order is set by F(s)

PLL Error Transfer Function



$$\text{Forward Path Gain} = 1$$

$$\text{Loop Gain}$$

$$l_1 = -\frac{K_{PD} K_{VCO} F(s)}{sN} = -\frac{G(s)}{N}$$

$$\text{Forward Path Determinant} \quad \Delta_1 = 1 - 0 = 1$$

$$\text{System Determinant} \quad \Delta = 1 - \left(-\frac{G(s)}{N}\right) + 0 = 1 + \frac{G(s)}{N}$$

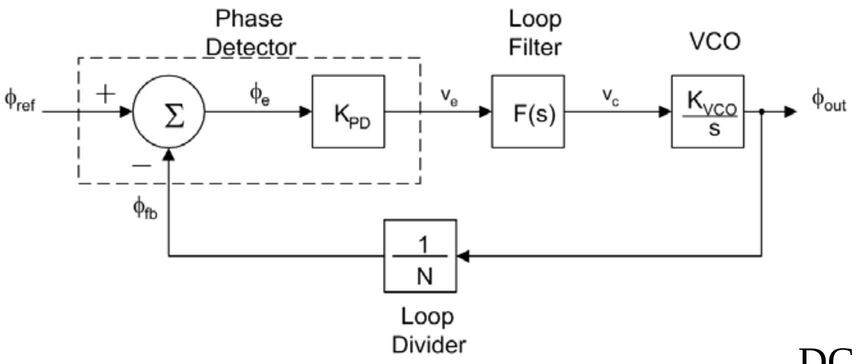
$$E(s) = \frac{\Phi_e(s)}{\Phi_{ref}(s)} = \frac{1}{1 + \frac{G(s)}{N}} = \frac{s}{s + \frac{K_{PD} K_{VCO} F(s)}{N}}$$

- Ideally, we want this to be zero
- Phase error generally increases with frequency due to this high-pass response

PLL Order and Type

- The PLL order refers to the number of poles in the closed-loop transfer function
  - This is typically one greater than the number of loop filter poles
- The PLL type refers to the number of integrators within the loop
  - A PLL is always at lease Type 1 due to the VCO integrator
- Note, the order can never be less than the type

First-Order PLL



- Simple first-order low-pass transfer function

- Closed-loop bandwidth is equal to the DC loop gain magnitude

$$F(s) = K_1$$

$$\text{Forward Path Gain}: G(s) = \frac{K_{PD}K_{VCO}K_1}{s} = \frac{NK_{DC}}{s}$$

$$\text{DC Loop Gain Magnitude}: K_{DC} = \lim_{s\to 0}\left(\frac{sG(s)}{N}\right) = \frac{K_{PD}K_{VCO}K_1}{N}$$

$$\text{Transfer Function}: H(s) = \frac{K_{PD}K_{VCO}K_1}{s + \frac{K_{PD}K_{VCO}K_1}{N}} = \frac{N\omega_{3dB}}{s+\omega_{3dB}} = \frac{NK_{DC}}{s+K_{DC}}$$

$$\text{Closed-Loop Bandwidth}: \omega_{3dB} = \frac{K_{PD}K_{VCO}K_1}{N} = K_{DC}$$

$$\text{Error Function}: E(s) = \frac{s}{s + \frac{K_{PD}K_{VCO}K_1}{N}} = \frac{s}{s+\omega_{3dB}} = \frac{s}{s+K_{DC}}$$

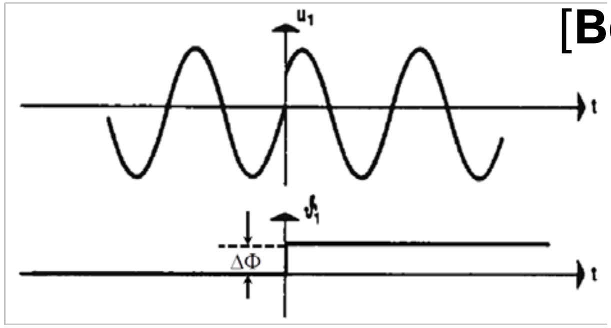
First-Order PLL Tracking Response

- The PLL's tracking behavior, or how the phase error responds to an input phase change, varies with the PLL type
- Phase Step Response

$$\phi_1(t) = \Delta\Phi u(t)$$

$$u_1(t) = \sin(\omega_1(t) + \Delta\Phi u(t))$$

No change in frequency



- The final value theorem can be used to find the steady-state phase error

$$\lim_{s\to 0}\left(\frac{\Delta\Phi}{s}\right)(sE(s)) = \lim_{s\to 0}\frac{\Delta\Phi s}{s+K_{DC}} = 0$$

- All PLLs should have no steady-state phase error with a phase step error
  - Note, this assumes that the frequency of operation is the same as the VCO center frequency (V_{ctrl}=0). Working at a frequency other than the VCO center frequency is considered having a frequency offset (step).

First-Order PLL Tracking Response

- Frequency Offset (Step)

$$\omega_1(t) = \omega_0 + \Delta\omega$$

$$u_1(t) = \sin(\omega_0 t + \Delta\omega t) = \sin(\omega_0 t + \phi_1(t))$$

$$\text{where } \phi_1(t) = \Delta\omega t$$

A frequency step produces a ramp in phase

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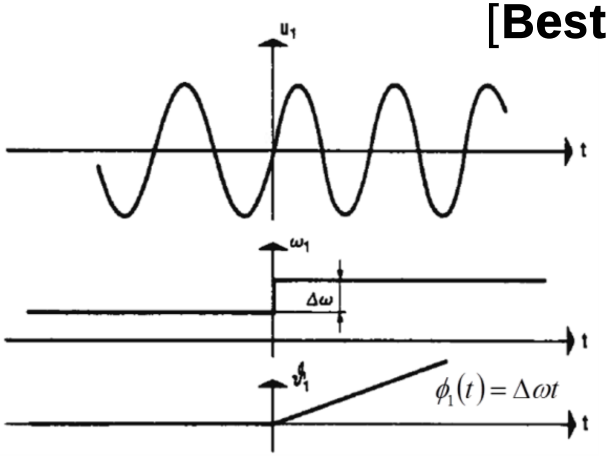


- The final value theorem can be used to find the steady-state phase error

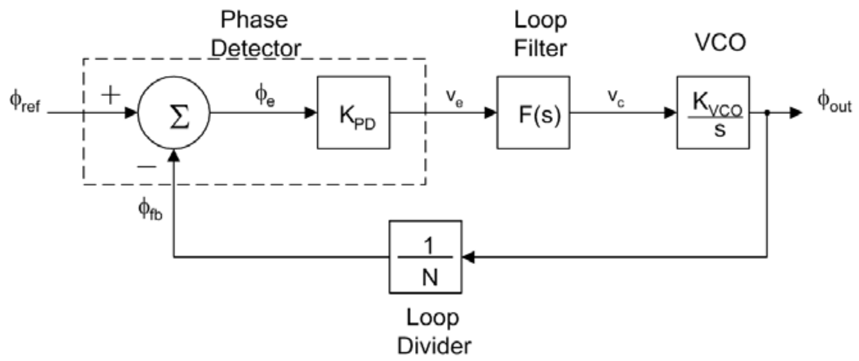
$$\lim_{s\to 0}\left(\frac{\Delta\omega}{s^2}\right)(sE(s)) = \lim_{s\to 0}\frac{\Delta\omega}{s+K_{DC}} = \frac{\Delta\omega}{K_{DC}}$$

- With a frequency offset (step), a first-order PLL will lock with a steady-state phase error that is inversely proportional to the loop gain

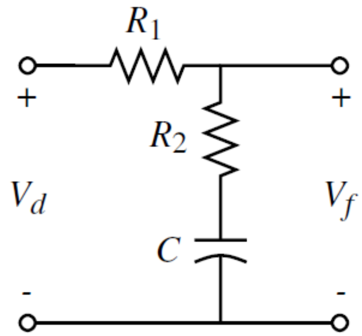
First-Order PLL Issues

- The DC loop gain directly sets the PLL bandwidth
  - No degrees of freedom
- In order to have low phase error, a large loop gain is necessary, which implies a wide bandwidth
  - This may not be desired in applications where we would like to filter input reference clock phase noise
- First-order PLLs offer no filtering of the phase detector output
  - Without this filtering, the PD may not be well approximated by a simple K_{PD} factor
    - Multiplier PDs have a “second-harmonic” term
    - Digital PDs output square pulses that need to be filtered

Second-Order Type-1 PLL w/ Passive Lag-Lead Filter



Passive Lag-Lead Loop Filter



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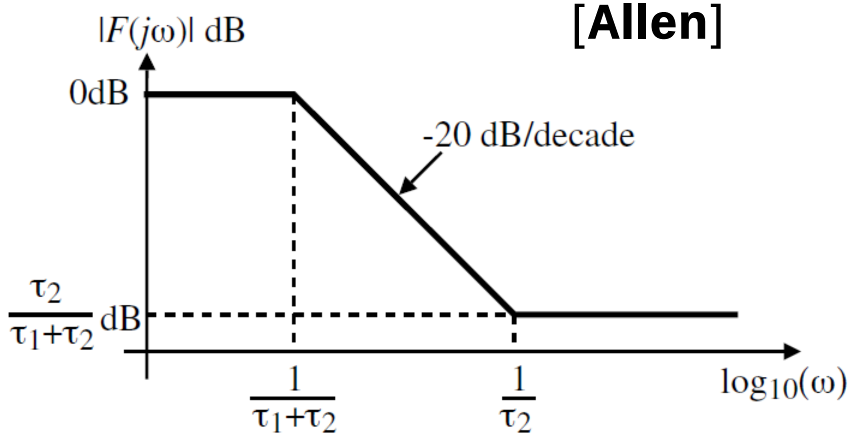


$$F(s) = \frac{1 + s\tau_2}{1 + s(\tau_1 + \tau_2)}$$

$$\tau_1 = R_1 C \qquad \tau_2 = R_2 C$$

Second-Order Type-1 PLL w/ Passive Lag-Lead Filter

$$F(s)=\frac{1+s\tau_2}{1+s(\tau_1+\tau_2)}$$

$$\tau_1 = R_1C \qquad \tau_2 = R_2C$$

$$\text{Forward Path Gain}: G(s)=\frac{K_{PD}K_{VCO}(1+s\tau_2)}{s(1+s(\tau_1+\tau_2))}=\frac{NK_{DC}\left(\frac{\tau_2}{\tau_1+\tau_2}\right)\left(s+\frac{1}{\tau_2}\right)}{s\left(s+\frac{1}{\tau_1+\tau_2}\right)}$$

$$\text{DC Loop Gain Magnitude}: K_{DC}=\lim_{s\to 0}\left(\frac{sG(s)}{N}\right)=\frac{K_{PD}K_{VCO}}{N}$$

$$\text{Transfer Function}: H(s)=\frac{\frac{K_{PD}K_{VCO}\tau_2}{\tau_1+\tau_2}\left(s+\frac{1}{\tau_2}\right)}{s^2+\left(\frac{1+K_{PD}K_{VCO}\tau_2/N}{\tau_1+\tau_2}\right)s+\frac{K_{PD}K_{VCO}}{N(\tau_1+\tau_2)}}=N\frac{\omega_n\left(2\zeta-\frac{N\omega_n}{K_{PD}K_{VCO}}\right)s+\omega_n^2}{s^2+2\zeta\omega_n s+\omega_n^2}$$

$$=N\frac{K_{DC}\left(\frac{\tau_2}{\tau_1+\tau_2}\right)\left(s+\frac{1}{\tau_2}\right)}{s^2+\left(\frac{1+K_{DC}\tau_2}{\tau_1+\tau_2}\right)s+\frac{K_{DC}}{\tau_1+\tau_2}}$$

$$\text{Natural Frequency}: \omega_n=\sqrt{\frac{K_{PD}K_{VCO}}{N(\tau_1+\tau_2)}}$$

$$\text{Damping Factor}: \zeta=\frac{\omega_n}{2}\left(\tau_2+\frac{N}{K_{PD}K_{VCO}}\right)$$

$$\text{Error Function}: E(s)=\frac{s\left(s+\frac{N\omega_n^2}{K_{PD}K_{VCO}}\right)}{s^2+2\zeta\omega_n s+\omega_n^2}$$

Second-Order Type-1 PLL Tracking Response

- Phase Step Response

$$\lim_{s\to 0}\left(\frac{\Delta\Phi}{s}\right)(sE(s)) = \lim_{s\to 0}\frac{\Delta\Phi s\left(s+\dfrac{N\omega_n^2}{K_{PD}K_{VCO}}\right)}{s^2+2\zeta\omega_n s+\omega_n^2} = 0$$

Again, phase error should be zero with a phase step

- Frequency Offset (Step)

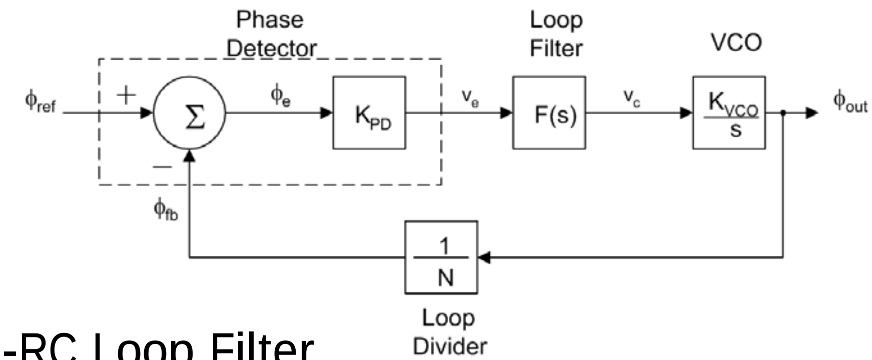
$$\lim_{s\to 0}\left(\frac{\Delta\omega}{s^2}\right)(sE(s)) = \lim_{s\to 0}\frac{\Delta\omega\left(s+\dfrac{N\omega_n^2}{K_{PD}K_{VCO}}\right)}{s^2+2\zeta\omega_n s+\omega_n^2} = \frac{\Delta\omega}{K_{DC}}$$

- A second-order type-1 PLL will still lock with a phase error if there is a frequency offset!

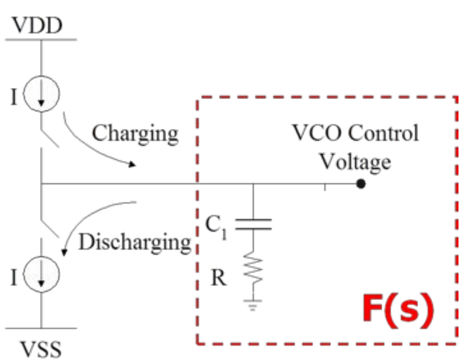
Second-Order Type-1 PLL Properties

- While the second-order type-1 PLL will still lock with a phase error with a frequency offset, it is much more useful than a first-order PLL
- There are sufficient design parameters (degrees of freedom) to independently set ω_n, ζ, and K_{DC}
- The loop filter conditions the phase detector output for proper VCO control
- Loop stability needs to be considered for the second-order system

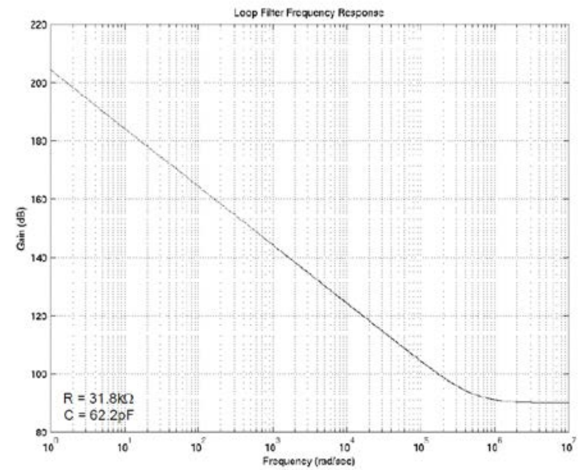
Second-Order Type-2 PLL w/ Passive Series-RC Lag-Lead Filter



Passive Series-RC Loop Filter



$$F(s) = \frac{R\left(s + \frac{1}{RC}\right)}{s}$$



- Note, this type of loop filter is typically used with a charge-pump driving it. Thus, the filter transfer function is equal to the impedance.

Second-Order Type-2 PLL w/ Passive Series-RC Lag-Lead Filter

$$F(s)=\frac{R\left(s+\frac{1}{RC}\right)}{s}$$

DC Loop Gain Magnitude : $K_{DC}=\infty$ (ideally)

Forward Path Gain : $G(s)=\frac{K_{PD}K_{VCO}R\left(s+\frac{1}{RC}\right)}{s^2}$

Transfer Function : $H(s)=\frac{K_{PD}K_{VCO}R\left(s+\frac{1}{RC}\right)}{s^2+\left(\frac{K_{PD}K_{VCO}R}{N}\right)s+\frac{K_{PD}K_{VCO}}{NC}}=\frac{N2\zeta\omega_n\left(s+\frac{\omega_n}{2\zeta}\right)}{s^2+2\zeta\omega_n s+\omega_n^2}$

Natural Frequency : $\omega_n=\sqrt{\frac{K_{PD}K_{VCO}}{NC}}$

Damping Factor : $\zeta=\frac{\omega_n}{2}RC$

Error Function : $E(s)=\frac{s^2}{s^2+2\zeta\omega_n s+\omega_n^2}$

Second-Order Type-2 PLL Tracking Response

- Phase Step Response

$$\lim_{s\to 0}\left(\frac{\Delta\Phi}{s}\right)\left(sE(s)\right)=\lim_{s\to 0}\frac{\Delta\Phi s^2}{s^2+2\zeta\omega_n s+\omega_n^2}=0$$

Again, phase error should be zero with a phase step

- Frequency Offset (Step)

$$\lim_{s\to 0}\left(\frac{\Delta\omega}{s^2}\right)\left(sE(s)\right)=\lim_{s\to 0}\frac{\Delta\omega s}{s^2+2\zeta\omega_n s+\omega_n^2}=0$$

- A second-order type-2 PLL will lock with no phase error with a frequency offset!

Second-Order Type-2 PLL Properties

- A big advantage of the type-2 PLL is that it has zero phase error even with a frequency offset
  - This is why type-2 PLLs are very popular
- A type-2 PLL requires a zero in the loop filter for stability.
  - Note, this is not required in a type-1 PLL
- This zero can cause extra peaking in the frequency response
  - Important to minimize this in some applications, such as cascaded CDR systems

Next Time

- PLL System Analysis
  - PLL Stability
  - Noise Transfer Functions
  - Transient Response