ECEN620: Network Theory
Broadband Circuit Design
Fall 2023

Lecture 1: Introduction

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Texas A&M University
Why Broadband Circuits?

- Broadband circuits are used in many wireline and wireless communication systems.
- Trends in processor design and the growing demand for digital connectivity are pushing data rates and bandwidth requirements in these systems.
- In this class, we will study key clocking and amplifier circuits that enable these communication systems to scale in performance.
Class Topics

• Broadband circuit design methodologies

• Clocking circuits
  • Phase-Locked Loops (PLLs)
  • Clock-and-Data Recovery systems (CDRs)

• Broadband amplifiers
  • Transimpedance, limiting, and variable-gain amplifiers
Analog Circuit Sequence

- Electronics I 325
- Electronics II 326
- Pre/Co-Requisite

- Operational Amplifiers 457
- VLSI Circuit Design 474/704

- Advanced-Analog Circuit Design 607
- Active Filter Analysis and Design 458

- Solid-State Devices 671
- Integrated CMOS RF Circuits and Systems 665

- Data Converters 610
- Active Network Synthesis 622

- Optical Interconnects Circuits & Systems 689
- MM-Wave Integrated Circuits 625

- High Frequency GaAs/SiGe Analog IC Design 650
- High-Speed Links Circuits & Systems 720
Administrative

• Instructor
  • Sam Palermo
  • 315E WERC Bldg., 979-845-4114, spalermo@tamu.edu
  • Office hours: MW 1:30PM-3:00PM
    • In-person and online via Zoom

• Lectures
  • TR 2:20PM-3:35PM
  • Videos posted on Canvas

• Class web pages
  • https://people.engr.tamu.edu/spalermo/ecen620.html
  • Will use Canvas for turning in assignments
Class Material

• Textbook: Class Notes and Technical Papers

• Key References

• Class notes will be posted online
Grading

- Exams (50%)
  - Two midterm exams (25% each)

- Homework (25%)
  - Collaboration is allowed, but independent simulations and write-ups
  - Need to setup CADENCE simulation environment
  - Turn in via Canvas
  - No late homework will be graded

- Final Project (25%)
  - Groups of 1-3 students
  - Report and PowerPoint presentation required
  - Turn in report and presentation files via Canvas
Prerequisites

• Circuits
  • ECEN474/704 or approval of instructor
  • Basic knowledge of CMOS gates, flops, etc...
  • Circuit simulation experience (HSPICE, Spectre)

• Systems
  • Basic knowledge of s- and z-transforms
  • MATLAB experience
Simulation Tools

• Matlab

• Cadence

• 90nm CMOS device models
  • Can use other technology models if they are a 90nm or more advanced CMOS node

• Other tools, schematic, layout, etc... are optional
Preliminary Schedule

<table>
<thead>
<tr>
<th>Topic</th>
<th>Week</th>
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<tbody>
<tr>
<td>I. Introduction and Linear Systems</td>
<td></td>
</tr>
<tr>
<td>II. PLL System Analysis</td>
<td>Week 1-8</td>
</tr>
<tr>
<td>III. PLL Building Blocks</td>
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<tr>
<td>1st Exam</td>
<td>Oct 12</td>
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<tr>
<td>IV. CDRs</td>
<td></td>
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<tr>
<td>V. Broadband Amplifiers</td>
<td>Week 9-14</td>
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<tr>
<td>VI. Other Topics</td>
<td></td>
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<tr>
<td>2nd Exam</td>
<td>Nov. 30</td>
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<tr>
<td>Project Report Due</td>
<td>Dec. 4</td>
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<tr>
<td>Project Presentation</td>
<td>Dec. 12 (1:00PM – 3:00PM)</td>
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</tbody>
</table>

- Dates may change with reasonable notice
High-Speed Electrical Link System
**10GHz PLL Example**

<table>
<thead>
<tr>
<th>PLL Performance</th>
<th>TxPLL</th>
<th>RxPLL</th>
</tr>
</thead>
<tbody>
<tr>
<td>Min freq (GHz)</td>
<td>8.98</td>
<td>8.96</td>
</tr>
<tr>
<td>Max freq (GHz)</td>
<td>13.54</td>
<td>13.47</td>
</tr>
<tr>
<td>Mean freq (GHz)</td>
<td>11.26</td>
<td>11.22</td>
</tr>
<tr>
<td>Lock range (GHz)</td>
<td>4.56</td>
<td>4.52</td>
</tr>
<tr>
<td></td>
<td>+/-20.2%</td>
<td>+/-20.1%</td>
</tr>
<tr>
<td>Fine tune hold range</td>
<td>5.8%</td>
<td>5.8%</td>
</tr>
<tr>
<td>Quarter rate clock phase noise @ 10MHz offset (dBc/Hz)</td>
<td>-117.8</td>
<td>-117.7</td>
</tr>
<tr>
<td>Jitter, 1MHz-100MHz (ps rms)</td>
<td>1.5</td>
<td>1.4</td>
</tr>
<tr>
<td>Jitter, fc/1667-100MHz (ps rms)</td>
<td>0.64</td>
<td>0.64</td>
</tr>
</tbody>
</table>

100mW Power consumption (with clock distribution)

[Mejhelli (IBM) ISSCC 2006]
High-Speed Logic Example: Divide-by-2 with CML FF

- High-speed logic blocks are required in numerous high-speed circuits, such as PLLs, CDRs, and equalizers.
- Relative to CMOS logic, current-mode logic (CML) circuits can achieve higher bandwidth due to lower self-loading.
- Additional bandwidth extension can be achieved with the addition of passives (inductors) and feedback.

[Reference: Razavi]
Detailed Serial-Link Receiver Architecture

Key Features:
- Half-rate design
- 5-tap continuously adaptive DFE
- Variable gain amplifier
- Digital CDR
- ESD protection (HBM & CDM)
- 130mW (with DFE and CDR logic)

[Meghelli (IBM) ISSCC 2006]
Key Features:
- Fully digital loop
- Can handle up to +/- 4000ppm frequency offset
- Independent I,Q control

[Meghelli (IBM) ISSCC 2006]
Variable-Gain Amplifier (VGA) Example

Key Features:
• Dual Diff Amps
  • Half/Full Amplitude
• Switched R Degen
• 7 Bit Thermometer
  • Multi-bit Slewrate
• Glitchless Operation
• Continuous Adjustment
• Optimized with GA

[Sorna (IBM) ISSCC 2005]
Optical Receiver Front-End

- Transimpedance amplifiers (TIAs) convert an input current signal into an output voltage with a transimpedance gain.
- Limiting amplifier amplifies the TIA output to a reliable level to achieve a given BER with a certain decision element (comparator).
Next Time

- Linear circuit analysis review