ECEN620: Network Theory Broadband Circuit Design Fall 2023

Lecture 1: Introduction

Sam Palermo

Analog & Mixed-Signal Center

Texas A&M University

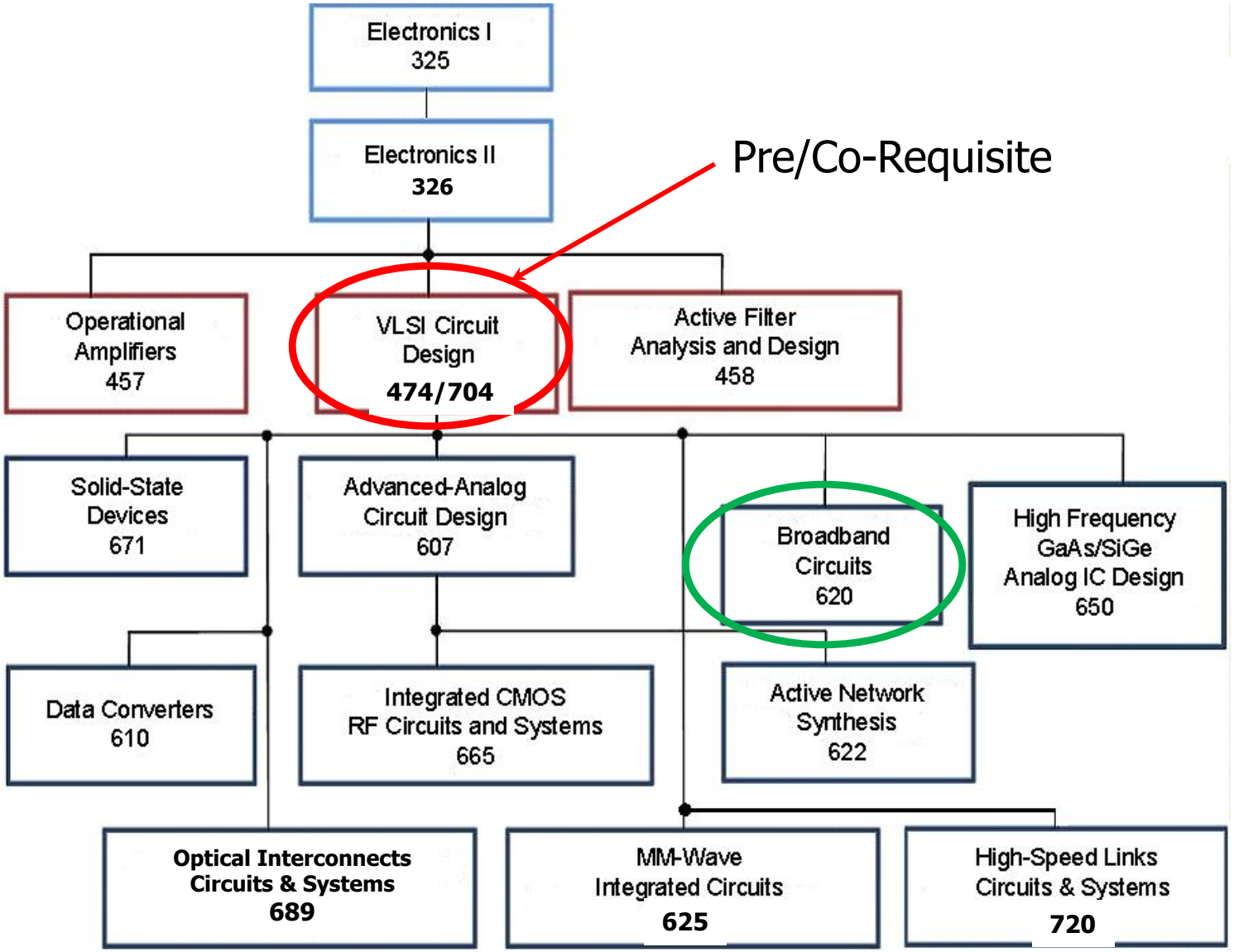
Why Broadband Circuits?

- Broadband circuits are used in many wireline and wireless communication systems
- Trends in processor design and the growing demand for digital connectivity are pushing data rates and bandwidth requirements in these systems
- In this class, we will study key clocking and amplifier circuits that enable these communication systems to scale in performance

Class Topics

- Broadband circuit design methodologies
- Clocking circuits
  - Phase-Locked Loops (PLLs)
  - Clock-and-Data Recovery systems (CDRs)
- Broadband amplifiers
  - Transimpedance, limiting, and variable-gain amplifers

Analog Circuit Sequence



Administrative

- Instructor
  - Sam Palermo
  - 315E WERC Bldg., 979-845-4114, spalermo@tamu.edu
  - Office hours: MW 1:30PM-3:00PM
    - In-person and online via Zoom
- Lectures
  - TR 2:20PM-3:35PM
  - Videos posted on Canvas
- Class web pages
  - https://people.engr.tamu.edu/spalermo/ecen620.html
  - Will use Canvas for turning in assignments

Class Material

- Textbook: Class Notes and Technical Papers
- Key References
  - *Phaselock Techniques,* F. Gardner, John Wiley & Sons, 2005.
  - *Design of Integrated Circuits for Optical Communications*, B. Razavi, McGraw-Hill, 2003.
  - *Phase-Locked Loops: Design, Simulation, & Applications*, R. Best, McGraw-Hill, 1997.
  - *Broadband Circuits for Optical Fiber Communication*, E. Sackinger, Wiley, 2005.
  - *Design of Analog CMOS Integrated Circuits*, B. Razavi, McGraw-Hill, 2001.
- Class notes will be posted online

Grading

- Exams (50%)
  - Two midterm exams (25% each)
- Homework (25%)
  - Collaboration is allowed, but independent simulations and write-ups
  - Need to setup CADENCE simulation environment
  - Turn in via Canvas
  - No late homework will be graded
- Final Project (25%)
  - Groups of 1-3 students
  - Report and PowerPoint presentation required
  - Turn in report and presentation files via Canvas

Prerequisites

- Circuits
  - ECEN474/704 or approval of instructor
  - Basic knowledge of CMOS gates, flops, etc…
  - Circuit simulation experience (HSPICE, Spectre)

- Systems
  - Basic knowledge of s- and z-transforms
  - MATLAB experience

Simulation Tools

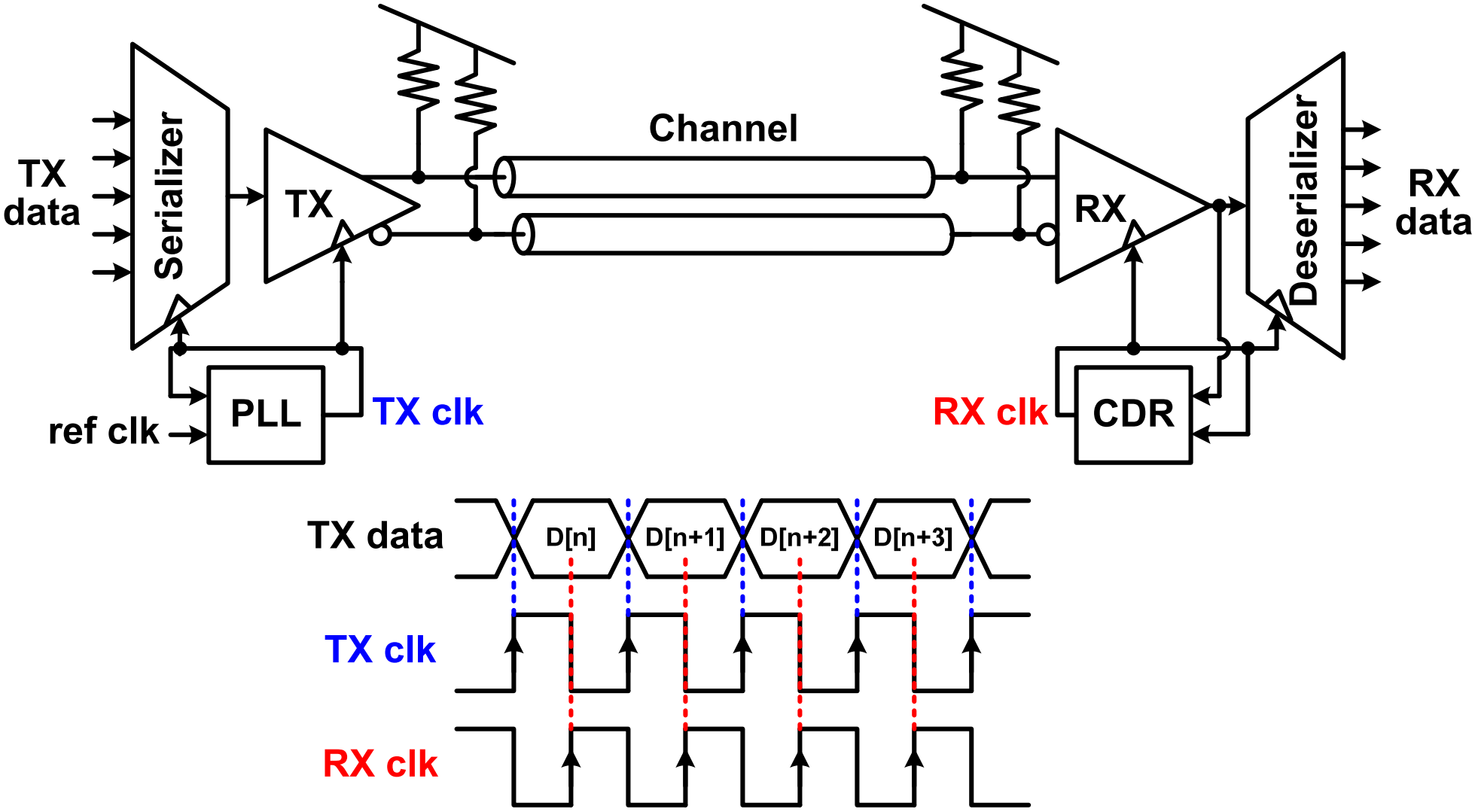
- Matlab
- Cadence
- 90nm CMOS device models
  - Can use other technology models if they are a 90nm or more advanced CMOS node
- Other tools, schematic, layout, etc… are optional

Preliminary Schedule

	Topic	Week
I.	Introduction and Linear Systems	Week 1-8
II.	PLL System Analysis	
III.	PLL Building Blocks	
	1st Exam	**Oct 12**
IV.	CDRs	Week 9-14
V.	Broadband Amplifiers	
VI.	Other Topics	
	2nd Exam	**Nov. 30**
	Project Report Due	**Dec. 4**
	Project Presentation	**Dec. 12 (1:00PM – 3:00PM)**

- Dates may change with reasonable notice

High-Speed Electrical Link System

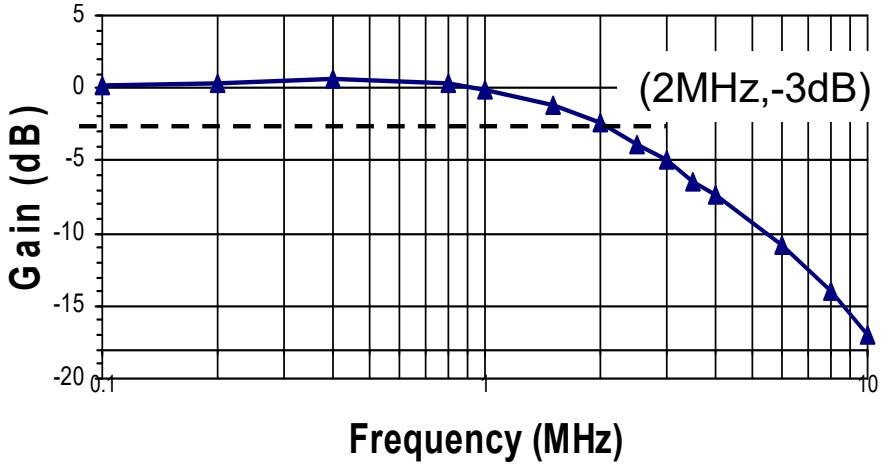


10GHz PLL Example

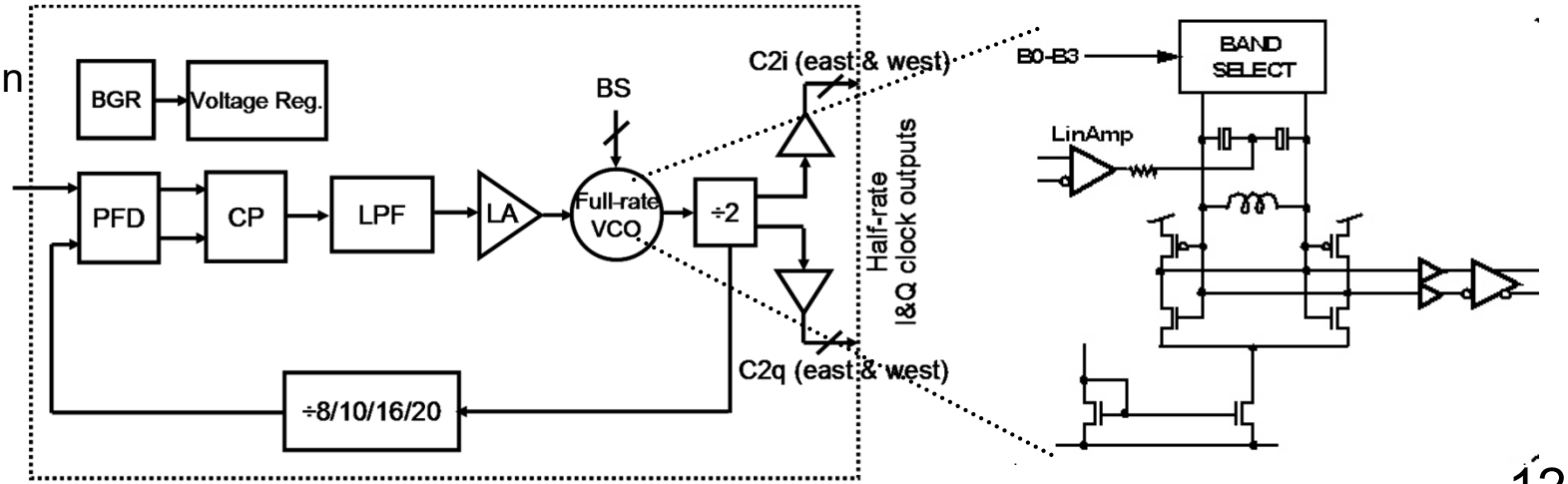
PLL Performance	TxPLL	RxPLL
Min freq (GHz)	**8.98**	**8.96**
Max freq (GHz)	**13.54**	**13.47**
Mean freq (GHz)	**11.26**	**11.22**
Lock range (GHz)	**4.56**	**4.52**
	+/-20.2%	**+/-20.1%**
Fine tune hold range	**5.8%**	**5.8%**
Quarter rate clock phase noise @ 10MHz offset (dBc/Hz)	**-117.8**	**-117.7**
Jitter, 1MHz-100MHz (ps rms)	**1.5**	**1.4**
Jitter, fc/1667-100MHz (ps rms)	**0.64**	**0.64**

[Meghelli (IBM) ISSCC 2006]

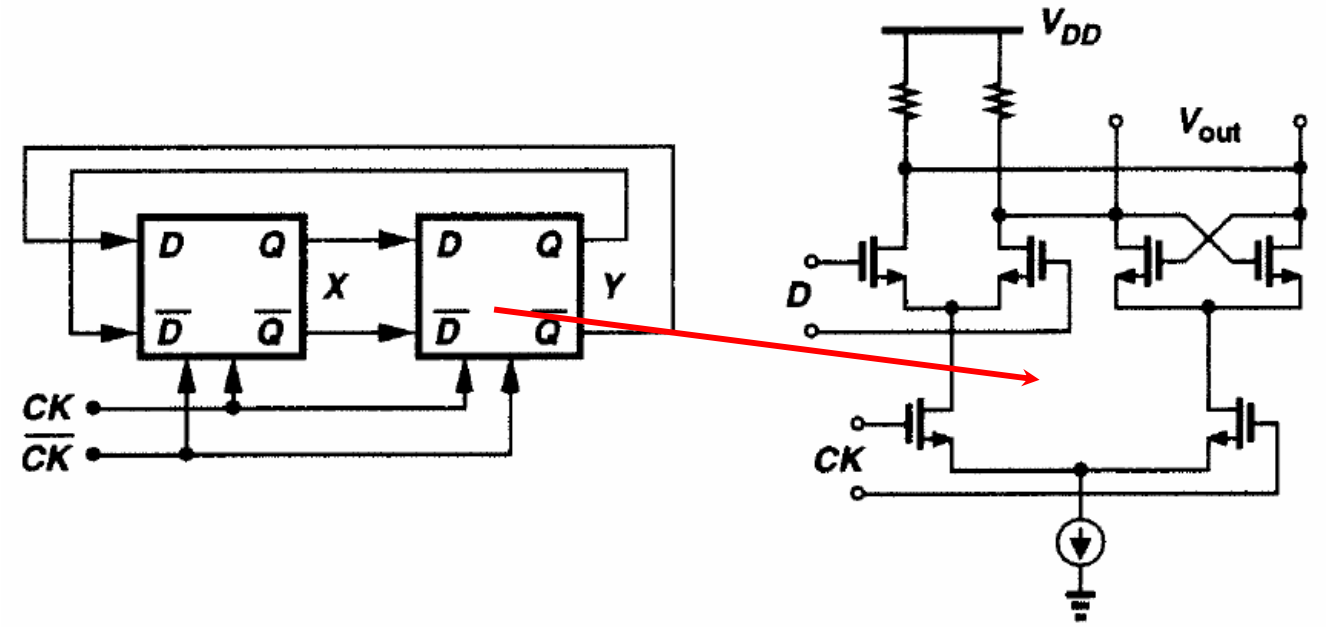
Measured Jitter Transfer Function



100mW Power consumption
(with clock distribution)



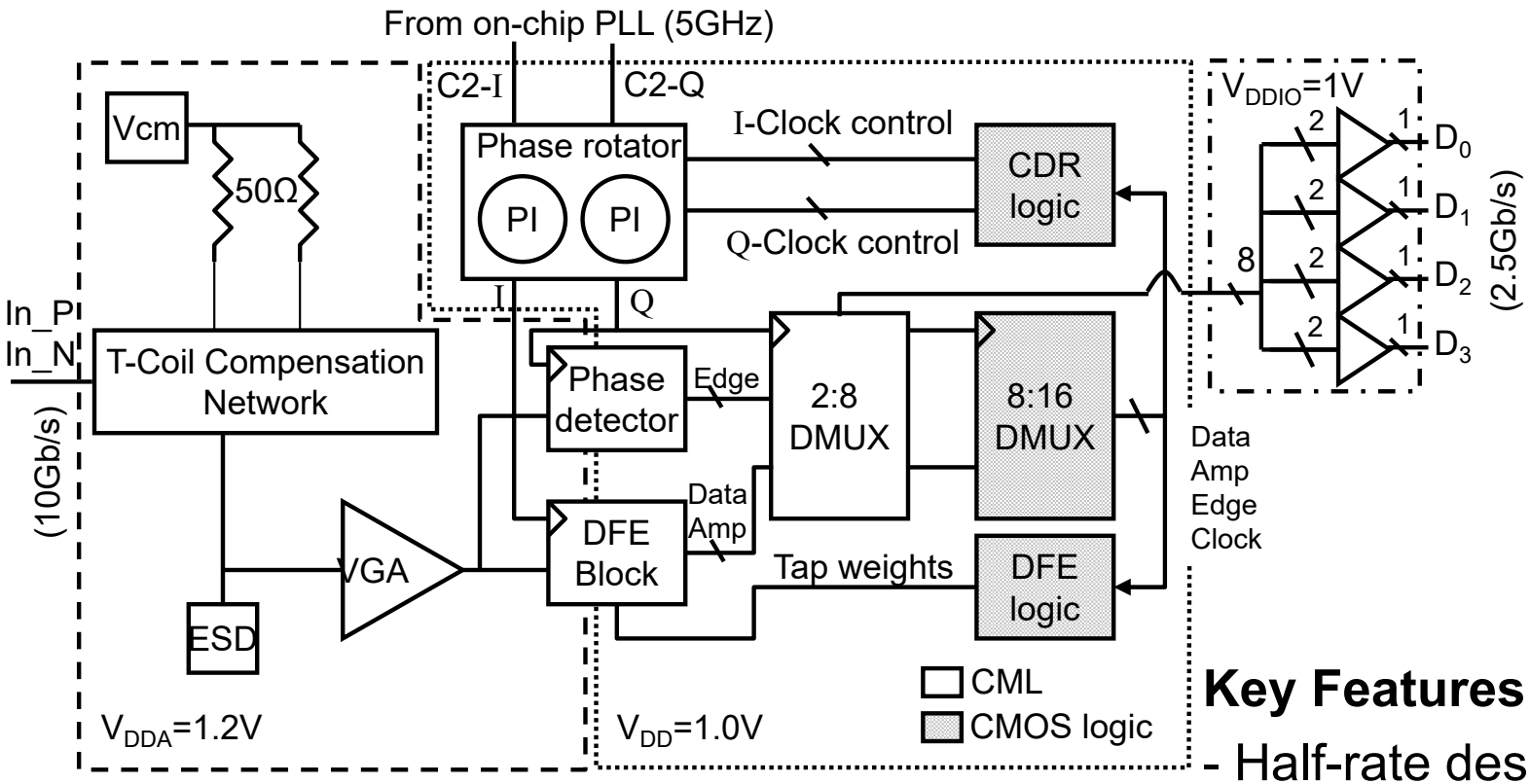
High-Speed Logic Example: Divide-by-2 with CML FF



[**Razavi**]

- High-speed logic blocks are required in numerous high-speed circuits, such as PLLs, CDRs, and equalizers
- Relative to CMOS logic, current-mode logic (CML) circuits can achieve higher bandwidth due to lower self-loading
- Additional bandwidth extension can be achieved with the addition of passives (inductors) and feedback

Detailed Serial-Link Receiver Architecture

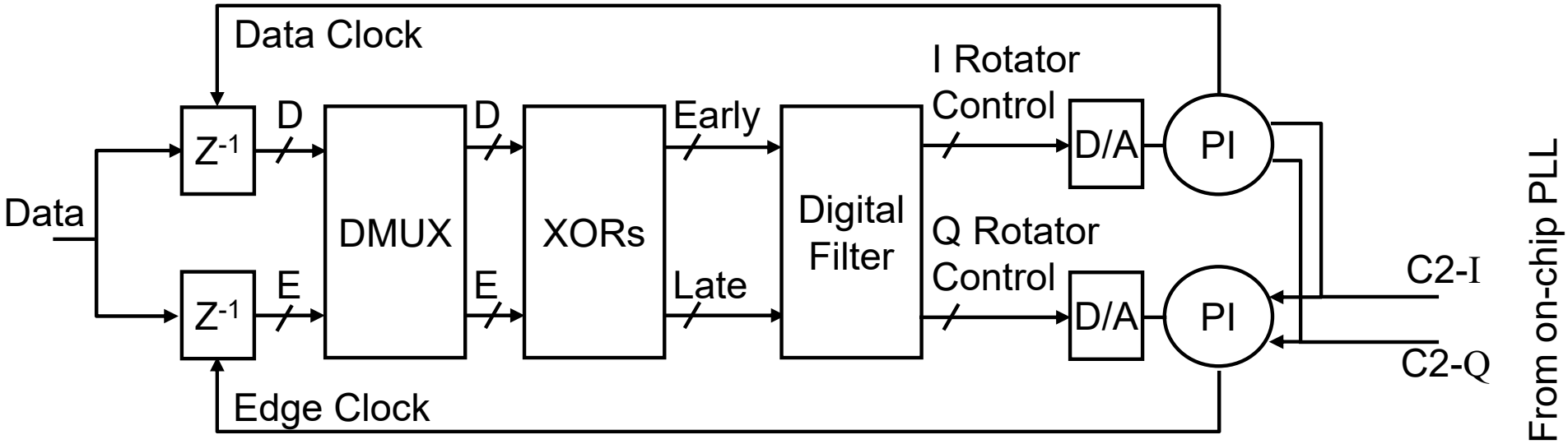


Key Features:

- Half-rate design
- 5-tap continuously adaptive DFE
- Variable gain amplifier
- Digital CDR
- ESD protection (HBM & CDM)
- 130mW (with DFE and CDR logic)

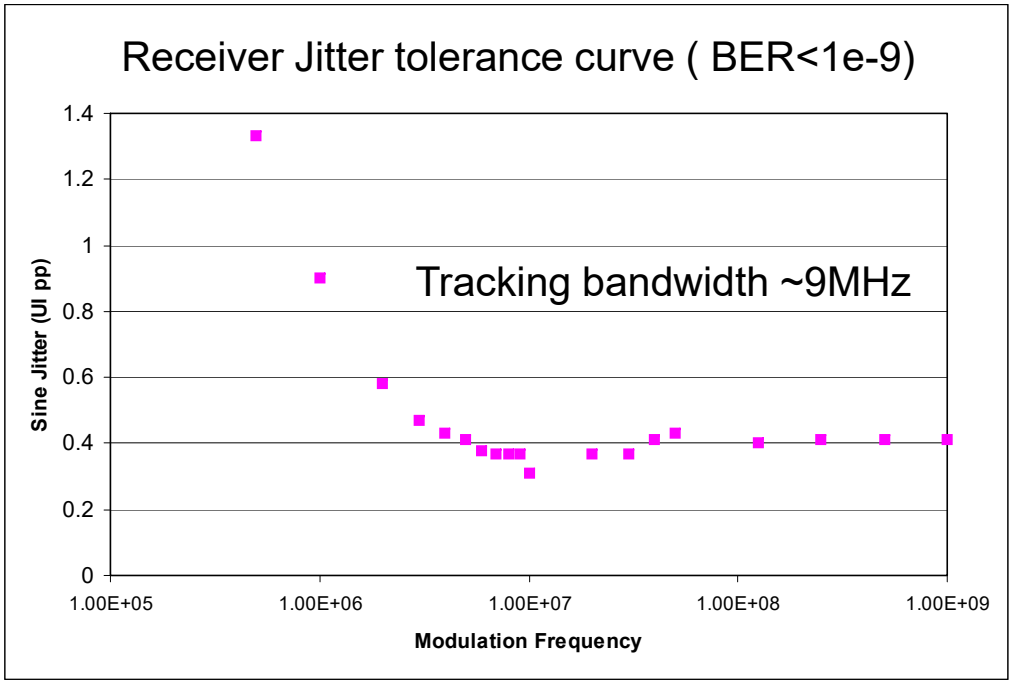
[Meghelli (IBM) ISSCC 2006]

CDR Loop



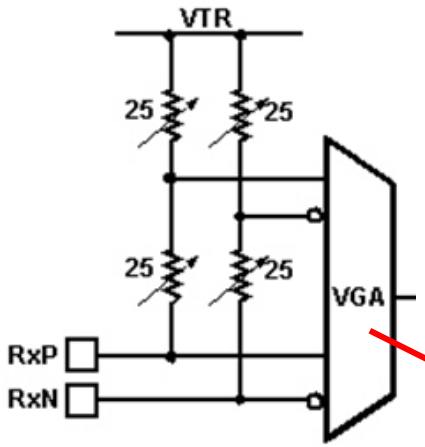
Key Features:

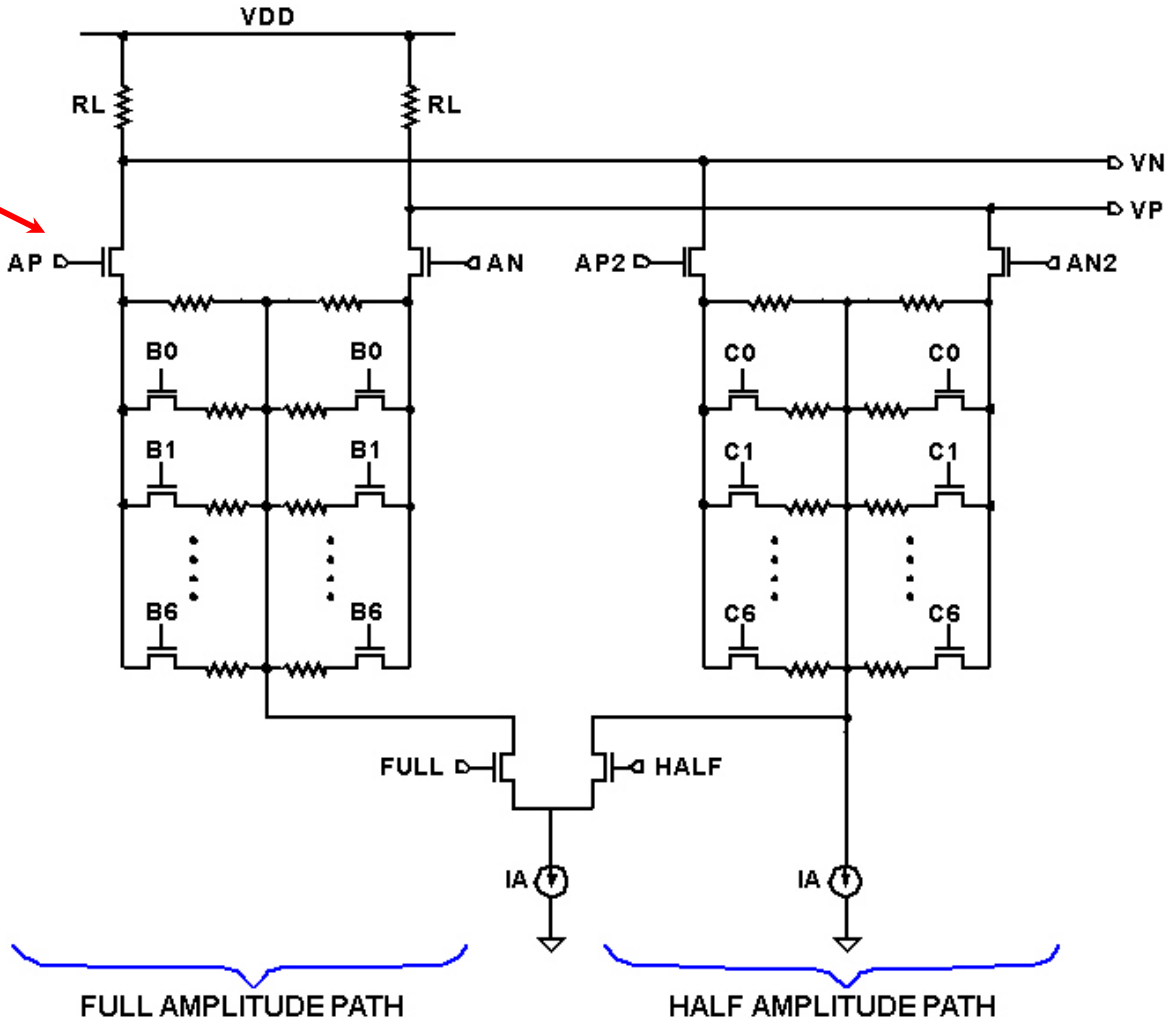
- Fully digital loop
- Can handle up to +/- 4000ppm frequency offset
- Independent I,Q control



[Meghelli (IBM) ISSCC 2006]

Variable-Gain Amplifier (VGA) Example





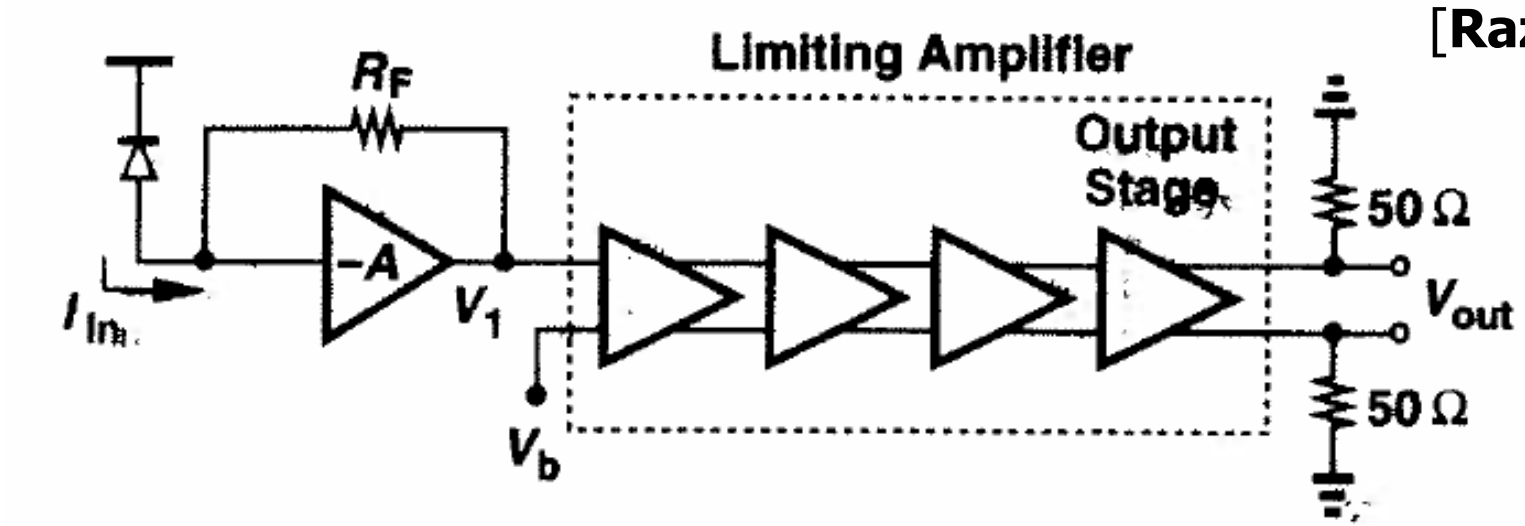
Key Features:

- Dual Diff Amps
  - Half/Full Amplitude
- Switched R Degen
- 7 Bit Thermometer
  - Multi-bit Slewrate
- Glitchless Operation
- Continuous Adjustment
- Optimized with GA

[Sorna (IBM) ISSCC 2005]

Optical Receiver Front-End

[Razavi]



- Transimpedance amplifiers (TIAs) convert an input current signal into an output voltage with a transimpedance gain
- Limiting amplifier amplifies the TIA output to a reliable level to achieve a given BER with a certain decision element (comparator)

Next Time

- Linear circuit analysis review