September 19, 2024

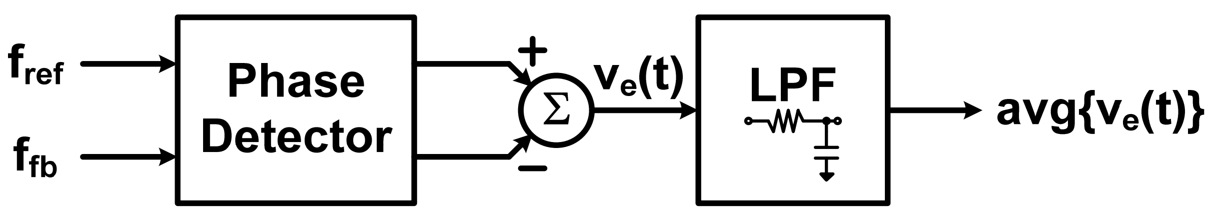
ECEN 620

Homework #2

Due: 10-3-2024, 11:59PM
Homeworks will not be received after due.
Instructor: Sam Palermo

This homework requires transistor-level circuit design for Problem 2 & 3. You may use any CMOS technology to solve the problem, as long as it is a 90nm or more advanced technology node (shorter channel length). For students who do not have access to a design kit, instructions on how to access the default 90nm CMOS transistor models are posted on the website. For this 90nm technology assume a nominal 1.2V supply.

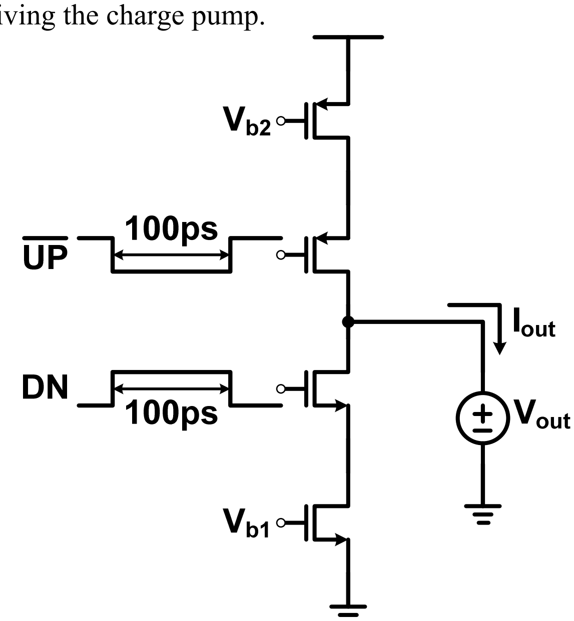
1. **Phase Detector Characterization.**
   a. **For the 4 phase detectors discussed in Lecture 4 (Analog Mixer, XOR, JK Flip-Flop, PFD), produce the phase detector transfer curves (avg(v_e) vs ϕ_e). Find the phase detector gain at the nominal PLL lock point.**
      i. Use the test setup shown in the figure below with $f_{fb}=f_{ref}$. For the analog mixer, use sinusoidal clock inputs. For all the others, use CMOS-level square-wave clocks. Use a VCVS as a buffer between the PD output and the averaging filter. For PDs with 2 outputs, a multi-input VCVS can be used to subtract the 2 outputs before low-pass filtering.
      ii. Plot over a phase range of $\pm 4\pi$, with a minimum of 20 phase points per curve.
      iii. Feel free to use a macro-model approach to generate the phase detector transfer curves, i.e. no transistor-level design is required. Although, if you prefer to implement the circuits at the transistor level, feel free to do so.
   b. **For the 4 phase detectors, find the average output with f_{fb}=0.5, 0.75, 1.5, and $2f_{ref}$. Assume an initial phase difference of 0°. What do these values imply regarding the usefulness of these circuits as a frequency detector?**



Phase Detector Characterization Test Bench

2. **Phase-Frequency Detector Design.** Design at the transistor level a PFD working at 100MHz with a minimum PFD output pulse width of at least 100ps.
   a. Give the transistor-level schematic and simulations showing the minimum PFD pulse width specification is satisfied.
   b. Plot the phase transfer characteristic over a phase range of $\pm 4\pi$, with a minimum of 20 phase points per curve.

3. **Charge Pump Design.** Design at the transistor level a simple charge pump (Lecture 5, Slide 8) that can supply a nominal I_{CP}=100µA and operate with the PFD from Problem 2. **Use one ideal reference current source and appropriate current mirrors to produce the charge pump bias voltages (V_{b1} & V_{b2}).**
   a. Use the test setup shown in the figure below with ideal 100ps switch signals that are in-phase. Use an ideal voltage source at the charge pump output to sense the net output current, I_{out}. From the transient I_{out} response, plot the peak (absolute value) and the average I_{out} as Vout is swept from 0.2*VDD to 0.8*VDD. Compute the phase error produced by the average I_{out} value.
   b. Repeat part (a) using the PFD designed in Problem 2 to produce the charge pump switch signals. Assume the PFD inputs are perfectly in-phase.
   c. Implement appropriate design techniques to improve both the peak and average I_{out} values, assuming the PFD is driving the charge pump.



Simple Charge Pump Characterization Test Bench