# Texas A&M University Department of Electrical and Computer Engineering

## ECEN 620 – Network Theory (Broadband Circuit Design)

### Fall 2024

## Exam #1

### Instructor: Sam Palermo

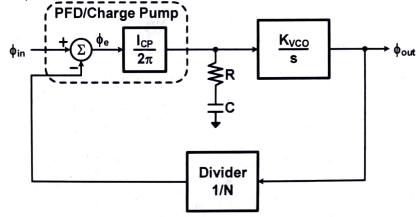
- Please write your name in the space provided below
- Please verify that there are 7 pages in your exam
- You may use <u>one</u> double-sided page of notes and equations for the exam
- Good Luck!

Problem	Score	Max Score
1		50
2		50
Total		100

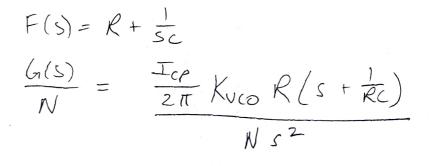
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Problem 1 (50 points)



a) For the PLL block diagram shown above, find the expressions for the product of the forward path gain and feedback factor,  $\frac{G(s)}{N}$ , the closed-loop transfer function  $H(s)=\phi_{out}(s)/\phi_{in}(s)$ , and the phase error transfer function,  $E(s)=\phi_{e}(s)/\phi_{in}(s)$ .



$$H(s) = \frac{G(s)}{1 + \frac{G(s)}{N}} = \frac{\frac{I_{cP}}{2\pi} K_{vco} R(s + \frac{1}{R_c})}{\frac{S^2 + \frac{I_{cP}}{2\pi} K_{vco} R}{N} s + \frac{\frac{I_{cP}}{2\pi} K_{uco}}{N}}$$

$$E(s) = \frac{1}{1 + \frac{G(s)}{N}} = \frac{s^2}{s^2 + \frac{I_{cP}}{2\pi} K_{vco} R}{s^2 + \frac{I_{cP}}{2\pi} K_{vco} R} s + \frac{\frac{I_{cP}}{2\pi} K_{uco}}{N}$$

$$H(s)=\phi_{out}(s)/\phi_{in}(s)=$$

 $E(s) = \phi_e(s)/\phi_{in}(s) =$ 

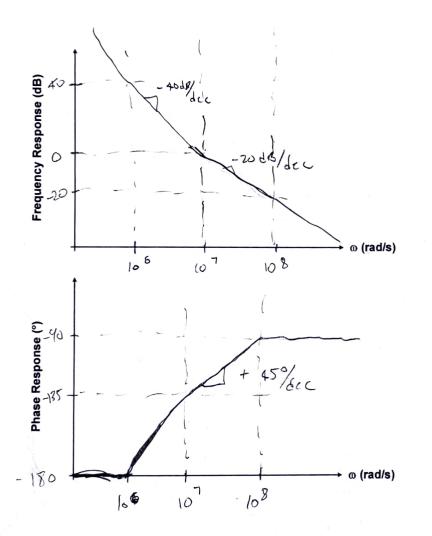
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b) Assume that  $I_{CP}=100\mu$ A, C=100pF,  $K_{VCO}=2\pi^*(10\text{GHz/V})$ , and N=100. What is the R value required for the closed-loop transfer function zero,  $\omega_z$ , to equal 10Mrad/s? Sketch the  $\frac{G(s)}{N}$  Bode Plot (magnitude and phase). What is the phase margin?

$$W_2 = \frac{1}{Rc} \Rightarrow R = \frac{1}{\sqrt{2}c} = \frac{1}{(10^{7} \text{ cm}/\text{s})(100\text{pF})} = 1 \text{ kn}$$

$$\frac{G(S)}{N} = \frac{\binom{100}{217}}{217} \left( \frac{217}{10} \cdot 10^{10} \frac{10}{10} \right) (1kn) (s + 10^7) = \frac{10^9 (s + 10^7)}{100 s^2}$$

$$\frac{100 s^2}{N} = \frac{100}{100 s^2} = \frac{100}{100 s^2}$$



$$R = | kA$$
Phase Margin = 45°
$$OT 51.9°$$
(more exact)

c) Using the same numerical values from part(b), what value should the charge pump current I<sub>CP</sub> be changed to achieve a phase margin of 60°?

$$PM = 180^{\circ} + \angle \frac{G(GWu)}{N} \qquad \frac{G(S)}{N} = \frac{I_{cP}}{\frac{Z+F}{Z+F}} \frac{Kv_{co}R(S+R_c)}{NS^2}$$
$$= 180^{\circ} + \tan^2(W_{u}R_c) - 180^{\circ} = +\sin^2(W_{u}R_c)$$

$$+an'(w_nRC) = 60^{\circ}$$
  
 $w_n = \frac{\sqrt{3}}{RC} = \sqrt{3} w_2 = \sqrt{3} \cdot 10^{7} v_{ad}/_{s}$ 

$$\left| \frac{G(j \omega_{\lambda})}{N} \right| = 1$$

$$\frac{I_{CP}}{2\pi} \left( 2\pi \cdot 10^{10} \frac{42}{V} \right) (1k_{\lambda}) \sqrt{(13 \cdot 10^{7})^{2} + (10^{7})^{2}} = 1$$

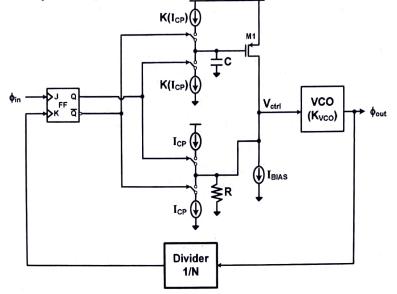
$$I_{OO} \left( \sqrt{13 \cdot 10^{7}} \right)^{2}$$

$$I_{CP} = 150 \text{ mA}$$

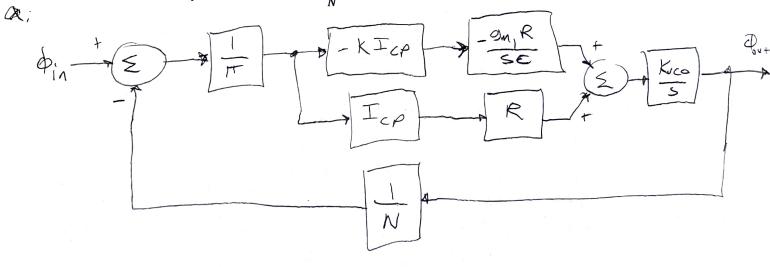
 $I_{CP}$  for 60° Phase Margin =  $150 \mu A$ 

#### Problem 2 (50 points)

For the PLL shown below, assume that the VCO gain is  $K_{VCO}$  is positive, all transistors are operating in saturation with  $r_0=\infty$  and you can ignore any transistor device capacitors.

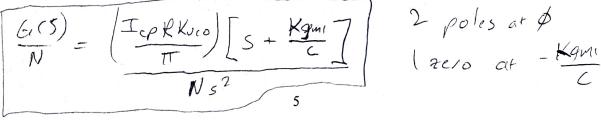


- a) Draw the phase domain small signal model of the loop.
- b) Find the expressions for the product of the forward path gain and feedback factor,  $\frac{G(s)}{N}$ , and determine the pole-zero locations of  $\frac{G(s)}{N}$ .



b.

$$\frac{G(S)}{N} = \frac{1}{TT} \left[ \left( -KI_{CP} \right) \left( -\frac{9u_{R}R}{5c} \right) + I_{CP}R \right] \left( \frac{K_{VCO}}{5c} \right) \left( \frac{1}{N} \right)$$



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c) Assume that  $I_{CP}=100\mu A$ , K=0.1, C=100pF,  $g_{m1}=100\mu A/V$ , R=100 $\Omega$ , and K<sub>VCO</sub>=2 $\pi$ \*(100MHz/V). Calculate the maximum loop division factor, N, for a minimum phase margin of 60°.

$$\frac{G(G)}{N} = \left(\frac{I_{CP}RK_{VLO}}{\pi}\right)\left[S + \frac{K_{gmi}}{C}\right]$$

$$\frac{N_{S}^{2}}{N}$$

C

$$\mathcal{P}M = 180^{\circ} + 2 \frac{GGWu}{N} = 180^{\circ} + 4u^{-1} \left(\frac{W_u C}{K_{gm_1}}\right) - 180^{\circ} = 4u^{-1} \left(\frac{W_u C}{K_{gm_1}}\right)$$
$$tan^{-1} \left(\frac{W_u C}{K_{gm_1}}\right) = 60^{\circ}$$
$$W_u = -\sqrt{3} \frac{K_{gm_1}}{C} = -\sqrt{2} \frac{(0.1)(100\mu)}{100\rho} = \sqrt{2} \frac{10^{\circ}}{100\rho}$$

$$\left|\frac{G(jw_{4})}{N}\right| = 1$$

$$\left[\frac{(100_{4})(100)(2TT.100^{M})}{TT}\right] - \sqrt{(73.10^{5})^{2} + (10^{5})^{2}} = 1$$

$$N(73.10^{5})^{2}$$

$$N = 13.3$$

Max. N for 60° Phase Margin = 13, 3 => 13 (asuming theger)

d) What is the phase relationship between  $\phi_{in}$  and  $\phi_{out}$  when is PLL locked?

$$\phi_{in} - \phi_{out} = 180^{\circ}$$