

Texas A&M University
Department of Electrical and Computer Engineering

ECEN 620 – Network Theory (Broadband Circuit Design)

Fall 2021

Exam #1

Instructor: Sam Palermo

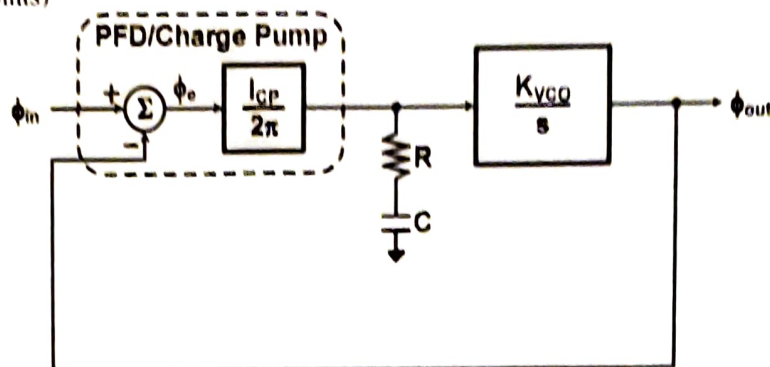
- Please write your name in the space provided below
- Please verify that there are 6 pages in your exam
- You may use one double-sided page of notes and equations for the exam
- Good Luck!

Problem	Score	Max Score
1		55
2		45
Total		100

Name: SAM PALERMO

UIN: _____

Problem 1 (55 points)



- a) For the PLL block diagram shown above, find the expressions for the forward path gain $G(s)$ and the closed-loop transfer function $H(s) = \phi_{out}(s)/\phi_{in}(s)$. (10 points)

$$F(s) = R + \frac{1}{sC}$$

$$G(s) = \frac{\frac{I_{CP}}{2\pi} K_{VCO} R \left(s + \frac{1}{RC} \right)}{s^2}$$

$$H(s) = \frac{G(s)}{1 + G(s)} = \frac{\frac{I_{CP}}{2\pi} K_{VCO} R \left(s + \frac{1}{RC} \right)}{s^2 + s \frac{I_{CP}}{2\pi} K_{VCO} R + \frac{\frac{I_{CP}}{2\pi} K_{VCO}}{C}}$$

$$H(s) = \phi_{out}(s)/\phi_{in}(s) =$$

- b) Assume that $\frac{I_{CP}}{2\pi} = 10 \mu A/(2\pi)$, $K_{VCO} = 2\pi \cdot (100 \text{ MHz/V})$, and that $R=0$. What is the value of C required for a ~~loop~~ ^{forward path} gain unity-gain crossover frequency of 1 Mrad/s ? What is the phase margin? (10 points)

$$\omega/R=0 \Rightarrow G(s) = \frac{\frac{I_{CP}}{2\pi} K_{VCO}}{s^2 C} = \frac{\frac{10 \mu A}{2\pi} (2\pi \cdot 100 \text{ MHz/V})}{s^2 C}$$

$$\left| G(j 10^6) \right| = \frac{\left(\frac{10 \mu A}{2\pi} \right) (2\pi \cdot 100 \text{ MHz/V})}{(10^6 \text{ rad/s})^2 C} = 1$$

$$C = 1 \text{ nF} \quad \text{PM} = 180^\circ + \angle G(j 10^6) = 180^\circ - 180^\circ = 0^\circ$$

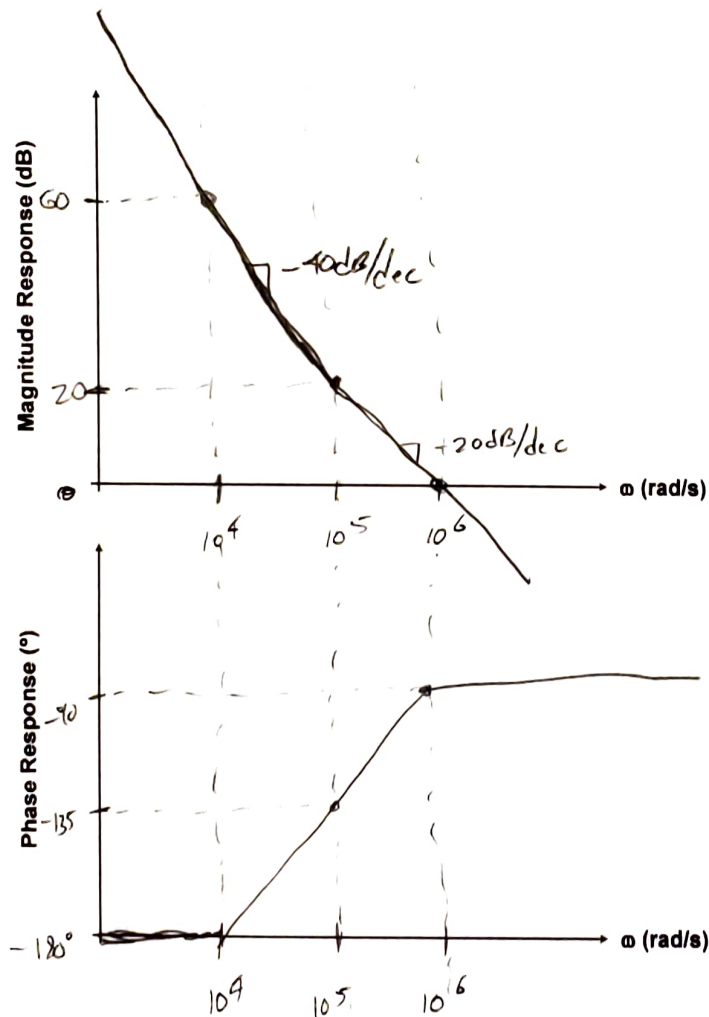
$$C = 1 \text{ nF} \quad \text{Phase Margin} = 0^\circ$$

- c) Now assume that $C=10\text{nF}$. Note, this is not the answer to (b). What is the R value required for the closed-loop transfer function zero, ω_z , to equal 100krad/s ? Sketch the $G(s)$ Bode Plot (magnitude and phase). What is the phase margin now? (20 points)

$$\omega_z = \frac{1}{RC} \Rightarrow R = \frac{1}{\omega_z C} = \frac{1}{(10^5 \text{ rad/s})(10\text{nF})} = 1\text{k}\Omega$$

$$G(s) = \frac{\frac{10\mu\text{A}}{2\pi} (2\pi \cdot 10^8)(1\text{k})(s + 10^5)}{s^2} = \frac{10^6 (s + 10^5)}{s^2}$$

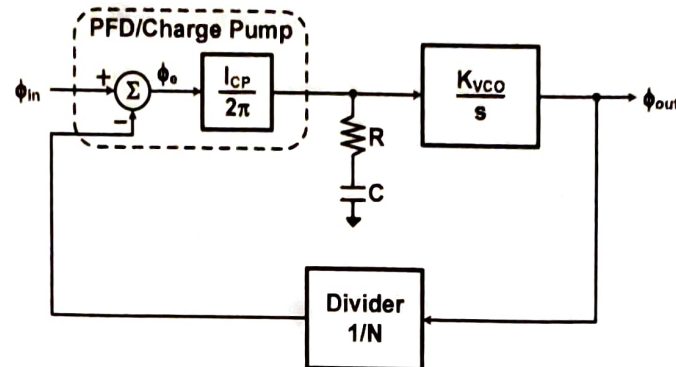
$$A + \omega = 10^4 \quad |G| \approx \frac{10^6 (10^5)}{10^8} = 10^3$$



$$R = 1\text{k}\Omega$$

$$\text{Phase Margin} = \sim 90^\circ$$

- d) Now assume that the PLL is modified to include a loop divider. Using the same numerical values from part(c), what is the maximum loop division factor, N , for a minimum phase margin of 30° ? (15 points)



$$\frac{G(s)}{N} = \frac{\frac{I_{CP}}{2\pi} K_{VCO} R (s + \frac{1}{RC})}{N s^2}$$

$$PM = 180^\circ + \angle \frac{G(j\omega_u)}{N} = 180^\circ + \tan^{-1}(\omega_u RC) - 180^\circ$$

$$= \tan^{-1}(\omega_u RC) = 30^\circ$$

$$\omega_u = \frac{1}{\sqrt{3} RC} = \frac{\omega_z}{\sqrt{3}} = \frac{10^5}{\sqrt{3}}$$

$$\left| \frac{G(j\omega_u)}{N} \right| = 1$$

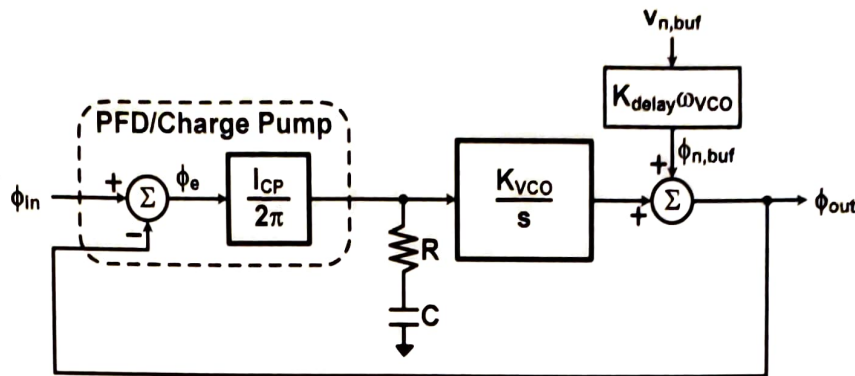
$$\frac{\left(\frac{10 \mu A}{2\pi}\right) (2\pi \cdot 10^8) (1k) \sqrt{\left(\frac{10^5}{\sqrt{3}}\right)^2 + (10^5)^2}}{N \left(\frac{10^5}{\sqrt{3}}\right)^2} = 1$$

$$N = 34.6$$

Max. N for 30° Phase Margin = $34.6 \Rightarrow 34$ (assuming only integer)

Problem 2 (45 points)

This problem investigates how voltage noise on an inside-the-loop post-VCO buffer impacts the output phase noise. Assume that the post-VCO buffer noise is modeled as an additive phase noise term, as shown in the model below.



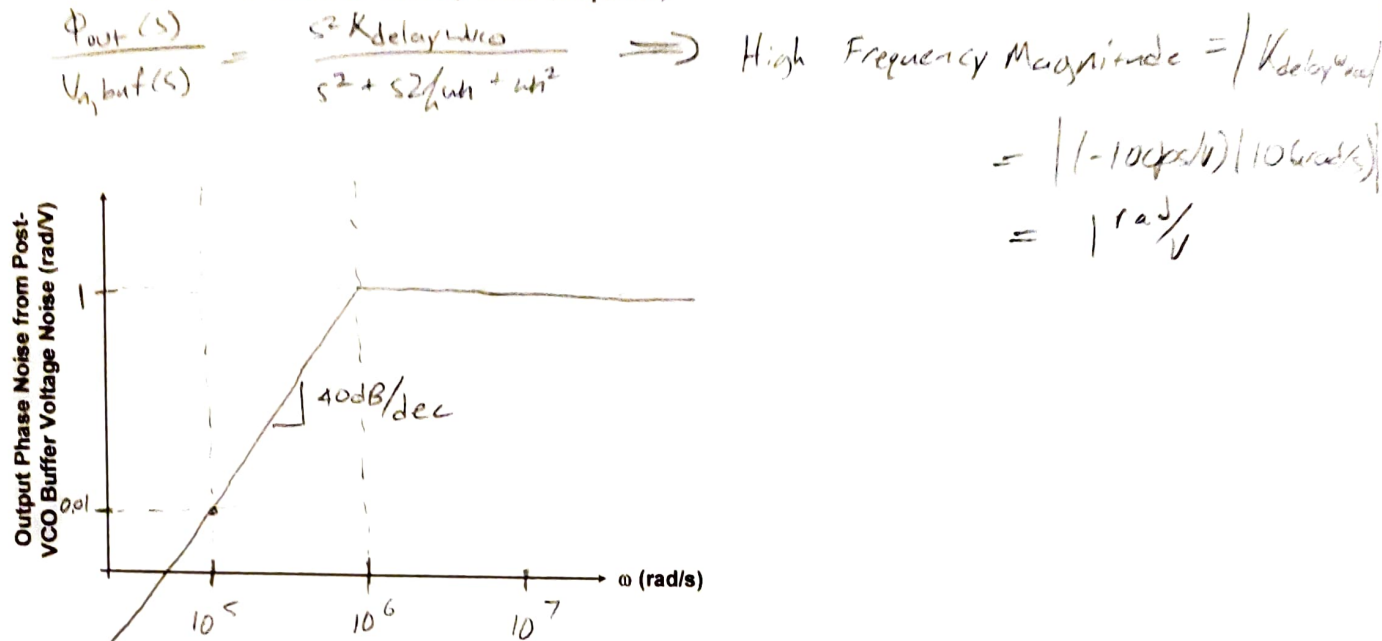
- a) Find the expression for the post-VCO buffer voltage noise induced phase noise transfer function, $T(s) = \phi_{out}(s)/v_{n,buf}(s)$. (15 points)

$$\frac{\phi_{out}(s)}{v_{n,buf}(s)} = \frac{s^2 K_{delay} \omega_{VCO}}{s^2 + 2\zeta \omega_n + \omega_n^2}$$

$$\text{where } \omega_n = \sqrt{\frac{I_{CP} K_{VCO}}{2\pi C}} \quad \text{and } \zeta = \frac{\omega_n}{2} RC$$

$$T(s) = \phi_{out}(s)/v_{n,buf}(s) =$$

- b) Assume that the PLL has been designed for $\omega_n = 1 \text{ Mrad/s}$ and $\zeta = 1$. Also, assume that $\omega_{VCO} = 10 \text{ Grad/s}$ and $K_{\text{delay}} = -100 \text{ ps/V}$. Sketch the post-VCO buffer voltage noise induced phase noise **magnitude versus frequency**. Label the high frequency value and the key frequencies and slopes in the plot. Use a log scale for both the x and y-axis. (10 points)



- c) Assume that the post-VCO buffer voltage noise has sinusoidal modulation.

$$v_{n,\text{buf}}(t) = 0.1 \sin(10^7 t) \text{ (V)}$$

What is the output jitter amplitude in ps? (10 points)

10^7 is well above the 2-poles, in the high-pass region

$$\text{Output jitter amplitude} = (1 \text{ rad/V})(100 \text{ mV}) = 0.1 \text{ rad}$$

$$\text{At } 10 \text{ Grad/s} \Rightarrow 0.1 \text{ rad} \left(\frac{2\pi(100 \text{ ps})}{2\pi \text{ rad}} \right) = 10 \text{ ps}$$

$$\text{Output Jitter Amplitude (ps)} = 10 \text{ ps}$$

- d) Assuming 10^5 rad/s sinusoidal noise, what is the maximum voltage amplitude for an output jitter amplitude of 0.5 ps ? (10 points)

$$\text{At } 10^5 \text{ rad/s} \Rightarrow 0.01 \text{ rad/V}$$

$$\text{Output jitter amplitude} = V_{\text{amp}}(0.01 \text{ rad/V}) \left(\frac{2\pi(100 \text{ ps})}{2\pi \text{ rad}} \right) = 0.5 \text{ ps}$$

$$V_{\text{amp}} = 0.5 \text{ V}$$

$$\text{Max Voltage Amplitude} = 500 \text{ mV}$$

Scratch Paper