30.5 90nm 4.7ps-Resolution 0.7-LSB Single-Shot Precision and 19pJ-per-Shot Local Passive Interpolation Time-to-Digital Converter with On-Chip Characterization

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Time-to-digital converters (TDC) support the industry wide trend of replacing mixed-signal functionality by digital realizations. High-resolution TDCs [1] become increasingly popular for time-of-flight measurements, full-speed testing, e.g., jitter measurement, clock and data recovery, measurement and instrumentation, and digital PLLs. As the speed leverage of technology scaling decreases below 100nm, robust TDCs with sub-gate-delay resolution are essential. The Vernier TDC [2] requires long delay lines, thus suffers from large latency, area and power consumption. Latency and a resolution limited by the inherent variation-related pulse-width modification are the drawbacks of the pulse-shrinking approach [3]. Parallel gradual-delay elements [4] are particularly susceptible to process variations. The same holds for analog operations on time intervals like delay amplification [5]. Ultra high-resolution TDCs [6] achieve sub-ps resolution but require iterative conversion.

A local passive interpolation TDC (LPITDC) [7] is shown in Fig. 30.5.1. Coarse delay resolution is achieved with a differential delay line. Sub-gate-delay resolution is accomplished by passive interpolation of 2 signals with the same switching direction but one inverter delay skew. Both the delay line and the interpolators are inherently monotonic. Salicide blocked poly resistors do not cause process overhead and provide best linearity. Thermal noise causing kT/C noise at the comparator inputs is negligible for signal slopes in the order of the gate delay. Several actions have been taken to provide a robust design: Differential sense amplifiers with large input devices (to minimize mismatch) are used as comparators. History effects from prior conversions are eliminated by the precharge. Comparators and delay elements are supplied by separate power networks and placed in separate wells. This assures undisturbed signal propagation in the delay line even if the stop signal starts to propagate in the clock tree of the comparators. The local wiring of the delay elements is shielded to avoid cross-coupling.

Delay variation and also nonlinearity increase with sqrt(N) where N is the number of delay elements. N is limited by a loop structure. The start impulse is injected via the multiplexed input of the first delay element. For matching reasons, all other delay cells have a second dummy input. The time when the loop is closed is chosen to capture the start signal safely. No signal out of the delay line is used to control the multiplexer, as this would introduce irregularity and compromise linearity. For the same reason, there is no interpolation between the splitter and the first inverter. Instead, the stop signal is delayed, so the start signal is injected deep into the chain even for small time intervals. The resulting offset error is compensated digitally.

The classical approach to cope with global process variations is the use of a DLL to tune the delay elements. However, this requires analog overhead and yields only a factor of sqrt(2) in linearity. The high resolution of the LPITDC enables digital compensation of global process variations. The free-running frequency of the delay line can be used as a process monitor to disable a subset of the comparators for nominal and fast process conditions.

For absolute time measurement calibration, i.e., gain correction is required, e.g., during calibration cycles. The measurement results of the TDC can then be normalized digitally to the full-scale value. The measurement of timing ratios, e.g., phases or duty cycles, requires no calibration. The monotonic conversion characteristics of the LPITDC allow for digital nonlinearity compensation. Therefore, an on-chip calibration circuit characterizes the converter. The correction words may be stored and added to the output word of the TDC. Figure 30.5.2 shows the implemented calibration circuit in detail. A characterization pulse is delayed in 2 delay lines and serves as both start and stop signal. The start delay line has a fixed delay whereas the stop delay can be changed. For coarse delay tuning, additional buffers are inserted; fine delay tuning is achieved by a chain of current-starved inverters where the gate potential of the header and footer devices can be controlled. To map the TDC output word to an absolute time interval the chains can be configured as ring oscillators. During a time period determined by a stable reference clock the number of periods of both oscillators is counted. With these counter values the delay difference, i.e., the time interval can be calculated. For offset characterization, the same signal is applied to the start and the stop input. For compensation the resulting value is subtracted from all further measurements.

The measured converter characteristics of a 7b LPI delay chain without digital nonlinearity correction are shown in Fig. 30.5.3. The circuit is implemented in a 90nm standard CMOS process with 4× interpolation. The resolution is 4.7ps at 1.2V and 3.9ps at 1.4V supply. The intrinsic monotony indeed translates into a strict monotonic converter characteristics. An integral nonlinearity of ±1.2 LSB and a differential nonlinearity of ±0.6 LSB are achieved. Beside the linearity, the single-shot precision is an important metric to describe the time resolution capability. It is defined as the standard deviation of the codewords at the output if a constant time interval is measured repeatedly. Figure 30.5.4 shows the mean output values and the single-shot precision for repeated measurement of a fine granular delay sweep. The histograms (dashed line indicates mean value) illustrate how the output statistics changes for increasing time intervals. For repeated measurements of slowly varying signals, the finite single-shot precision dithers the output values, so averaging of multiple measurements results reduces the quantization error, i.e., increases the effective resolution. These results, especially the strict monotony, suggest that an even higher resolution is achievable by an increased interpolation factor. For an operation frequency of 180MHz at 1.2V, the supply current is 3mA corresponding to an energy of 19pJ/measurement.

In low-cost applications with simple clock generators, clock jitter limits the effective resolution of picosecond TDCs. An active jitter-compensation technique is shown in Fig. 30.5.5. A tracking unit determines the actual jitter and corrects the output of the main TDC. Therefore, the clock period is continuously measured by the auxiliary TDCs. A digital LPF eliminates jitter and calculates the average clock period. The difference of the actual and the average period is integrated to obtain the correction word. As the jitter is actually measured, no prerequisites on the jitter statistics are required. For a $10ps_{rms}$ long-term jitter of the reference clock, the presented TDC limits the error to ±1LSB.

Figure 30.5.6 gives a comparison with previously published TDCs. Among the variation-robust TDCs, the best resolution with low area and power consumption is achieved. The on-chip calibration allows for accurate testing on digital standard testers, adaptation to environmental conditions and aging.

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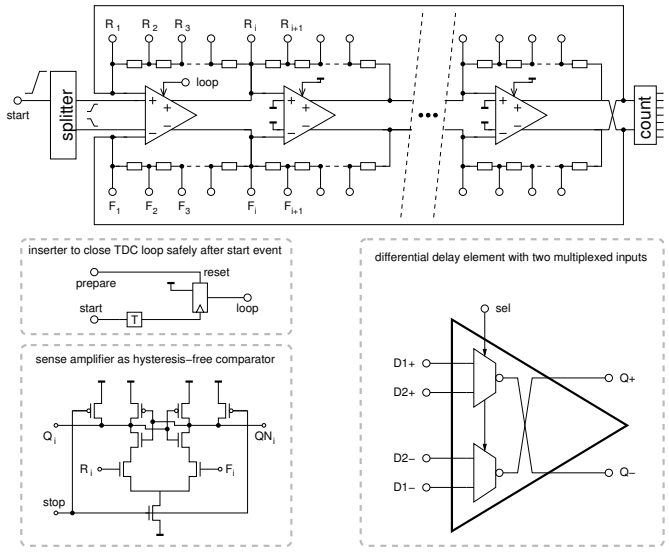

Figure 30.5.1: Local passive interpolation TDC in loop structure.

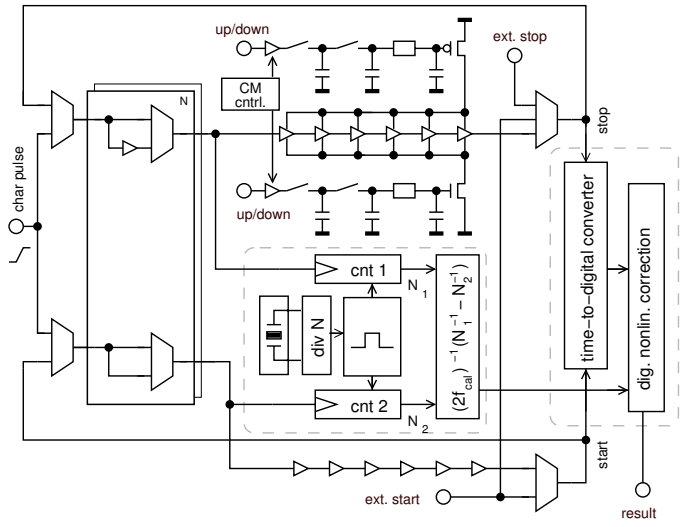

Figure 30.5.2: On-chip TDC characterization and calibration unit.

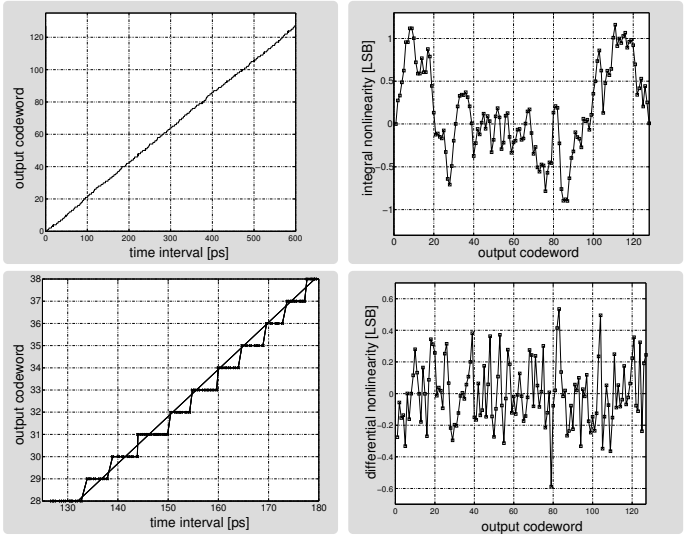

Figure 30.5.3: Measured TDC characteristics and non-linearity plots.

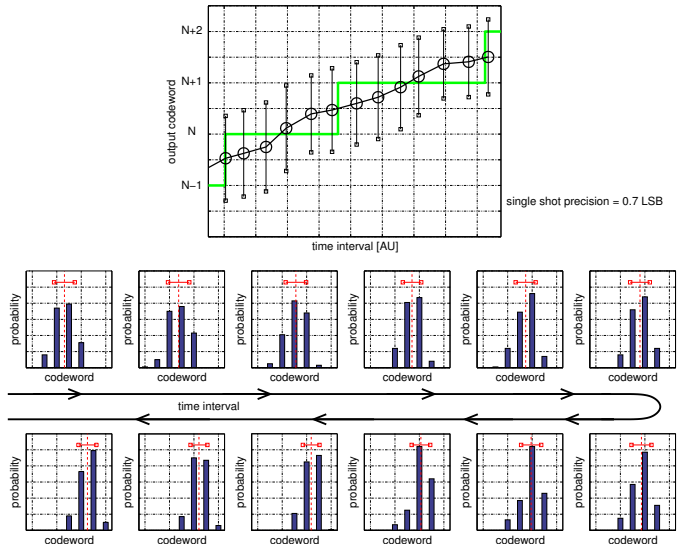

Figure 30.5.4: Measured single-shot precision.

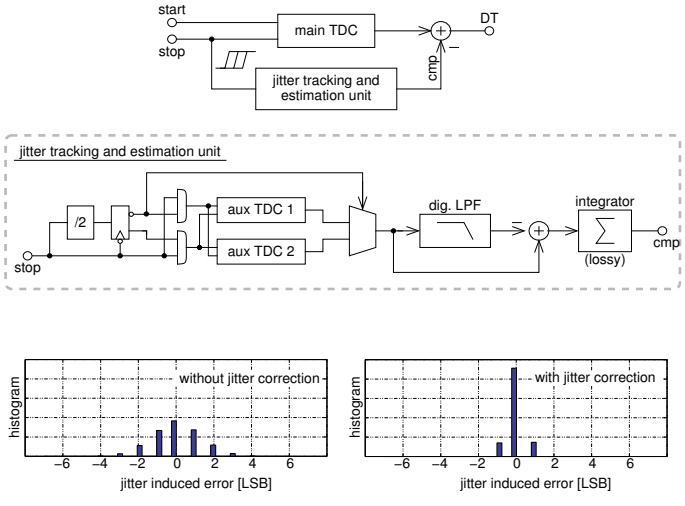

Figure 30.5.5: Reference-clock jitter compensated TDC.

ref.	technique	tech. [nm]	resol. [ps]	single shot precision	INL [LSB]	INL [ps]	DNL [LSB]	DNL [ps]	power[1]	area [mm^2]	variation robustness
[1]	delay line	90	20.0		0.7	14.0	0.6	12.0	157	0.01	++
[2]	vernier	700	30.0	0.7 LSB	1.3	39.0				10	+
[3]	pulse shrinking	350	68.0	0.8 LSB					1102	0.03	–
[4]	parallel del. elements	350	12.2		1.6	19.5			735	7.5	––
[5]	delay amplification	90	1.25		3.0	3.7	0.8	1.0	300	0.6	––
[6]	scrambling	130								0.02	
this	loc. passive interpol.	90	4.7	0.7 LSB	1.2	5.6	0.6	2.8	14	0.02	++

[1] normalized power defined by (1MHz x P)/(V_{DD}^2 x f)

Figure 30.5.6: Comparison with prior-art.

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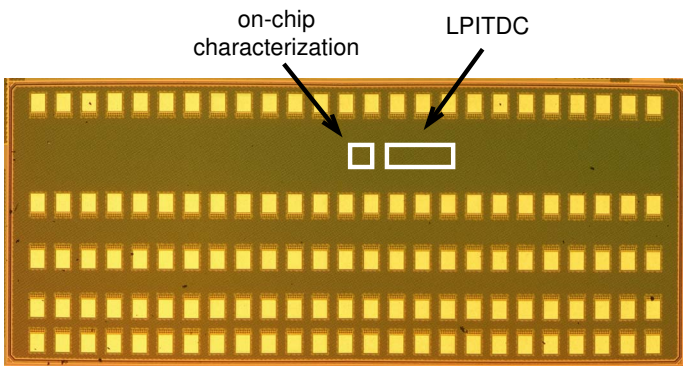

Figure 30.5.7: Chip micrograph.

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