ECEN474: (Analog) VLSI Circuit Design

Fall 2012

Lecture 17: Fully Differential Amplifiers & CMFB

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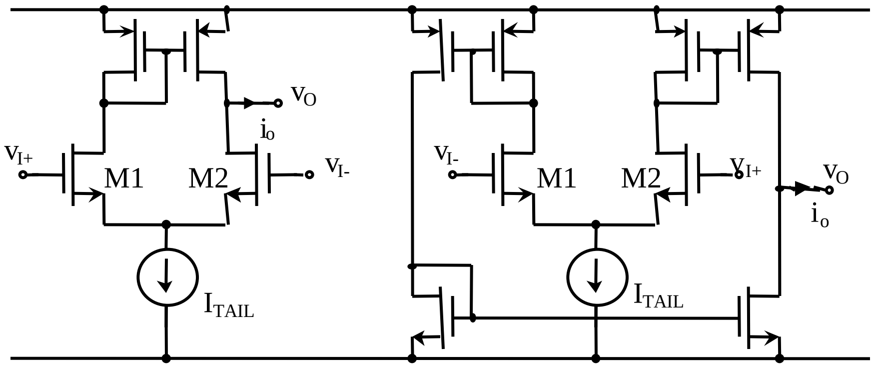
Announcements & Agenda

- Preliminary report due 11/19

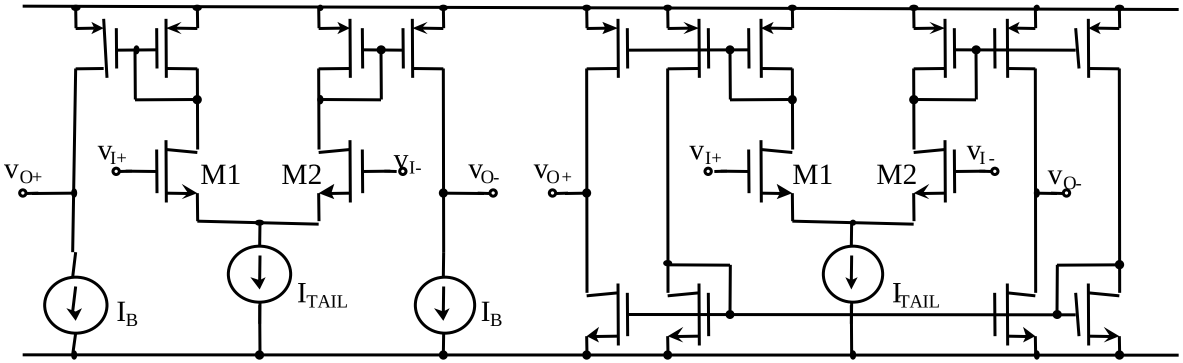
- Fully differential circuits
- Common-mode feedback circuits

Basic Operational Transconductance Amplifier Topologies



(a) (b)

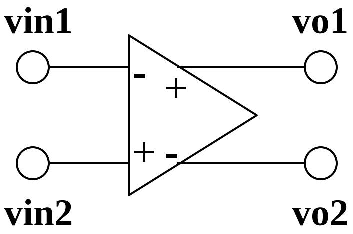
SINGLE-ENDED



(c) (d)

FULLY-DIFFERENTIAL

Fully-Differential Circuits



In general:

$$v_{o1} = \frac{v_{o1} - v_{o2}}{2} + \frac{v_{o1} + v_{o2}}{2} = \frac{v_{od}}{2} + v_{oc}$$

$$v_{o2} = \frac{v_{o2} - v_{o1}}{2} + \frac{v_{o1} + v_{o2}}{2} = -\frac{v_{od}}{2} + v_{oc}$$

- Hence

$$\begin{bmatrix} \mathrm{v}_{\mathrm{od}} \\ \mathrm{v}_{\mathrm{oc}} \end{bmatrix} = \begin{bmatrix} \mathrm{A}_{\mathrm{dd}} & \mathrm{A}_{\mathrm{dc}} \\ \mathrm{A}_{\mathrm{cd}} & \mathrm{A}_{\mathrm{cc}} \end{bmatrix} \begin{bmatrix} \mathrm{v}_{\mathrm{id}} \\ \mathrm{v}_{\mathrm{ic}} \end{bmatrix}$$

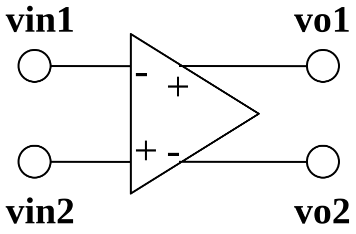
Differential-mode output

Common-mode output

$$\mathrm{A}_{\mathrm{dd}} = \left.\frac{\mathrm{v}_{\mathrm{od}}}{\mathrm{v}_{\mathrm{id}}}\right|_{\mathrm{Vic}=0} \qquad \mathrm{A}_{\mathrm{dc}} = \left.\frac{\mathrm{v}_{\mathrm{od}}}{\mathrm{v}_{\mathrm{ic}}}\right|_{\mathrm{Vid}=0}$$

$$\mathrm{A}_{\mathrm{cd}} = \left.\frac{\mathrm{v}_{\mathrm{oc}}}{\mathrm{v}_{\mathrm{id}}}\right|_{\mathrm{Vic}=0} \qquad \mathrm{A}_{\mathrm{cc}} = \left.\frac{\mathrm{v}_{\mathrm{oc}}}{\mathrm{v}_{\mathrm{ic}}}\right|_{\mathrm{Vid}=0}$$

Fully-Differential Filters: Effects of current source inpedance and mismatches



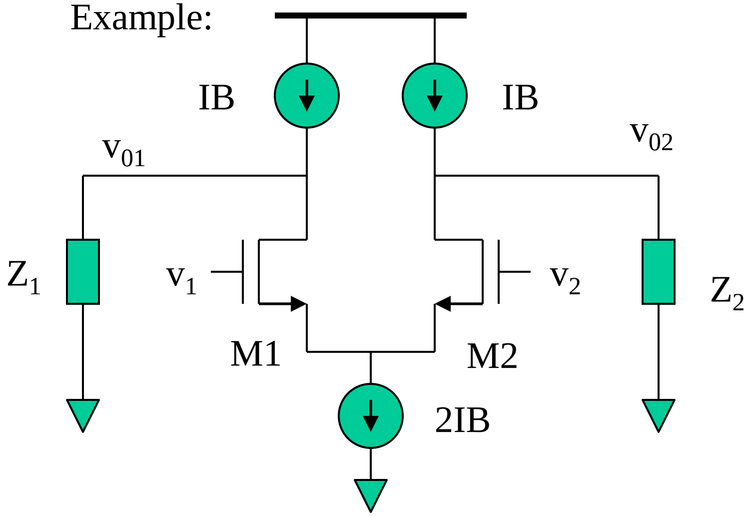
A very important parameter:

$$\mathrm{CMRR} = \frac{A_{dd}}{A_{dc}}$$

w/ $v_{id} = v_{i2} - v_{i1}$ **and** $v_{ic} = \dfrac{v_{i2} + v_{i1}}{2}$

Solving the circuit:

Example:



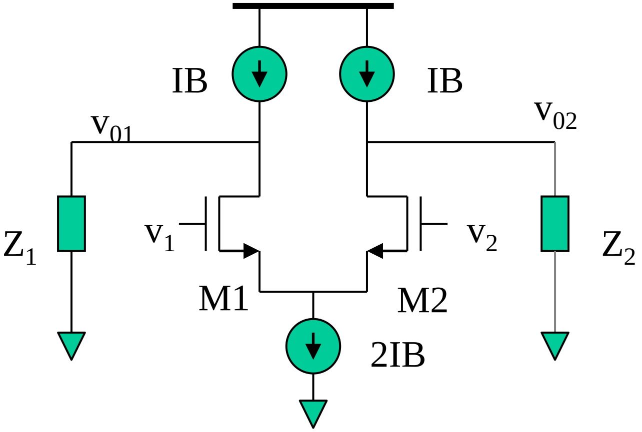
$$v_{01} = \frac{g_{m1} g_{m2} Z_1}{g_{m1} + g_{m2} + Y_s}\left[\left(1 + \frac{Y_s}{2g_{m2}}\right)v_{id} - \left(\frac{Y_s}{g_{m2}}\right)v_{ic}\right]$$

$$v_{02} = \frac{g_{m1} g_{m2} Z_2}{g_{m1} + g_{m2} + Y_s}\left[-\left(1 + \frac{Y_s}{2g_{m1}}\right)v_{id} - \left(\frac{Y_s}{g_{m1}}\right)v_{ic}\right]$$

Y_s is the admittance associated with the current source 2IB

Fully-Differential Filters: Non-idealities

Voltage gain: Note the effects of the mismatches, especially in A_{dc} and A_{cd}



$$A_{dd}=\left.\frac{v_{o1}-v_{o2}}{v_{i2}-v_{i1}}\right|_{v_{ic}=0}=\frac{g_{m1}g_{m2}}{g_{m1}+g_{m2}+Y_s}\left[Z_1+Z_2+\frac{Y_s}{2}\left(\frac{Z_1}{g_{m2}}+\frac{Z_2}{g_{m1}}\right)\right]$$

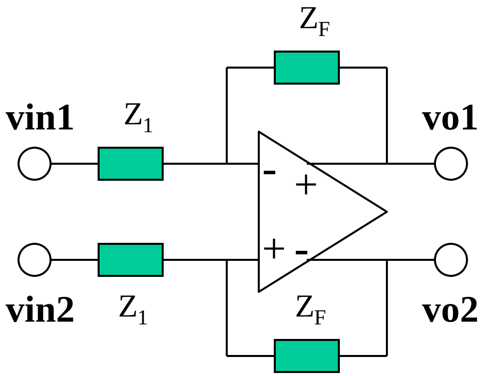
$$A_{dc}=\left.\frac{v_{o1}-v_{o2}}{(v_{i2}+v_{i1})/2}\right|_{v_{id}=0}=\frac{g_{m1}g_{m2}}{g_{m1}+g_{m2}+Y_s}\left[Y_s\left(\frac{Z_2}{g_{m1}}-\frac{Z_1}{g_{m2}}\right)\right]$$

$$A_{cd}=\left.\frac{(v_{o2}+v_{o1})/2}{v_{i2}-v_{i1}}\right|_{v_{ic}=0}=\frac{g_{m1}g_{m2}}{g_{m1}+g_{m2}+Y_s}\left(\frac{1}{2}\right)\left[Z_1-Z_2+\frac{Y_s}{2}\left(\frac{Z_1}{g_{m2}}-\frac{Z_2}{g_{m1}}\right)\right]$$

$$CMRR=\frac{A_{dd}}{A_{dc}}\cong\frac{g_{m1}\left(1+\dfrac{Z_1}{Z_2}\right)}{Y_s\left(1-\dfrac{g_{m1}Z_1}{g_{m2}Z_2}\right)}$$

$$A_{cc}=\left.\frac{(v_{o2}+v_{o1})/2}{(v_{i2}+v_{i1})/2}\right|_{v_{id}=0}=-\frac{g_{m1}g_{m2}}{g_{m1}+g_{m2}+Y_s}\left(\frac{1}{2}\right)\left[Y_s\left(\frac{Z_2}{g_{m1}}+\frac{Z_1}{g_{m2}}\right)\right]$$

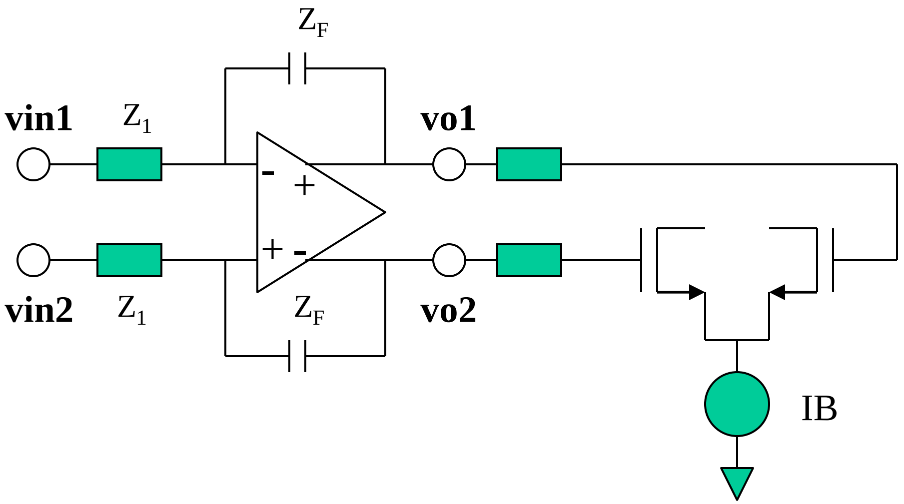
Fully-Differential Circuits



- **Ideal voltage gain**

$$A_{dd} = \frac{v_{01} - v_{02}}{v_{in2} - v_{in1}} = \frac{Z_f}{Z_1}$$

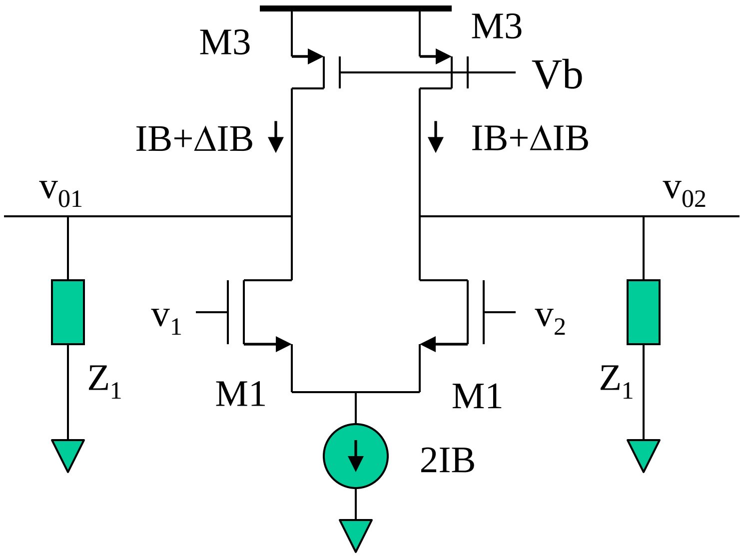
- **Ideally even-order distortions are cancelled**
- **Ideally common-mode signals are rejected**
- **What sets the output common-mode of these circuits?**
  - **Function of the amplifier output resistance**



Common-mode offsets can impact the performance of the following stages

- **Can exceed the common-mode input range of preceeding stages**
- **With finite A_{cc} can accumulate in a multi-stage amplifier circuit**

Fully-Differential Amplifiers: COMMON-MODE DC offset



✓**If ΔIB is positive transistors M3 eventually will be biased in triode region (small resistance)**

✓**dc gain reduces drastically**

✓**Linear range is further minimized**

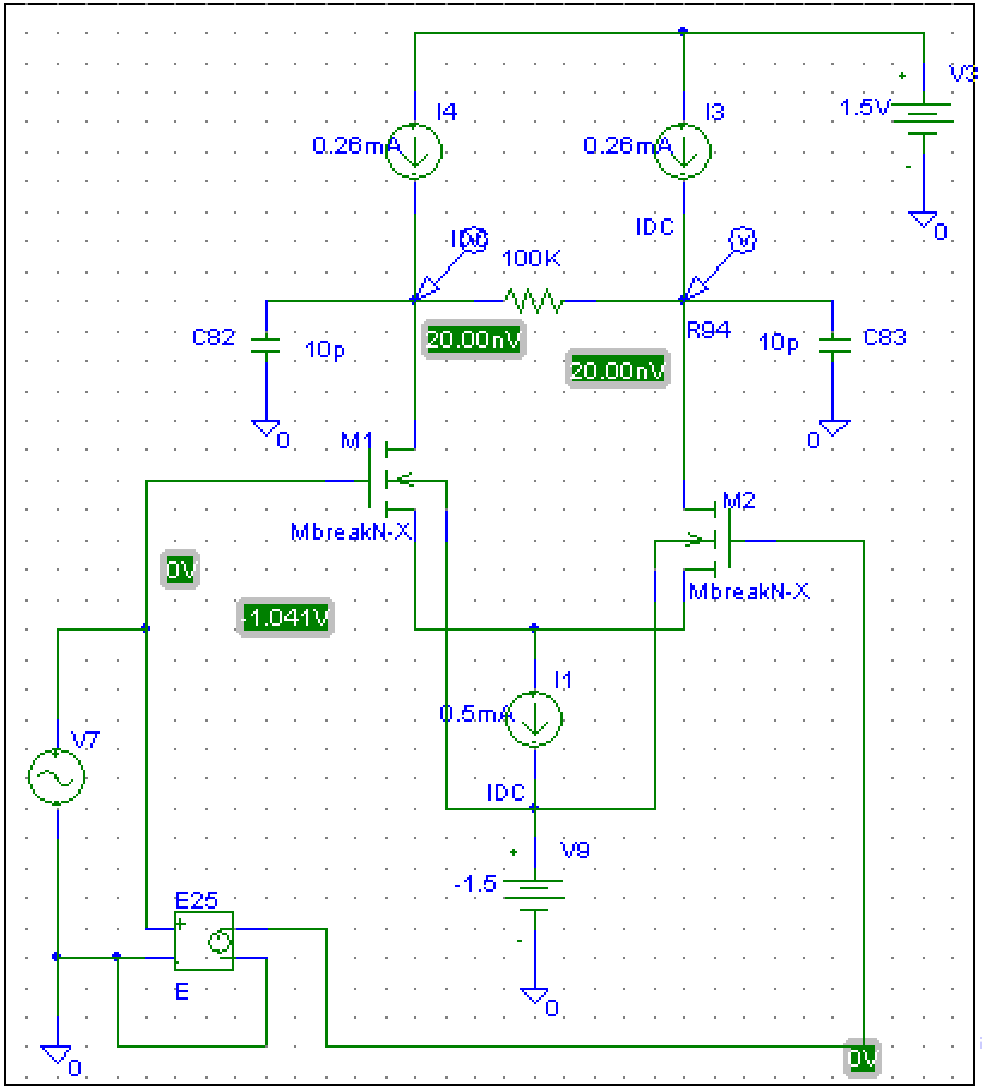
✓**THD increases**

✓**The common-mode output impedance is the parallel of the equivalent output resistance (M1 and M3) and the parasitic capacitors.**

✓**For large dc gain, the output impedance at nodes v01 and v02 are further increased and ΔIB produces a dc offset = $R_{out}\Delta IB$.**
Large common-mode offsets!

✓**How can this issue be fixed?**

Fully-Differential Amplifiers: Characterization

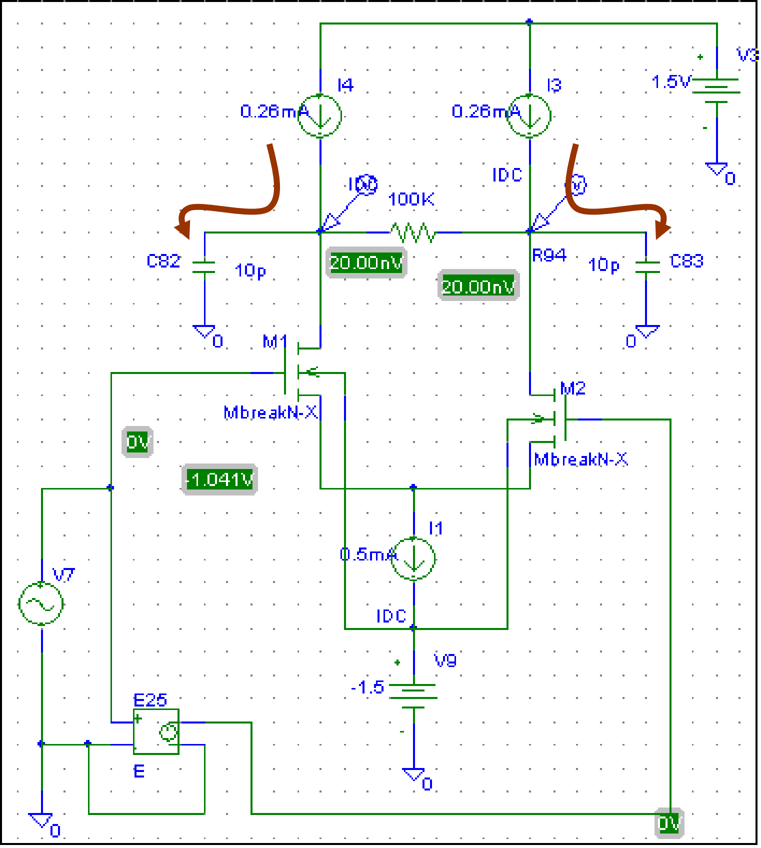


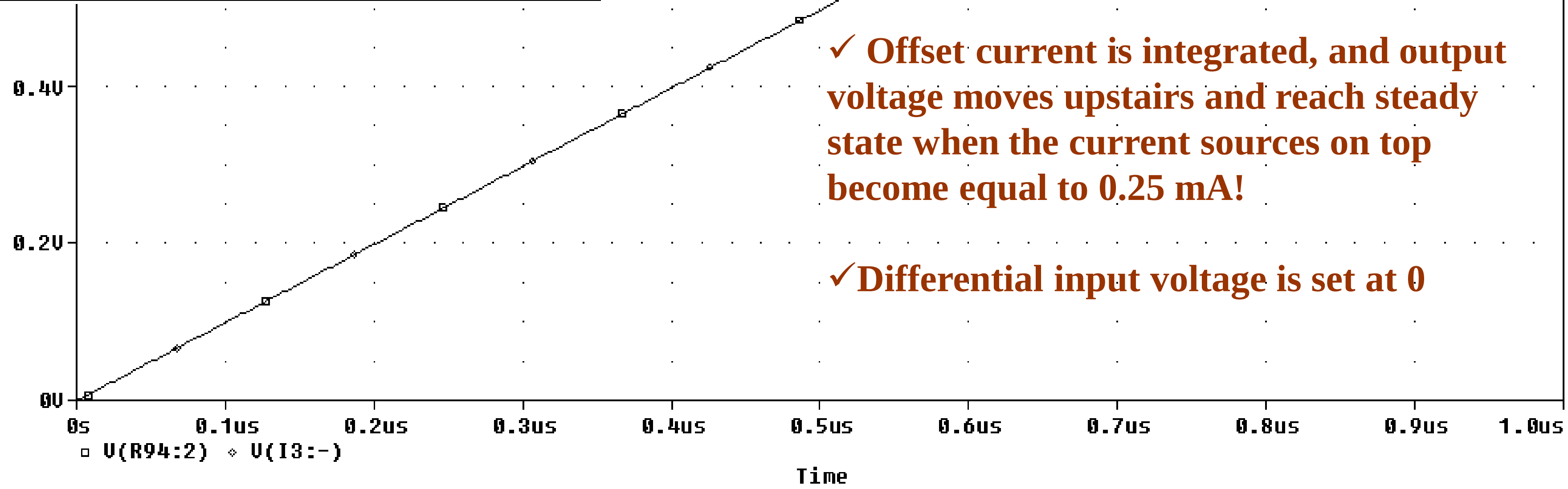
✓Common-mode current offset of 0.01 mA per side is added on purpose

Tail current is 0.5 mA while the current sources on top are 0.26 mA!

✓Differential input voltage is set at 0

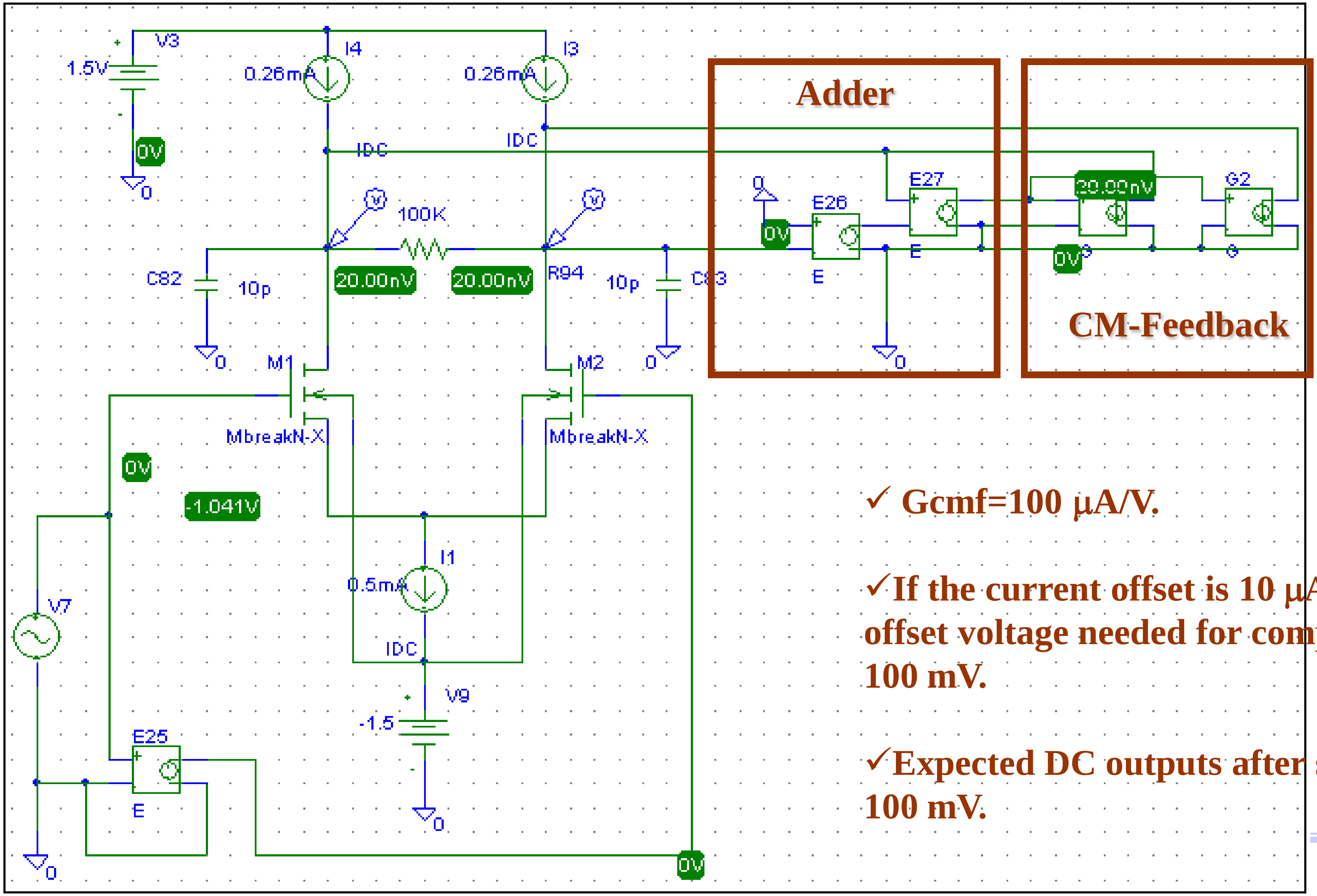
al Amplifiers: Characterization





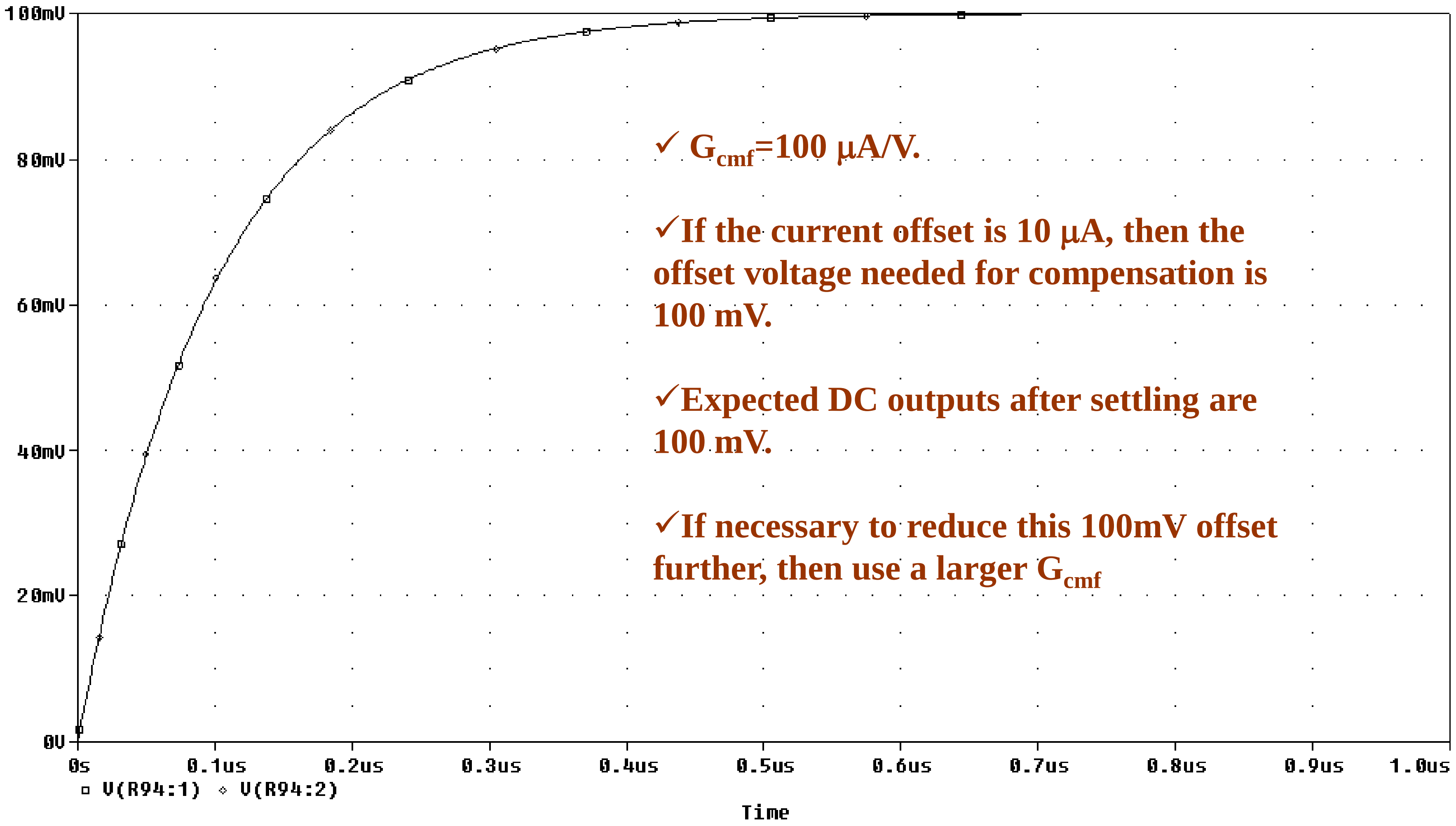
- ✓ **Offset current is integrated, and output voltage moves upstairs and reach steady state when the current sources on top become equal to 0.25 mA!**
- ✓**Differential input voltage is set at 0**

Fully-Differential Amplifiers: Common-mode Feedback



- ✓ Gcmf=100 μA/V.
- ✓If the current offset is 10 μA, then the offset voltage needed for compensation is 100 mV.
- ✓Expected DC outputs after settling are 100 mV.

Fully-Differential Amplifiers: Common-mode Feedback

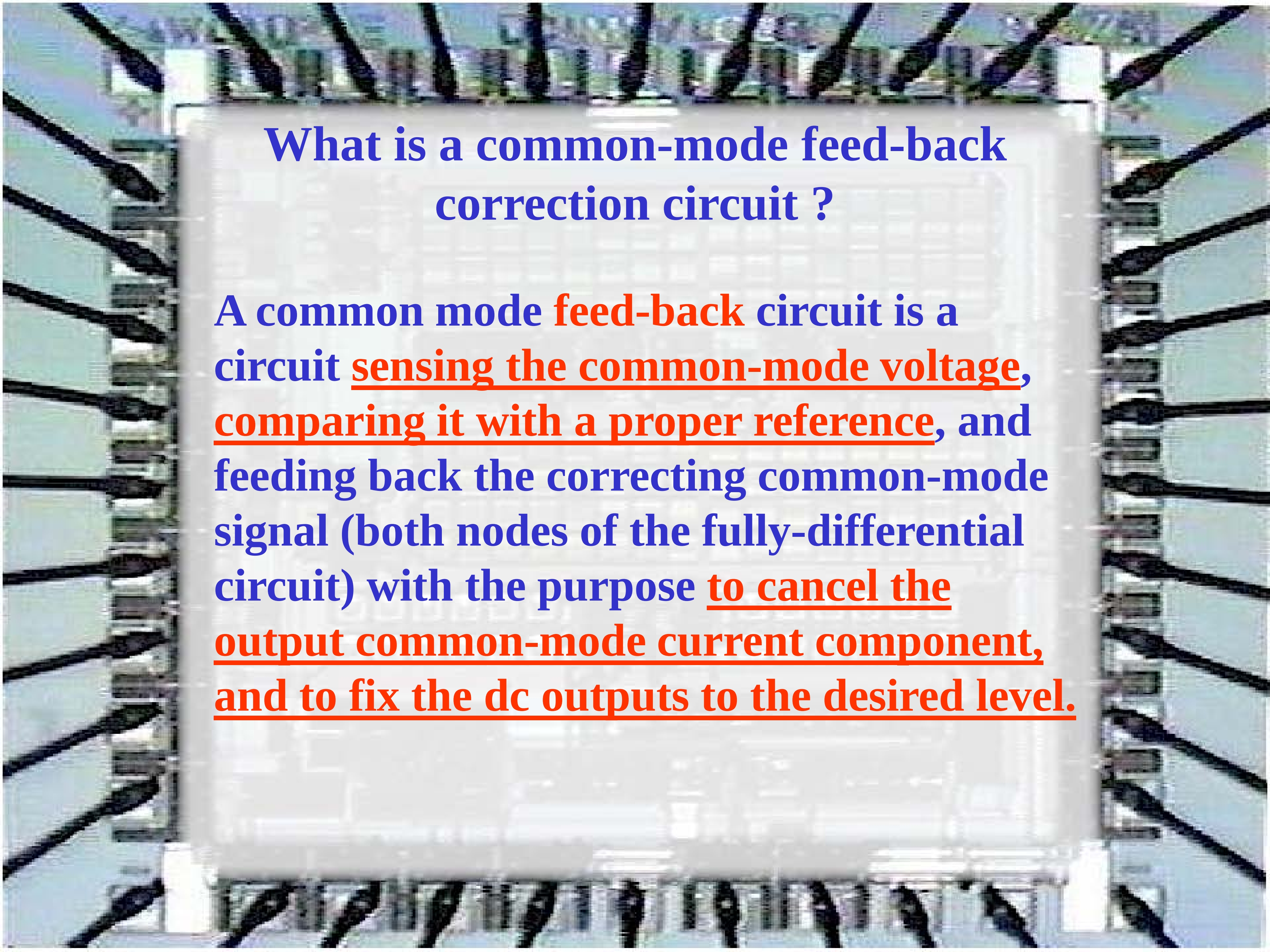


✓ G_{cmf}=100 μA/V.

✓If the current offset is 10 μA, then the offset voltage needed for compensation is 100 mV.

✓Expected DC outputs after settling are 100 mV.

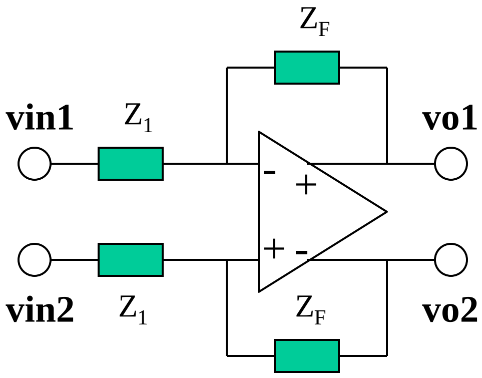
✓If necessary to reduce this 100mV offset further, then use a larger G_{cmf}



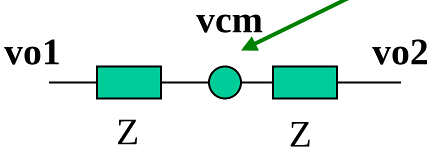
What is a common-mode feed-back correction circuit ?

A common mode feed-back circuit is a circuit sensing the common-mode voltage, comparing it with a proper reference, and feeding back the correcting common-mode signal (both nodes of the fully-differential circuit) with the purpose to cancel the output common-mode current component, and to fix the dc outputs to the desired level.

Fully-Differential Filters: CMFB Principle



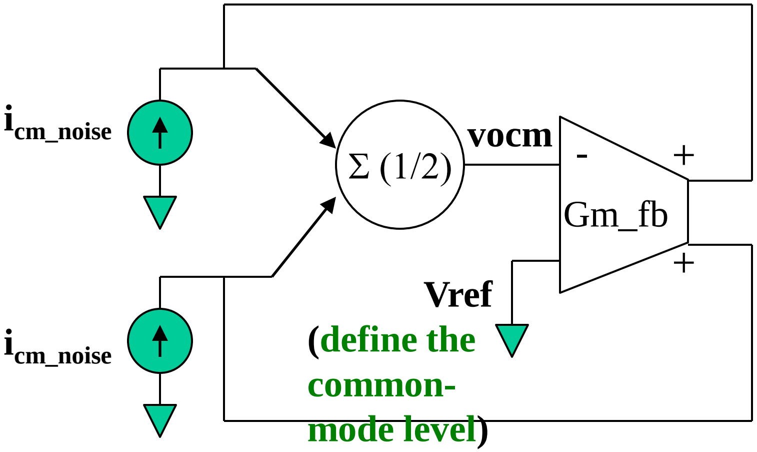
Simplest common-mode detector



$$v_{cm} = \frac{v_{01} + v_{02}}{2}$$

- **A common-mode feedback loop must be used: Circuit must operate on the common-mode signals only!**
- **BASIC IDEA: CMFB is a circuit with very small impedance for the common-mode signals but transparent for the differential signals.**
- **Use a common-mode detector (eliminates the effect of differential signals and detect common-mode signals)**
- **Analyze the common-mode feedback loop: Large transconductance gain and enough phase margin**
- **Minimum power consumption**

CMFB Principles: Analysis of the loop for common-mode signals only

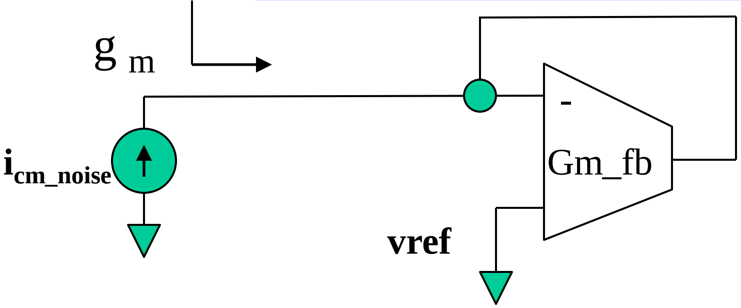


(define the common-mode level)

Effect of common-mode noise:

$$Zcm=\frac{1}{g_m}$$

$$v_{cm\_noise} = i_{cm\_noise}/G_{m\text{-}fb}$$



- Analysis for common-mode noise; for instance noise due to power supplies:
- io1=io2=icm_noise

- **The two outputs can be connected together for the analysis of the CMFB loop!**

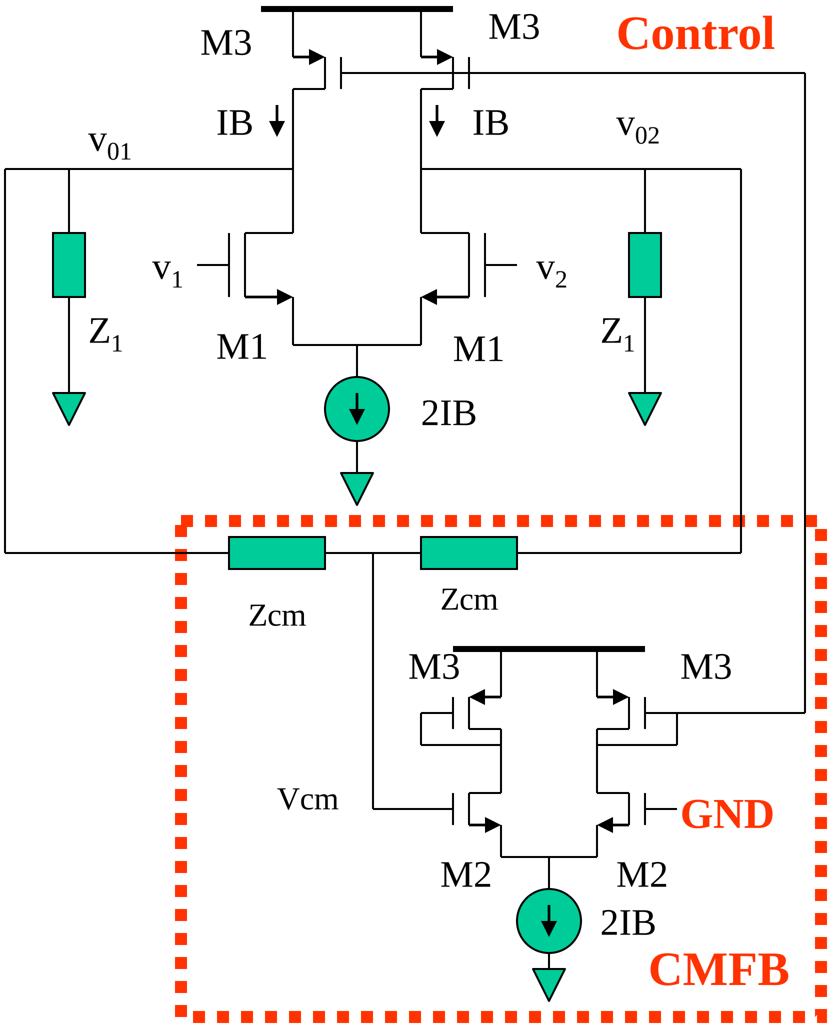
- **BASIC CONCEPTS:**

- The common-mode input noise is converted into a common-mode voltage (common-mode voltage noise) by the common-mode transconductance of the CMFB =1/Gm_fb.

- **common-mode voltage variations $v_{cm\_noise}=i_{cm\_noise}/G_{m\_fb}$!!**

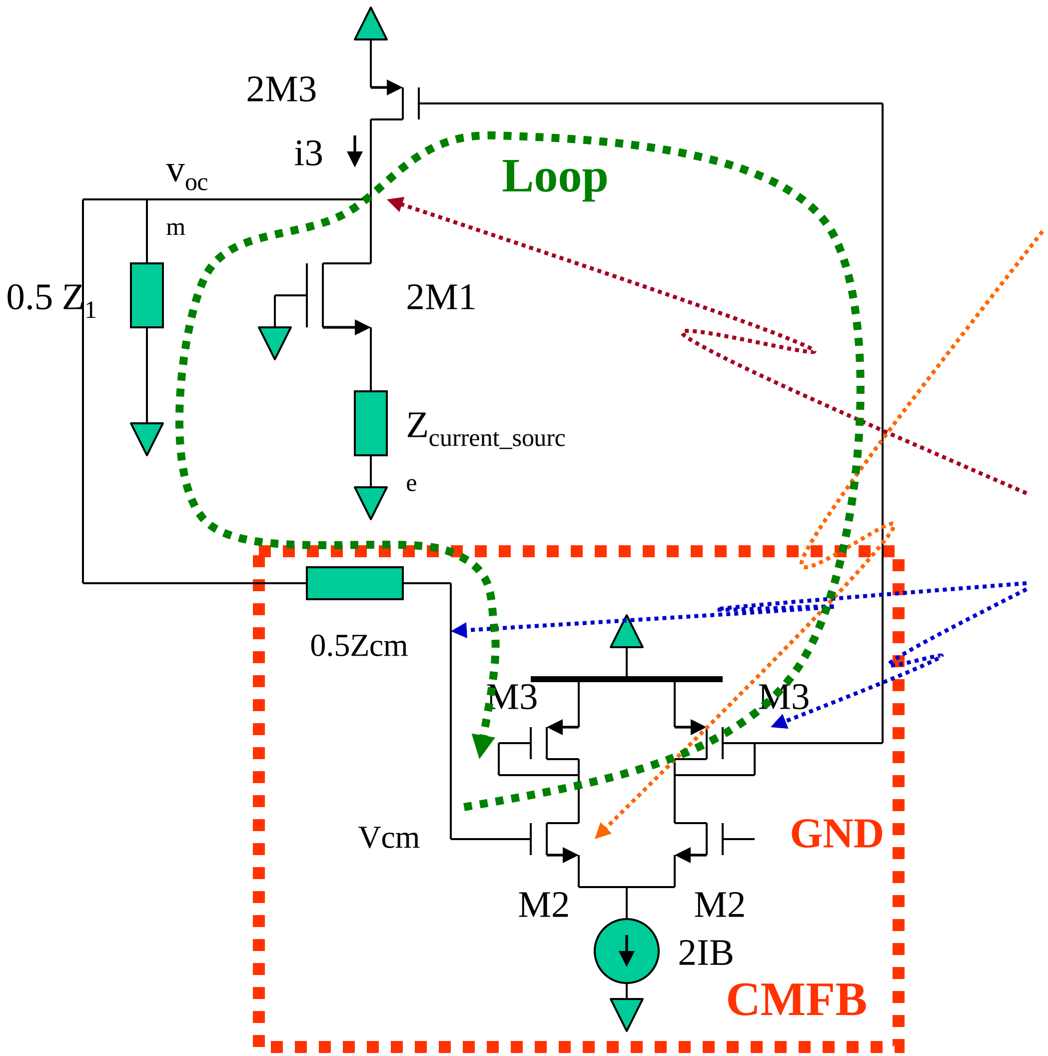
- **The larger Gm_fb the smaller the effects of the common-mode noise!**

Fully-Differential Filters: CMFB



- ➢**CMFB Characteristics:**
- ➢Transconductance gain=$g_{m2}/2$ (no PMOS mirror in CMFB OTA)
- ➢dominant pole at the output
- ➢At least 2 additional poles in the loop
- ➢Zcm reduces the OTA dc gain, affecting the differential gain
- ➢NOTE THAT Vcm IS FORCED TO BE AROUND THE GROUND LEVEL.
- ➢**DC OFFSET VOLTAGE IS AROUND 2*Ioff/gm2**

Fully-Differential Filters: CMFB

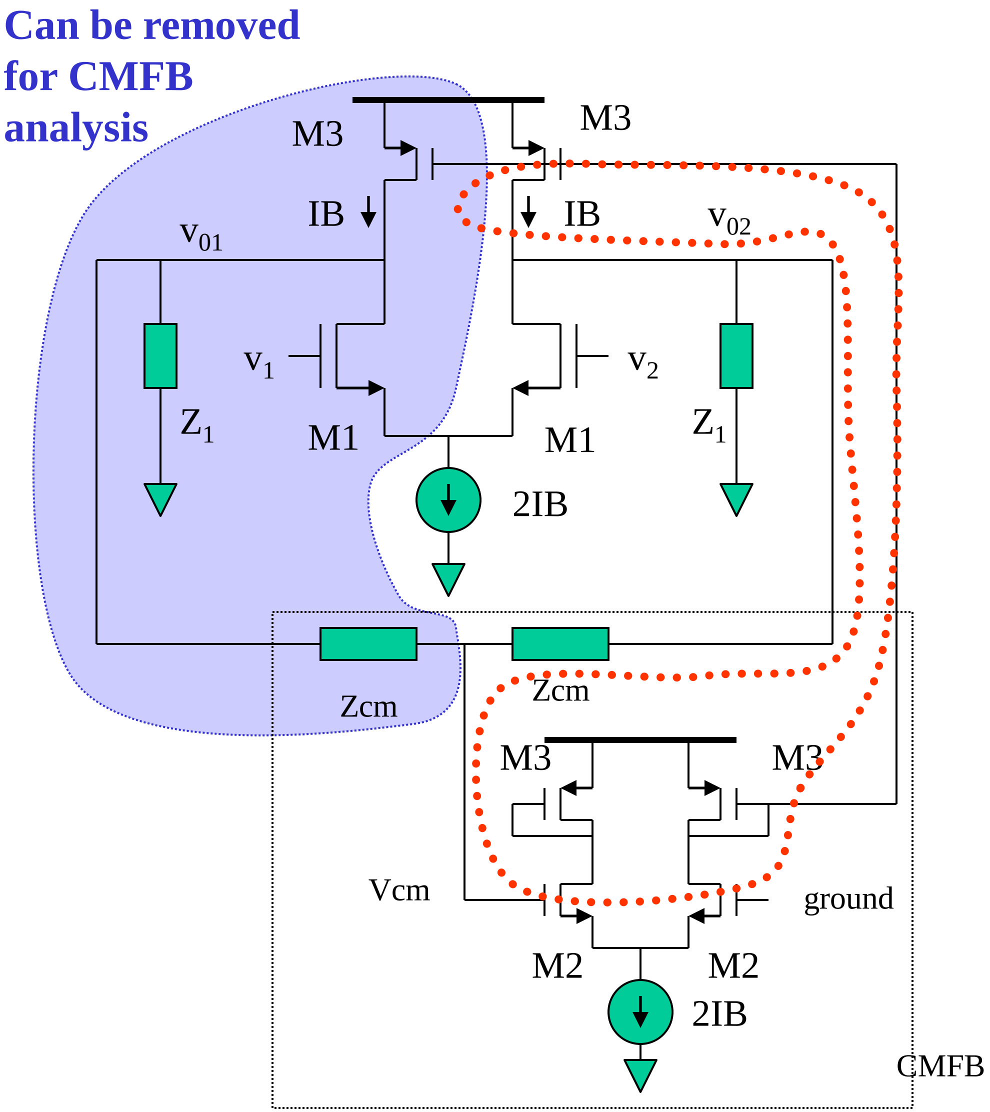


- **CMFB Characteristics:**
- DC Transconductance gain=$g_{m2}/2$
- Loop gain (ignoring poles)

$$\approx\left(\frac{g_{m2}}{2}\right)\left(\frac{1}{g_{m3}}\right)\left(-2g_{m3}\right)\left(\frac{Z_1}{2}\right)=-\frac{g_{m2}Z_1}{2}$$

- dominant pole at the output
- At least 2 additional poles in the loop
- **DC OFFSET IS AROUND 2Ioff/gm2**

Fully-Differential Filters: CMFB Principles

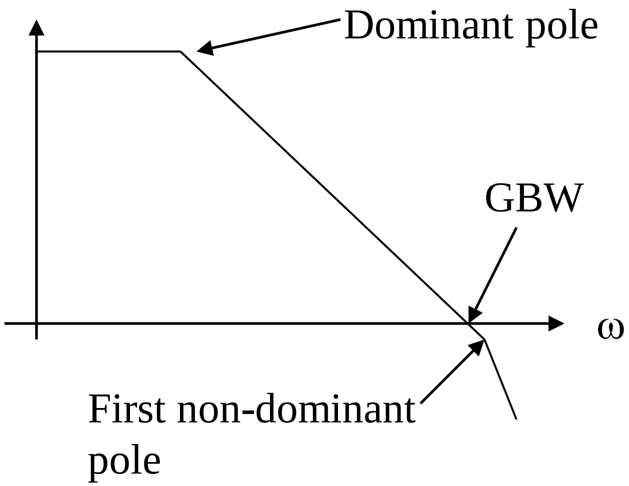


Can be removed for CMFB analysis

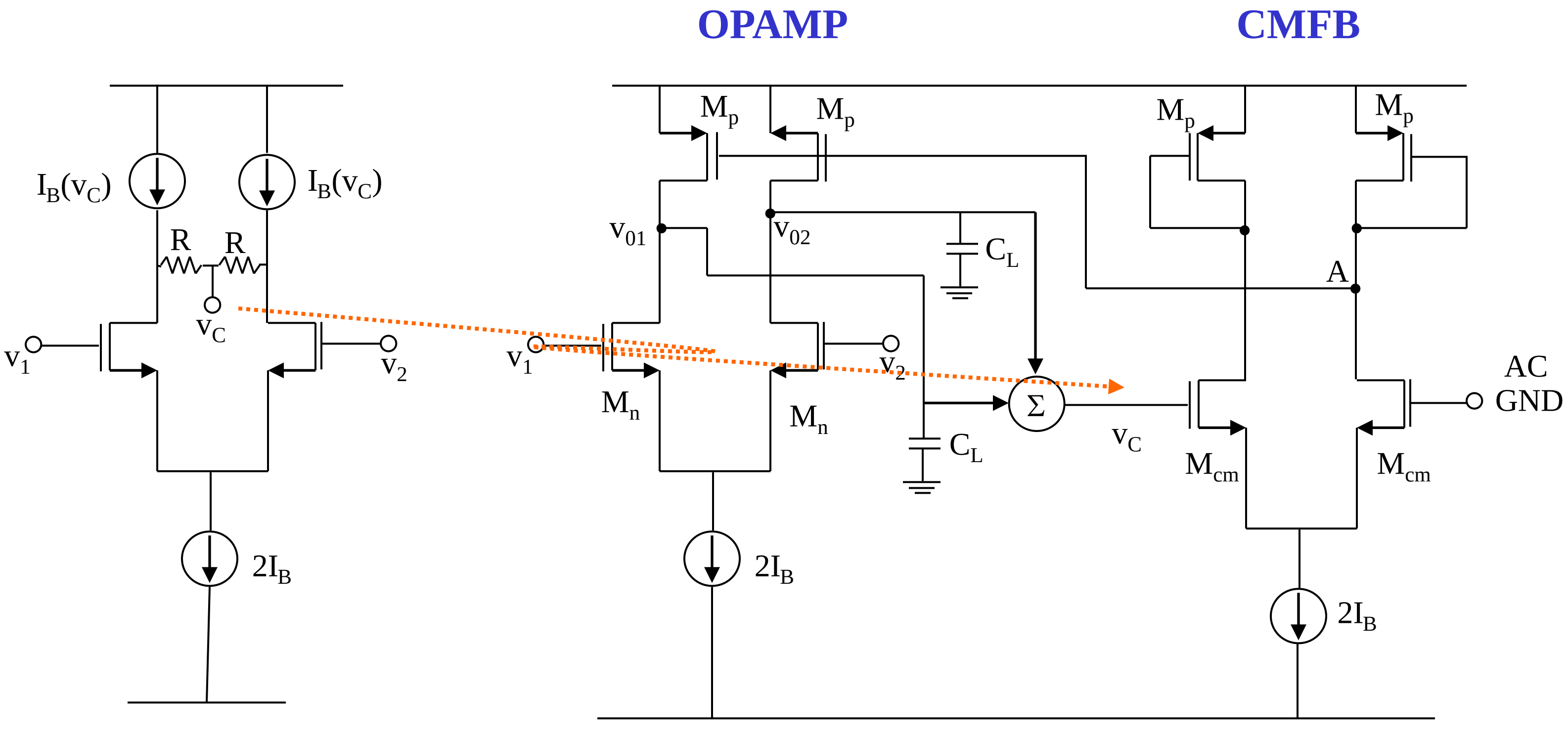
- **Common-mode stability: DC gain and most relevant poles**

- 1 pole at vcm (1/RC)
- 1 pole at gate of M3 (g_{m3}/C_{P3})
- 1 pole at the output (g_{01}/C_1)

- **dc gain = 0.5 $g_{m2}R_{01}$**



Be sure phase margin > 45º

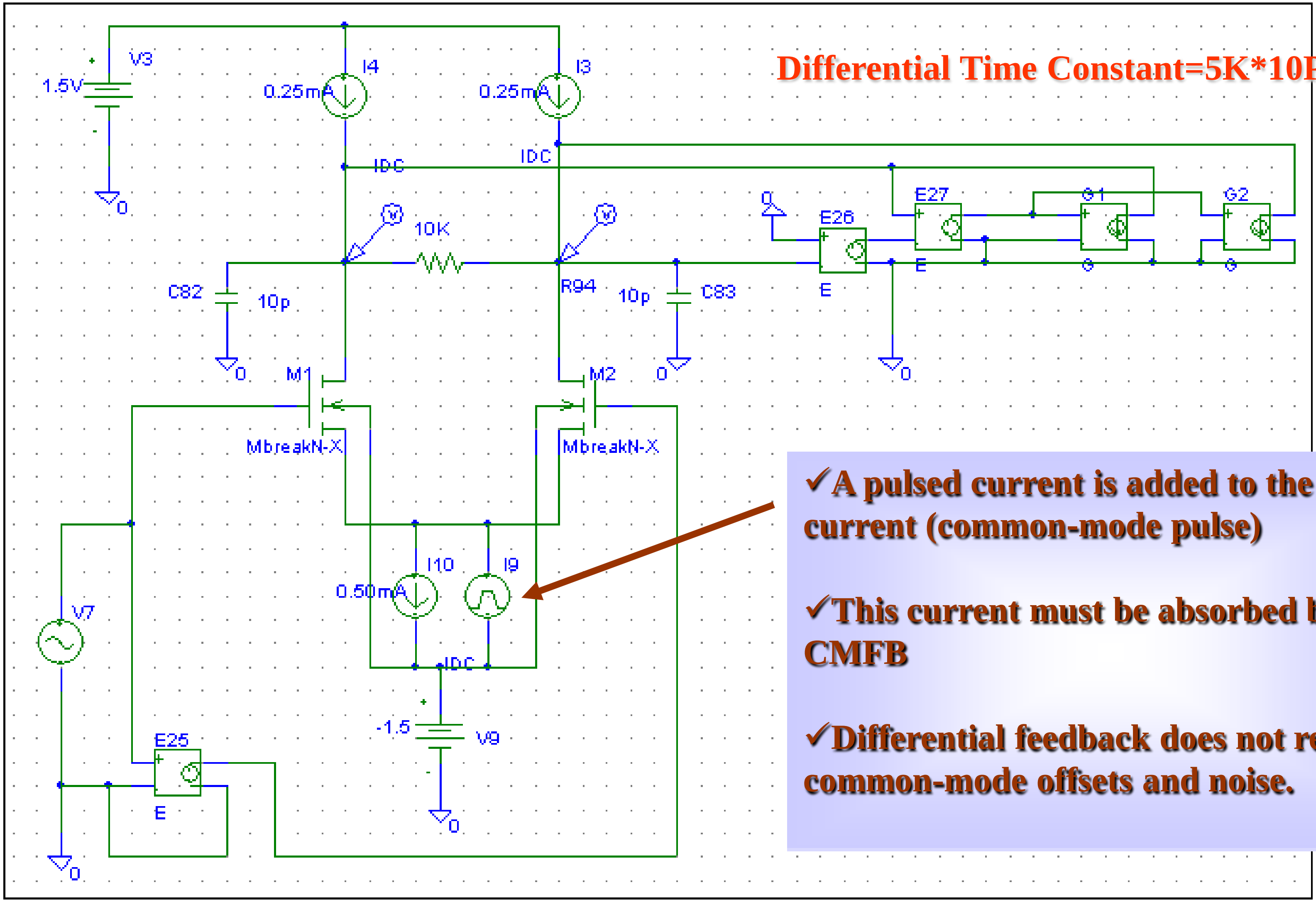


(a) (b)

Fig. 3 Common-mode feedback basic circuit concept. (a) Basic common-mode detector, (b) A CMOS CMFB Implementation.

Notice that the resistors R reduce the differential gain!

Fully-Differential Amplifiers: Common-mode pulse



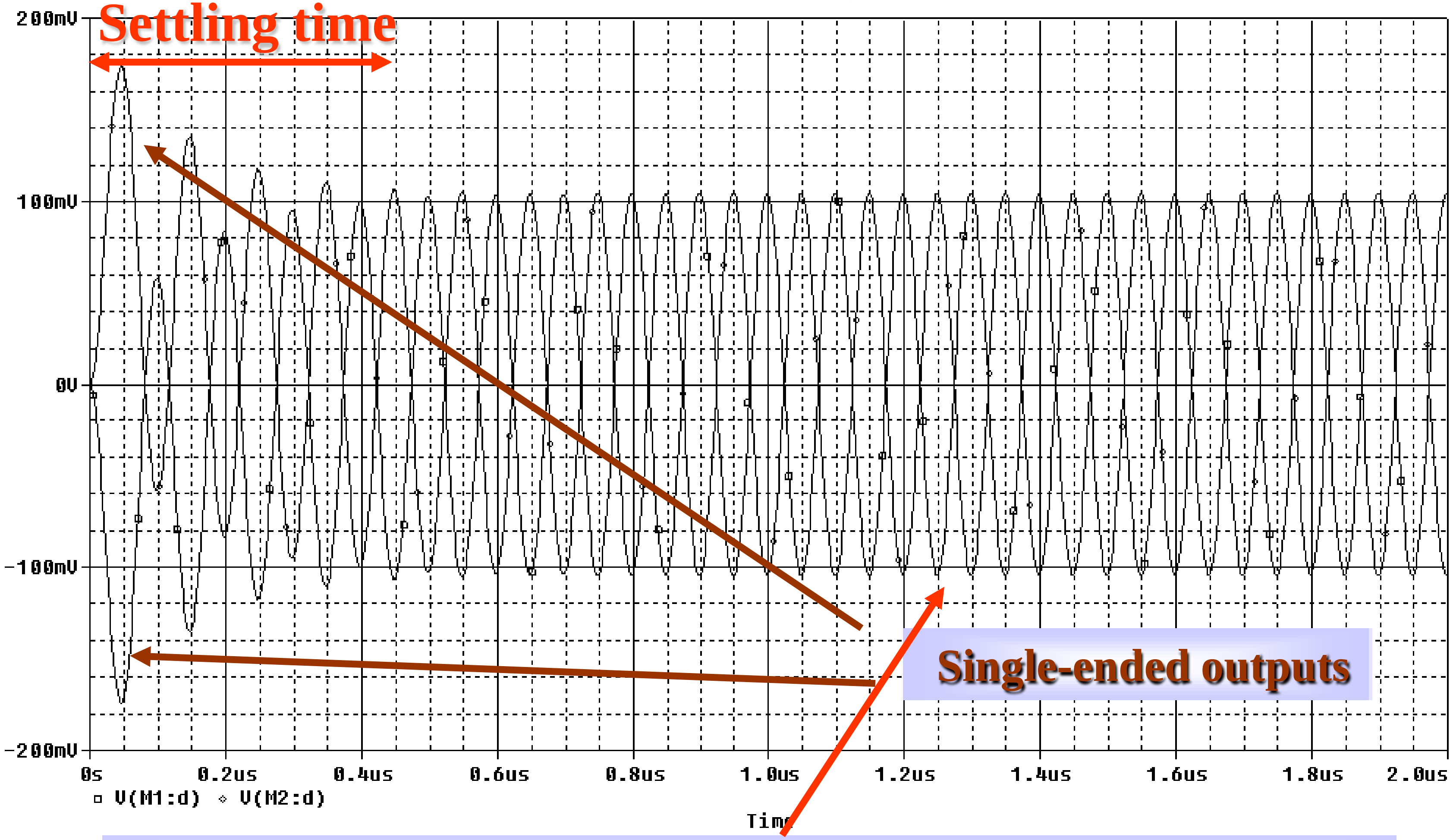
Differential Time Constant=5K*10P=50nsecs

✓A pulsed current is added to the tail current (common-mode pulse)

✓This current must be absorbed by the CMFB

✓Differential feedback does not reduce common-mode offsets and noise.

Fully-Differential Amplifiers with CMFB
Differential input signals only



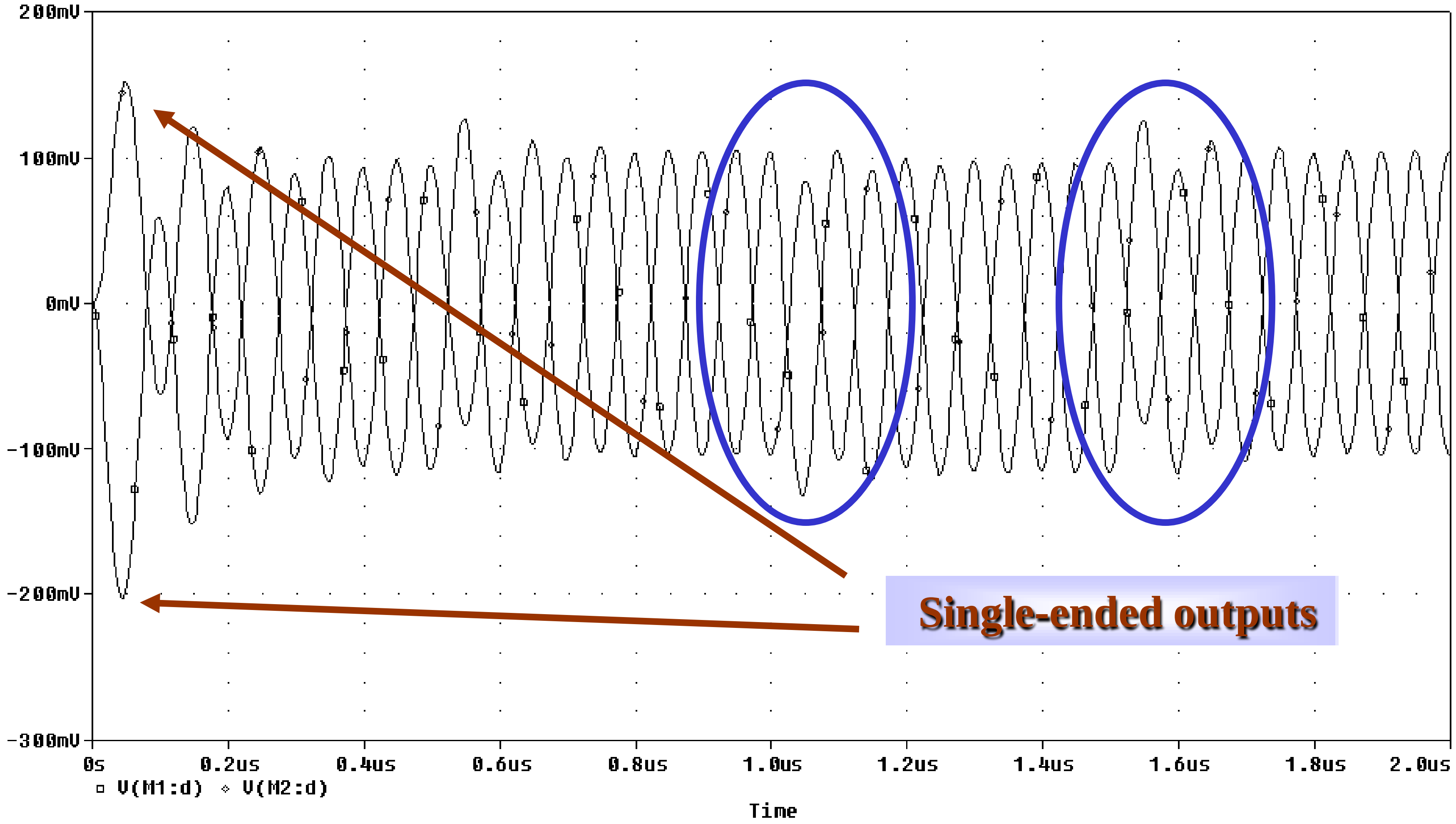
Settling time

Single-ended outputs

Seems to be that the system is working fine, isn't it?

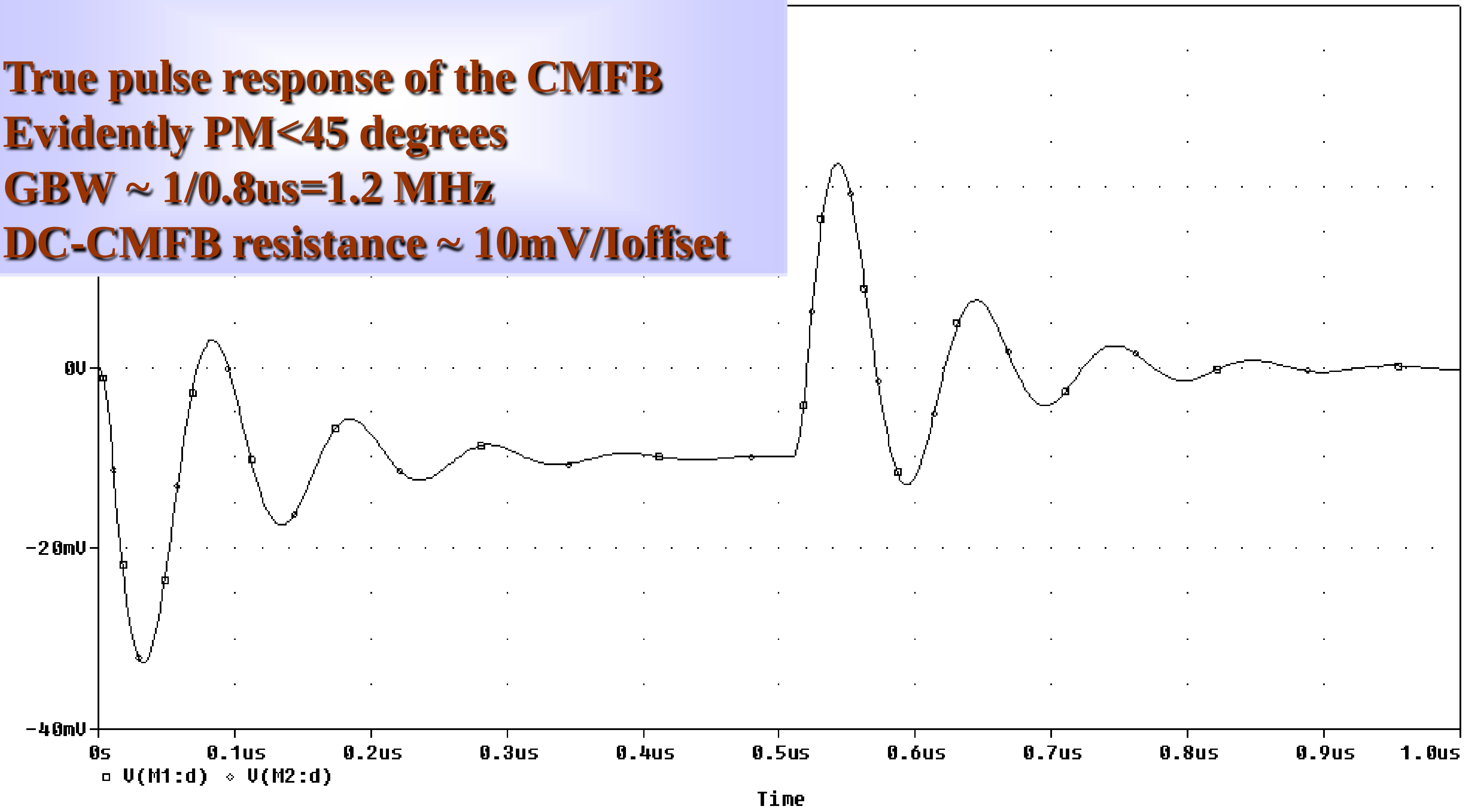
Fully-Differential Amplifiers with CMFB

Differential input signals + common-mode pulses



Single-ended outputs

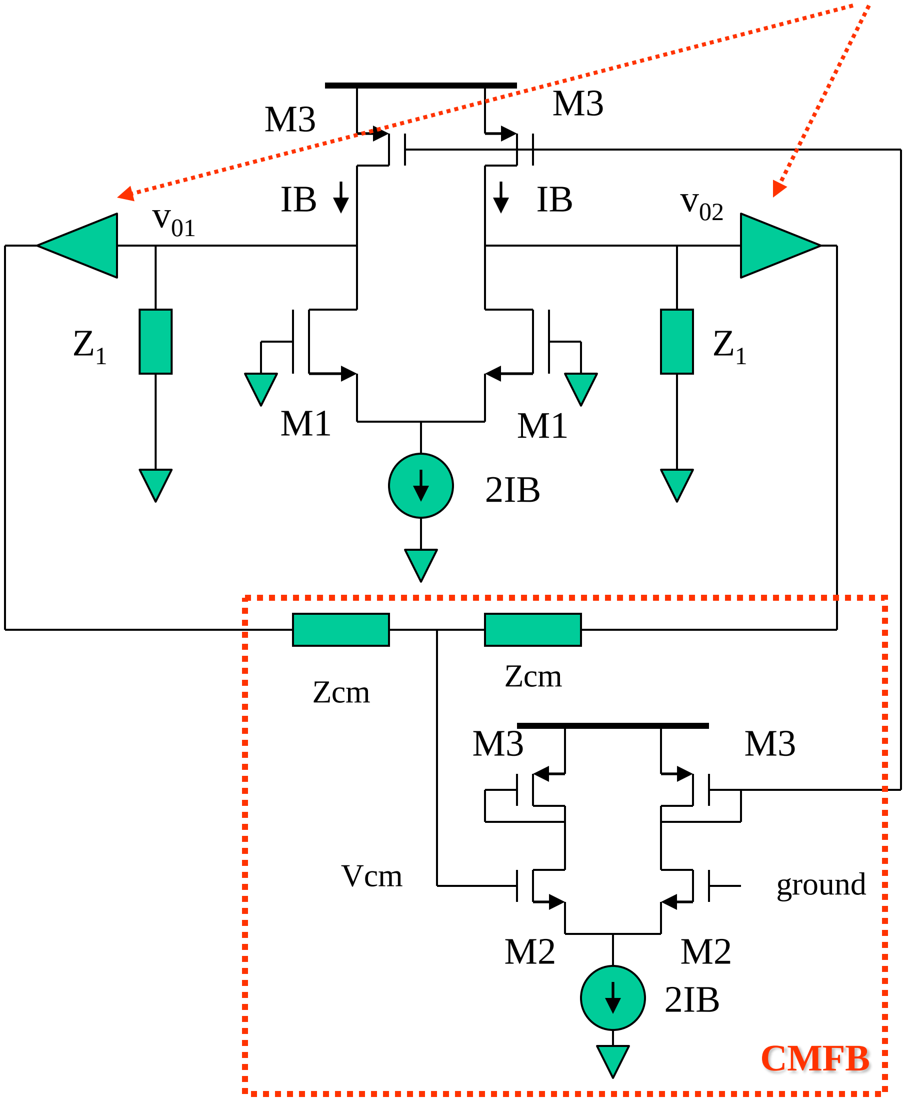
Fully-Differential Amplifiers with CMFB
Differential input signals + common-mode pulses



Common-mode output

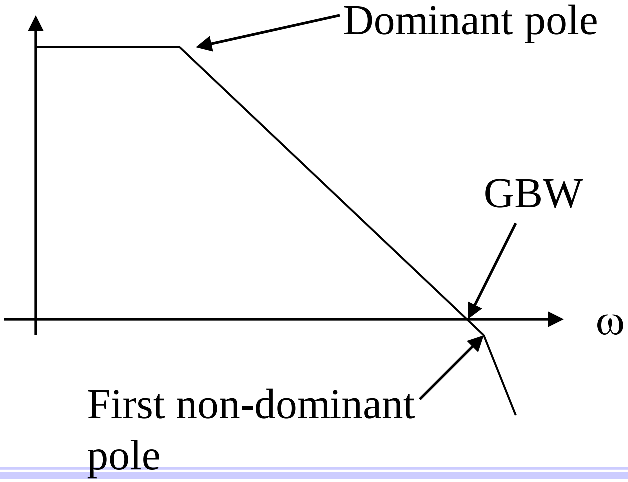
True pulse response of the CMFB
Evidently PM<45 degrees
GBW ~ 1/0.8us=1.2 MHz
DC-CMFB resistance ~ 10mV/Ioffset

Fully-Differential Filters: Adding buffers to handle the resistive CM-detector

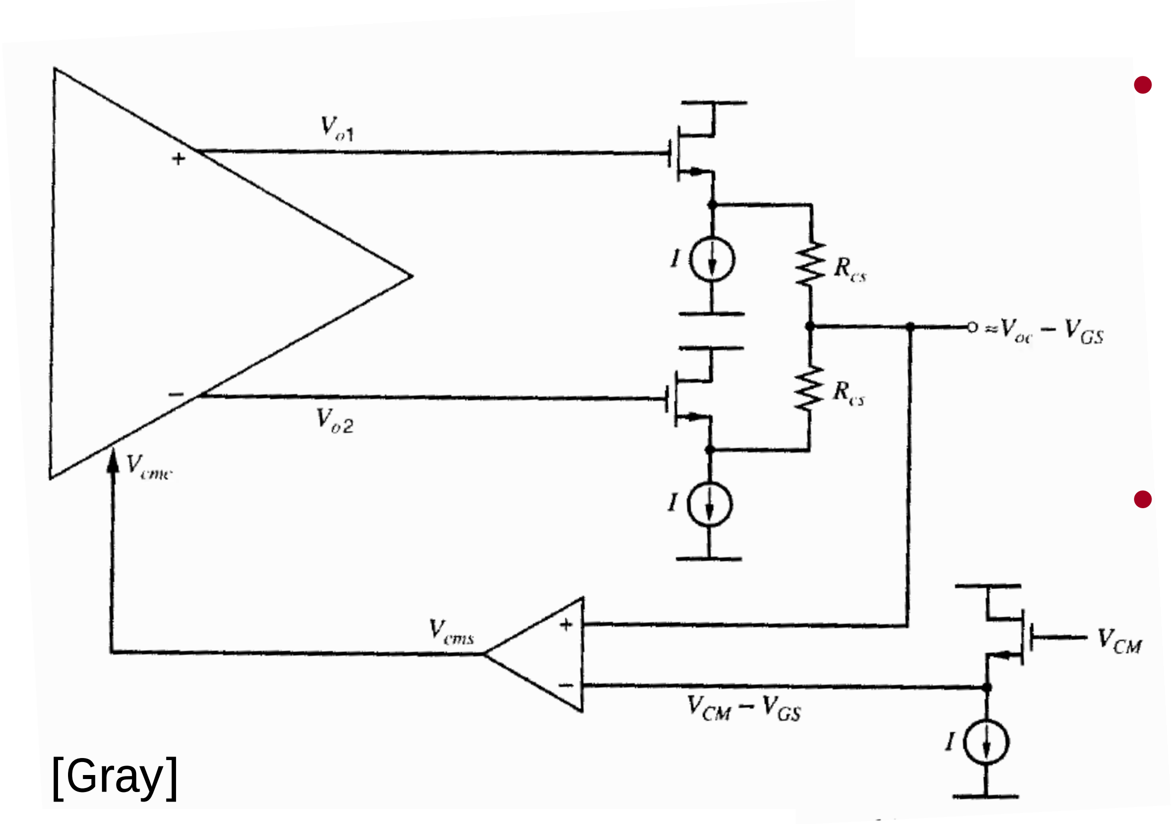


- ➢**The stability conditions are exactly the same for OTA's and OPAMP's:**

- ➢1 pole at vcm (1/RC)
- ➢1 pole at gate of M3 (g_{m3}/C_{P3})
- ➢1 pole at the output (g_{01}/C_1)
- ➢**In OPAMP's you can use resistors as common-mode detector due to the presence of the output buffers**
- ➢dc gain = $0.5g_{m2}R_{01}$



Isolated Common-Mode Sensing



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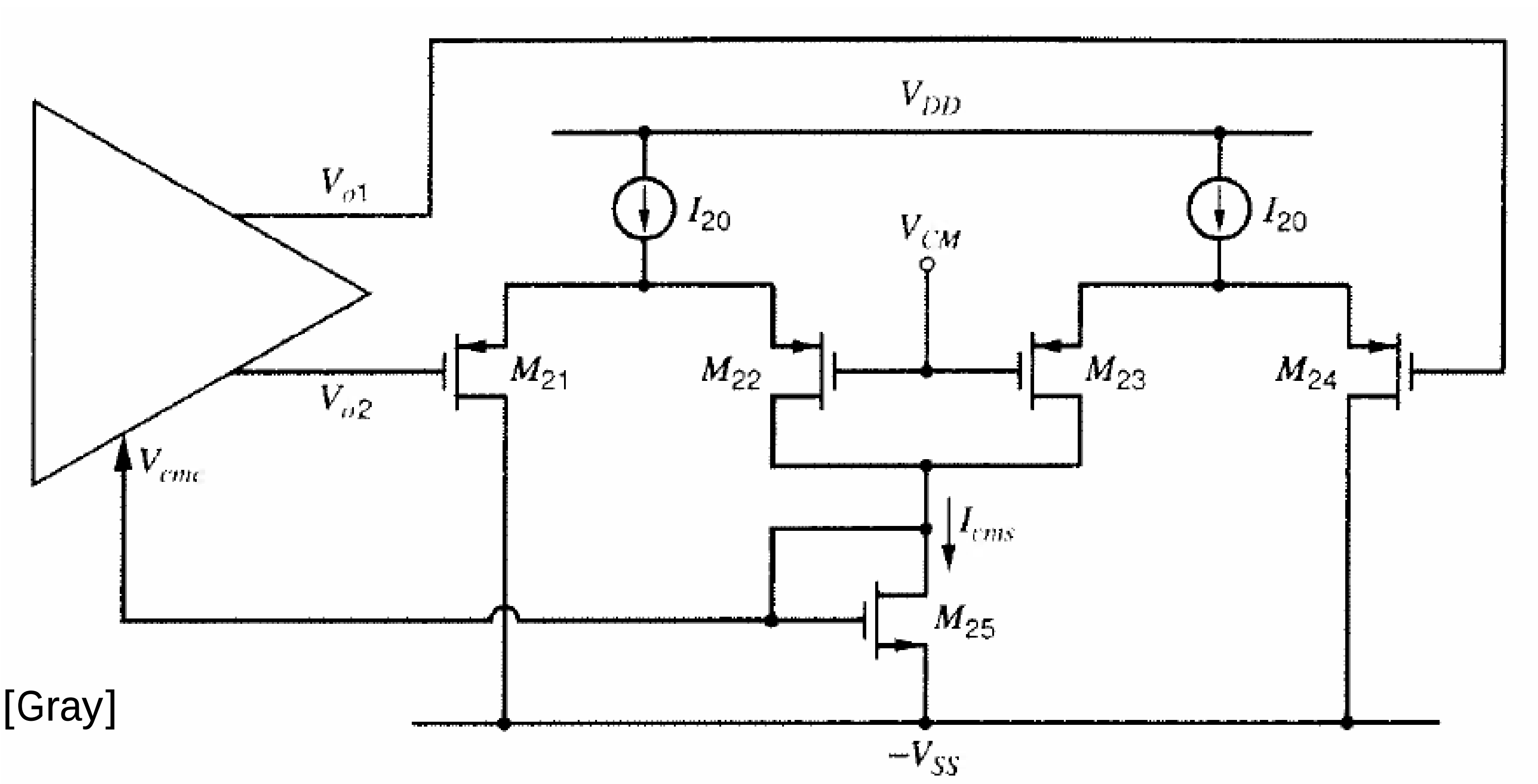
- Source-Followers isolate the loading of the common-mode sensor resistors
- Need to have a replica source follower to set the appropriate reference level for the CMFB amplifier

Two Differential Pair CM Sensor



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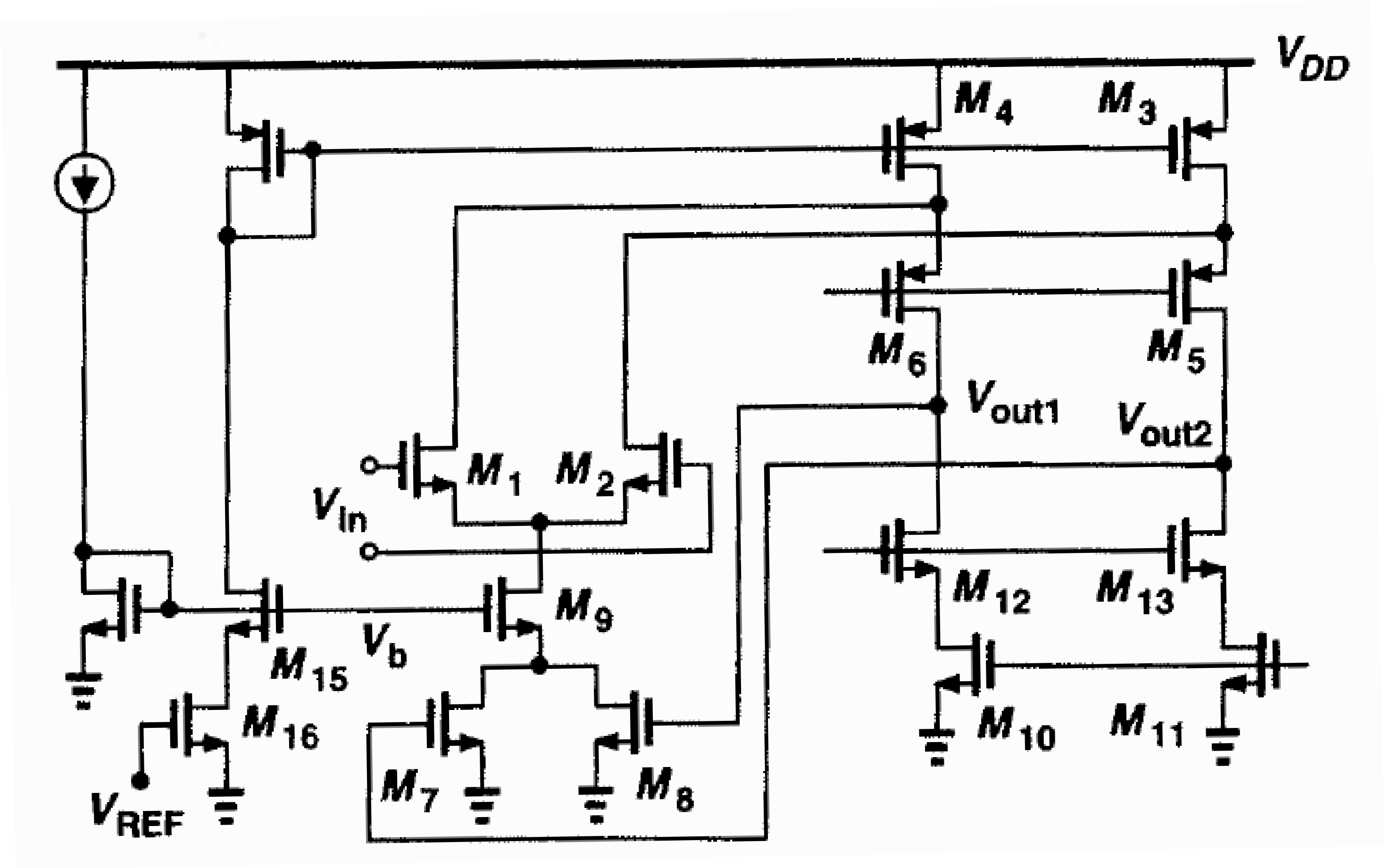
$$I_{cms} = I_{20} + g_{m22}(V_{oc} - V_{CM})$$

$$G_{cmf} = g_{m22}$$

CMFB w/ Triode Devices in Tail Current Source

[Razavi]



Next Time

- OTA CMFB Examples

- Output Stages