ECEN474: (Analog) VLSI Circuit Design
Fall 2012

Lecture 8: Current Mirrors

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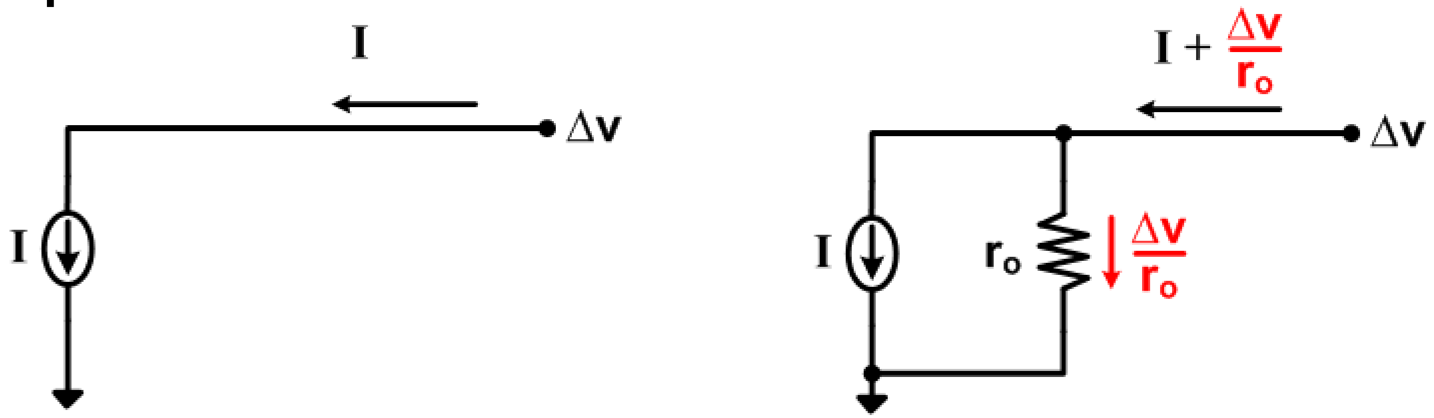
Announcements & Agenda

- HW2 due Monday
- Reading
  - Razavi Chapter 5
- Biasing in ICs
- Simple Current Mirror
- Transistor Small-Signal Impedances
  - Simple Amplifiers
- Other Current Mirror Topologies

Current Source Properties

- Output Resistance



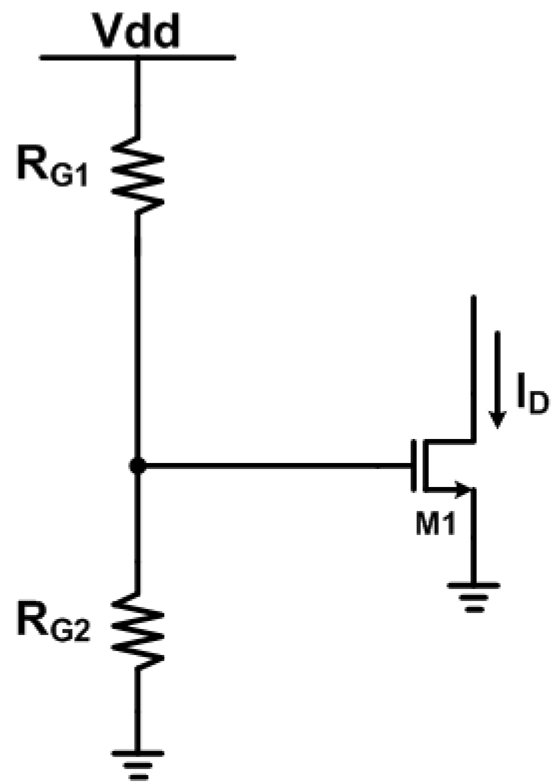
  - Finite output resistance degrades current source accuracy and amplifier gain
- Other important properties:
  - Voltage headroom (compliance voltage)
  - Accuracy
  - Noise

How Should We Bias Our Circuits?

- Resistive Biasing
  - Assuming saturation

$$I_D = \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(V_G - V_{Tn}\right)^2$$

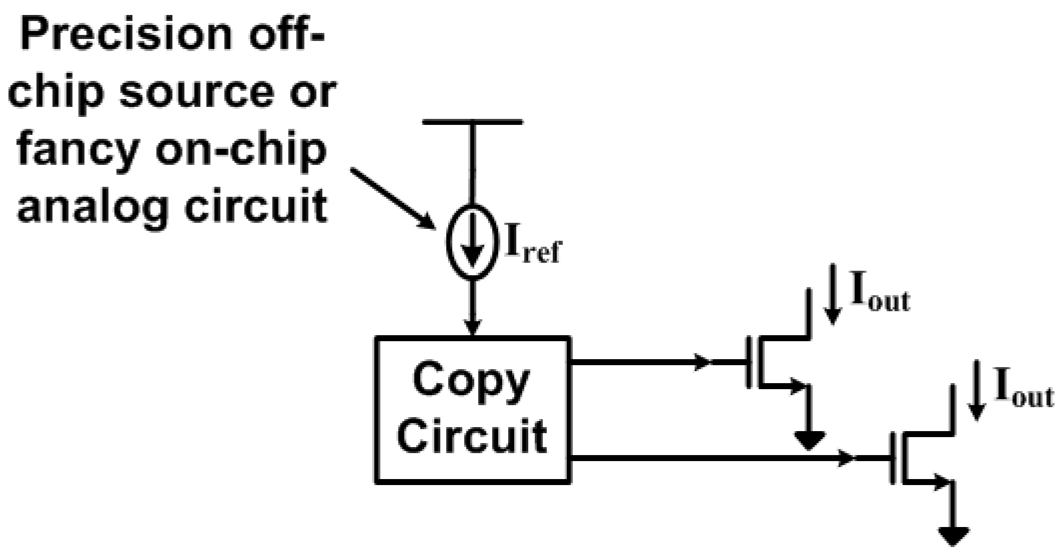
$$= \frac{1}{2}\mu_n C_{ox}\frac{W}{L}\left(\frac{R_{G2}}{R_{G1}+R_{G2}}Vdd - V_{Tn}\right)^2$$



- I_D is sensitive to
  - Supply (Vdd)
  - Process (V_{Tn} and $\mu_n C_{ox} W/L$)
  - Temperature (V_{Tn} and μ_n)

IC Biasing

- In IC design we often assume that we have **one** precise current source and we copy its value to our circuits



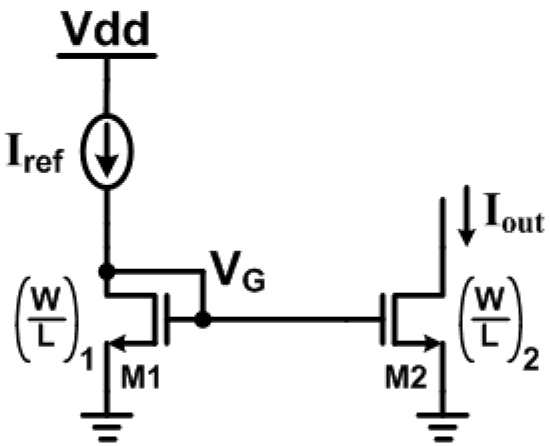
Simple Current Mirror

- That copy circuit is a current mirror
- Simple Current Mirror

What is V_G ?

$$I_D = I_{REF} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_1 (V_G - V_{Tn})^2$$

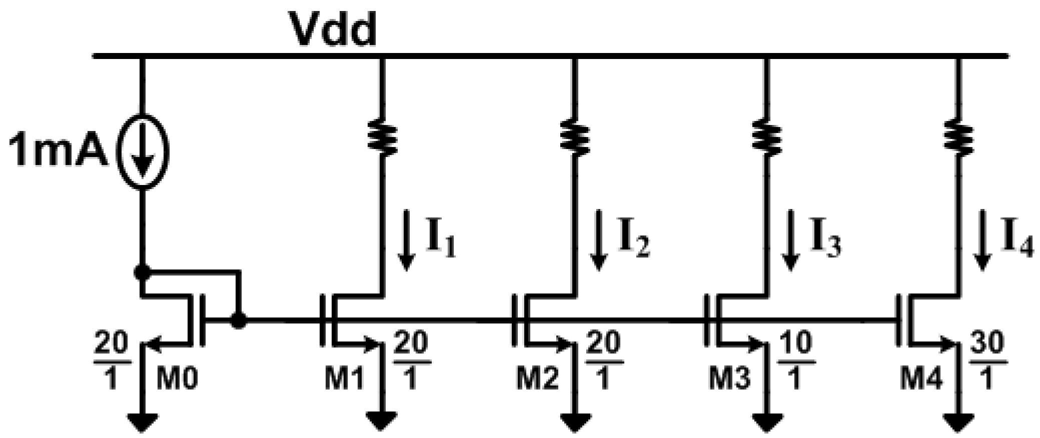
$$V_G = \sqrt{\frac{2I_{REF}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} + V_{Tn}$$



- If VG is applied to another transistor

$$I_{out} = \frac{1}{2}\mu_n C_{ox}\left(\frac{W}{L}\right)_2 \left(\sqrt{\frac{2I_{REF}}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} + V_{Tn} - V_{Tn}\right)^2 \Rightarrow \boxed{I_{out} = \frac{\left(\frac{W}{L}\right)_2}{\left(\frac{W}{L}\right)_1} I_{REF}}$$

Ideal Current Mirror Example



I_1=1mA

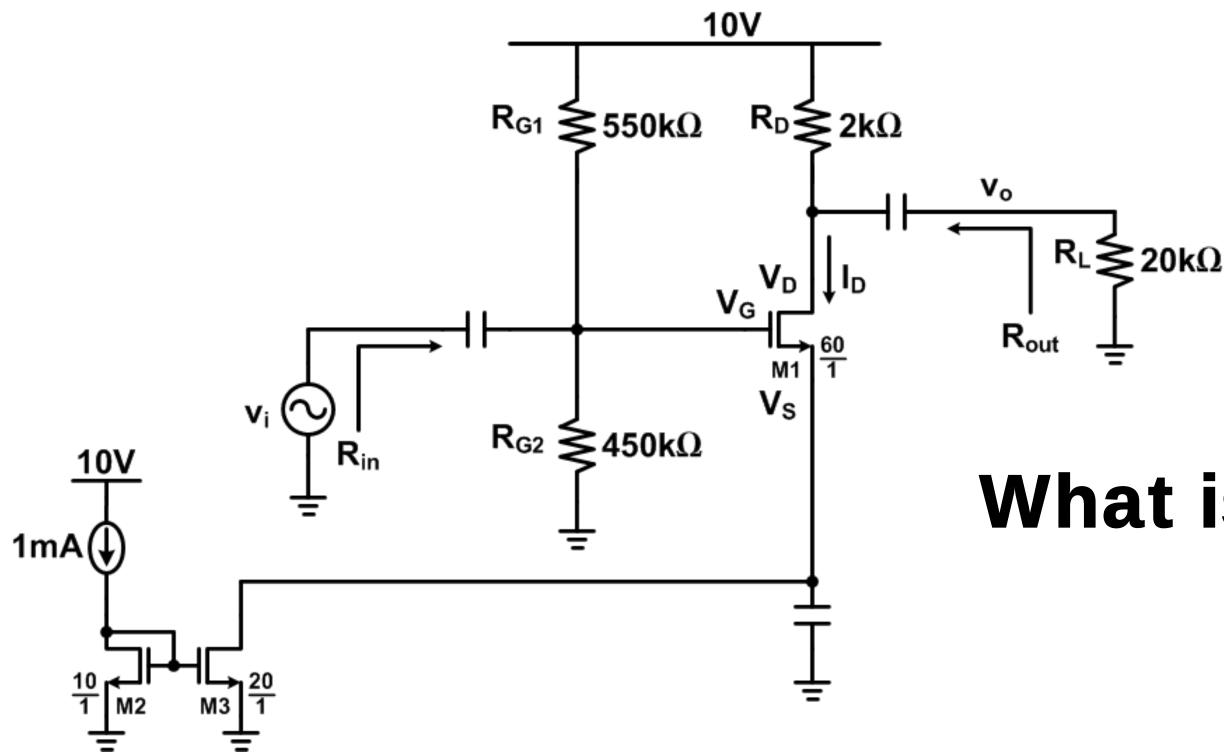
I_2=1mA

I_3=0.5mA

I_4=1.5mA

- This bias scheme reduces sensitivity to process, voltage, and temperature variations

CS Amplifier w/ Current Source

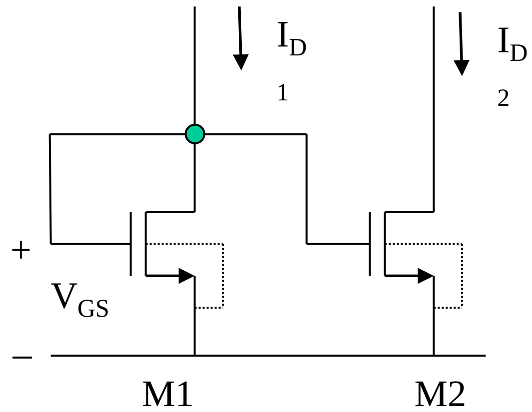


What is I_D?

- Need to insure that M3 remains in saturation

$$V_s = V_G - (V_{ov1} + V_{Tn}) = \left(\frac{R_{G2}}{R_{G1} + R_{G2}}\right) Vdd - \left(\sqrt{\frac{2I_D}{\mu_n C_{ox}\left(\frac{W}{L}\right)_1}} + V_{Tn}\right)$$

Current Mirrors: Accuracy limitations



In general $(W/L)_2=N(W/L)_1$, most probably $VT1\neq VT2$, then

$$I_{D2} = \frac{\mu_n C_{OX}}{2}\left(\frac{W}{L}\right)_2 (V_{GS} - V_T)^2 (1 + \lambda_2 V_{DS2})$$

$$I_{D2} = \frac{\frac{\mu_n C_{OX}}{2}\left(\frac{W}{L}\right)_2 (V_{GS} - V_{T2})^2 (1 + \lambda_2 V_{DS2})}{\frac{\mu_n C_{OX}}{2}\left(\frac{W}{L}\right)_1 (V_{GS} - V_{T1})^2 (1 + \lambda_1 V_{DS1})} I_{D1} = \frac{K_{P2}(V_{GS} - V_{T2})^2 (1 + \lambda_2 V_{DS2})}{K_{P1}(V_{GS} - V_{T1})^2 (1 + \lambda_1 V_{DS1})} N I_{D1}$$

$$\text{Error} \approx \lambda_2 V_{DS2} \neq \lambda_1 V_{DS1}$$

$$\text{Error} \approx K_{P2} \neq K_{P1}$$

$$\text{Error} \approx V_{T2} \neq V_{T1}$$

$$\lambda \propto \frac{1}{L}$$

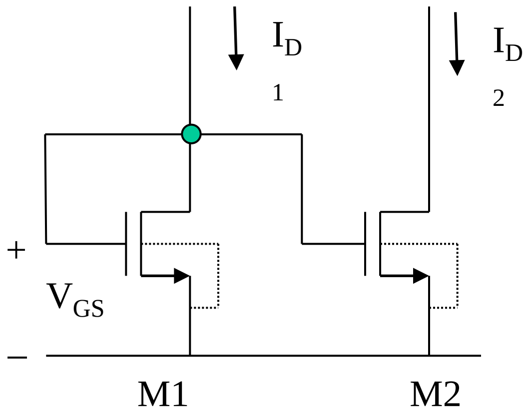
Long devices reduce the error; make VDS1=VDS2

Errors can be reduced (but not eliminated) by using replicas of the main device and good layout!

Effective mobility and threshold voltages are sensitive to V_{DS}.and Vdsat

Good solution ==> use cascode structures

DC Current Mirrors: Second-Order Effects



After good layout: Tolerances in N are in the range of 0.5-2 %. Usually mismatches are inversely proportional to gate area!

$$\frac{I_{D2}}{I_{D1}} = \frac{\mu_{n2}(V_{GS}-V_{T2})^2(1+\lambda_2 V_{DS2})}{\mu_{n1}(V_{GS}-V_{T1})^2(1+\lambda_1 V_{DS1})} N$$

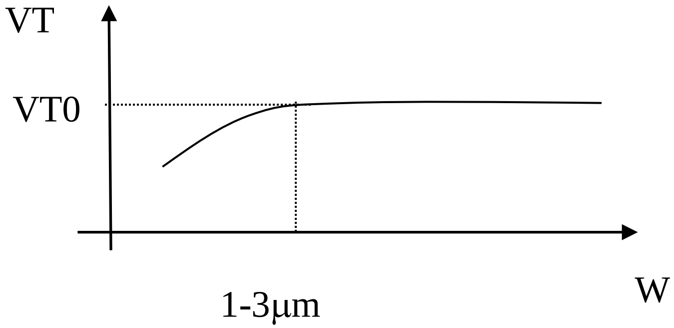
Mobility degradation

$$\text{Error} \approx \mu_2 - \mu_1 \qquad \mu = \mu_0 \frac{1}{1+\theta V_{gs}} \frac{1}{1+\frac{V_{ds}}{L\varepsilon_{crit}}}$$

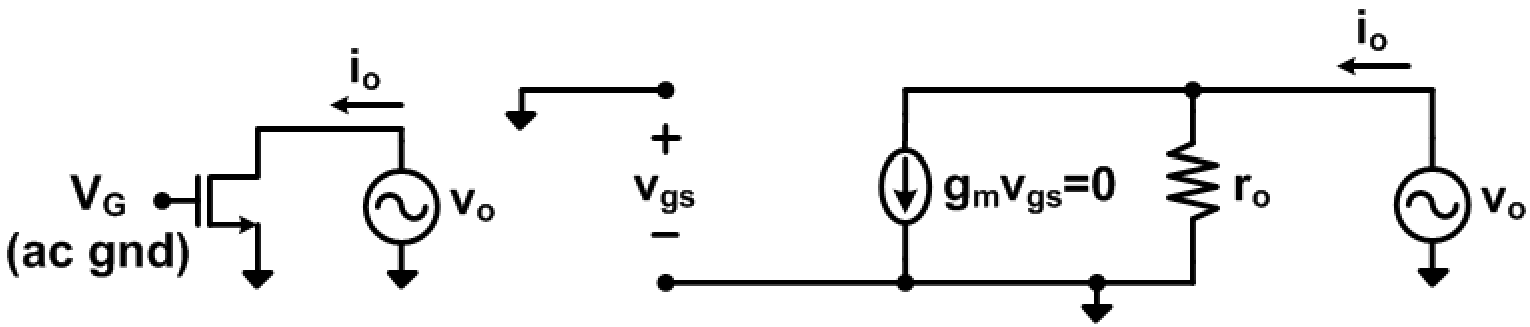
$$\text{Error} \approx V_{T2} - V_{T1}$$

Error is minimized by using replicas of the basic device

Intra-die V_T mismatches are inversely proportional to gate area!

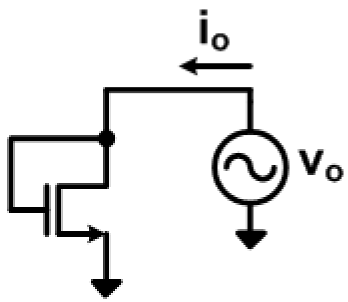


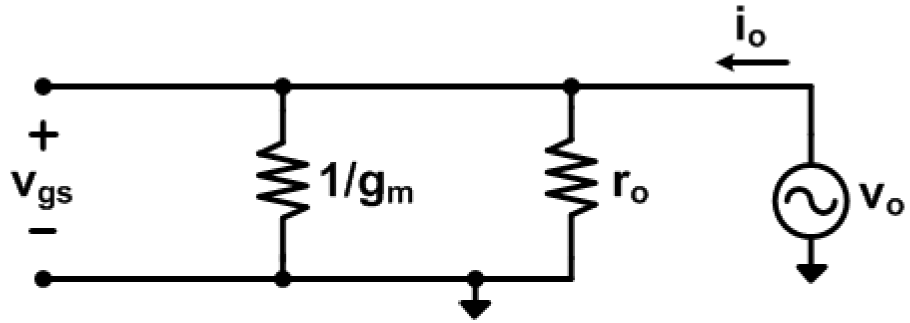
Small-Signal Impedance: Simple Current Source



$$r_{out} = \frac{1}{g_o}$$

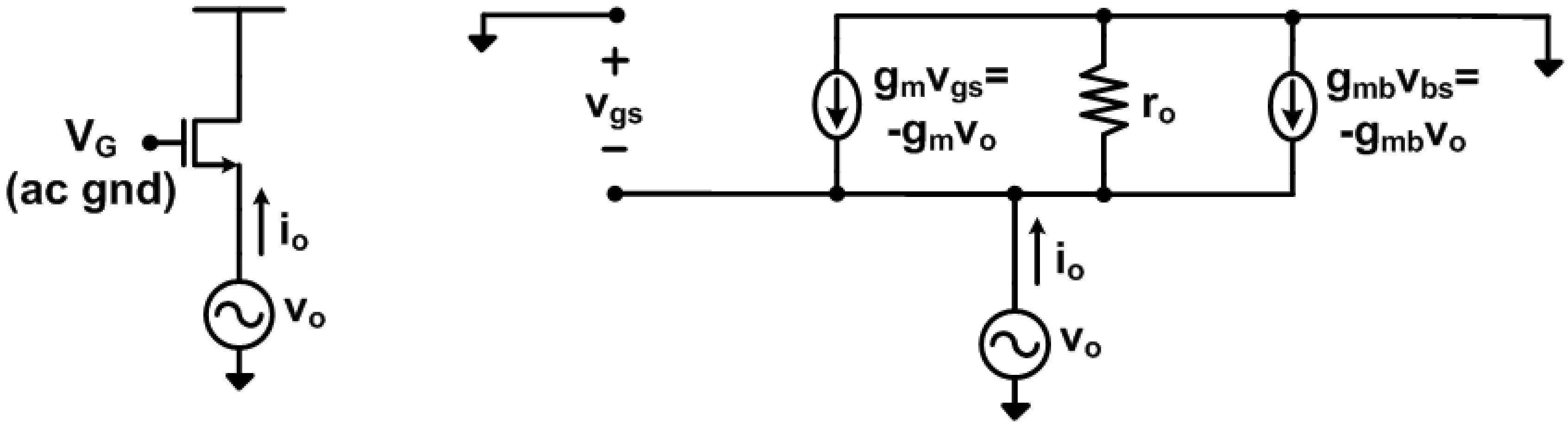
Small-Signal Impedance: "Diode" Load





$$r_{out} = \frac{1}{g_m + g_o} \approx \frac{1}{g_m}$$

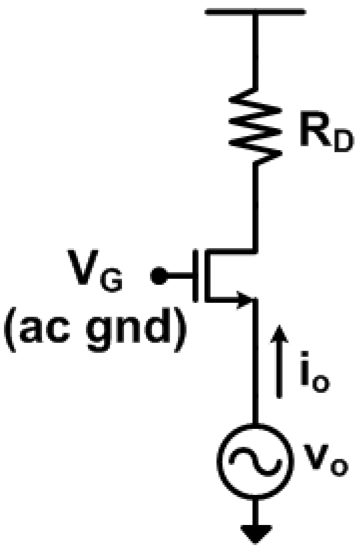
Small-Signal Impedance: Looking Into Source

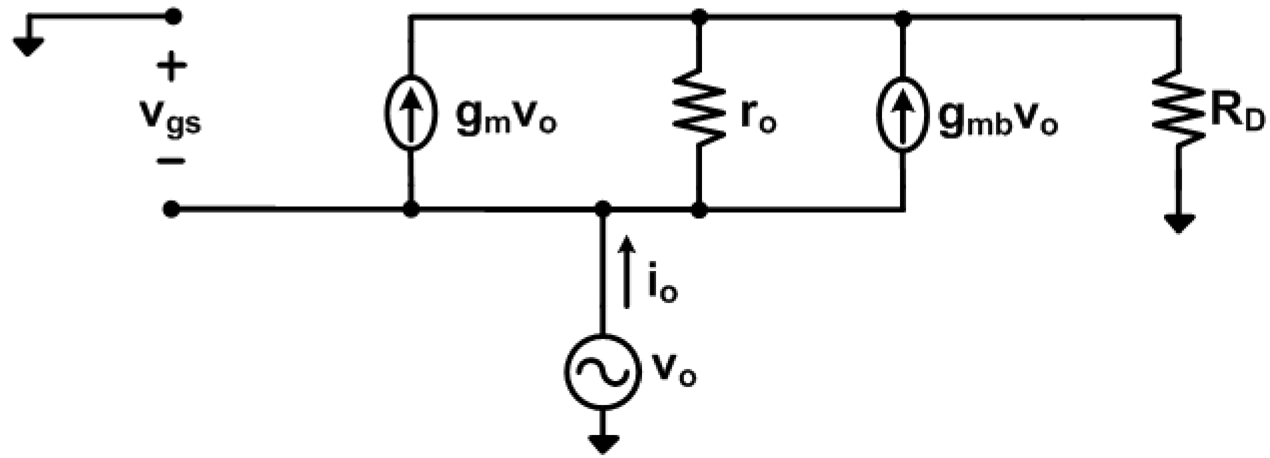


$$i_o = (g_m + g_{mb})v_o + \frac{v_o}{r_o} = (g_m + g_{mb} + g_o)v_o$$

$$r_{out} = \frac{1}{g_m + g_{mb} + g_o} \approx \frac{1}{g_m}$$

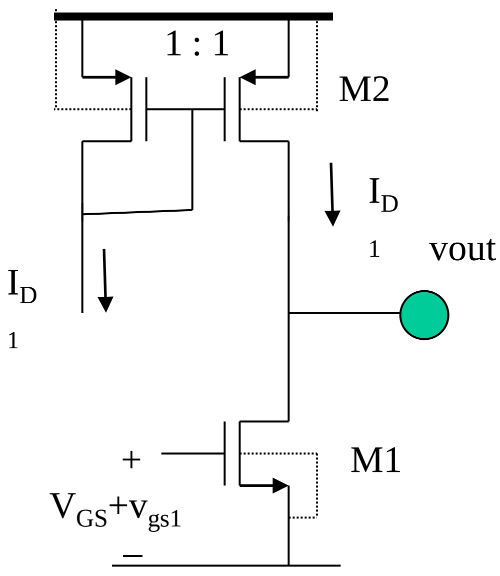
Small-Signal Impedance: Looking Into Source w/ Drain Resistor



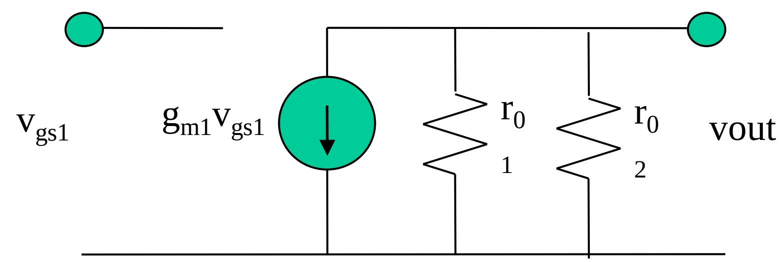


$$r_{out} = \frac{1}{g_m + g_{mb} + g_o}\left(1 + \frac{R_D}{r_o}\right)$$

Small signal analysis: Common-source amplifier

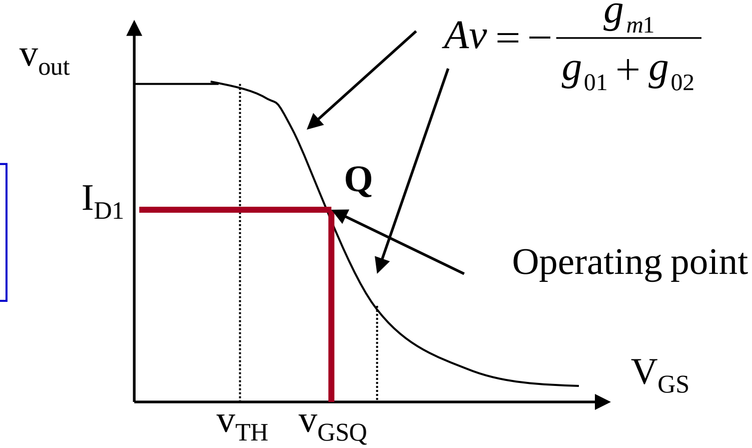


Small signal equivalent



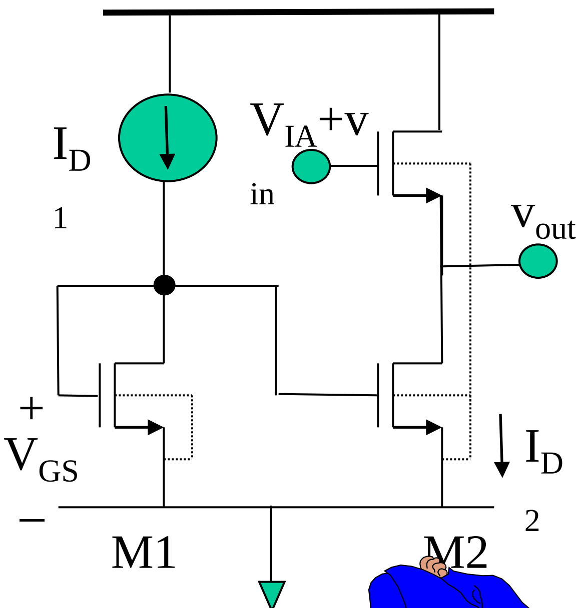
If $V_{OUT}>V_{DSAT1}$, $V_{OUT}<VDD-V_{SAT2}$

$$Av = -\frac{g_{m1}}{g_{01}+g_{02}}$$

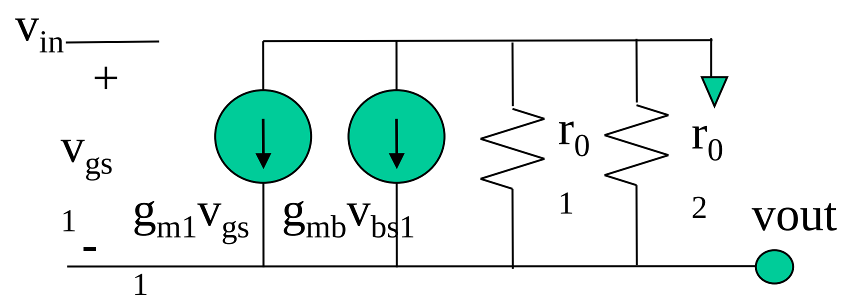


g_{m1}, g_{01}, and g_{02} are function of Q

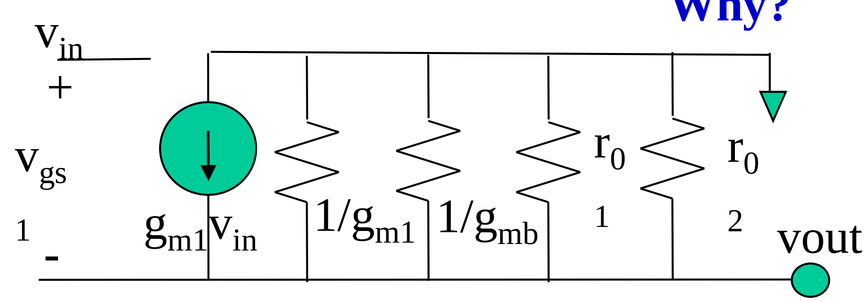
Small signal analysis: Common-drain (source follower) amplifier



Small signal equivalent circuit

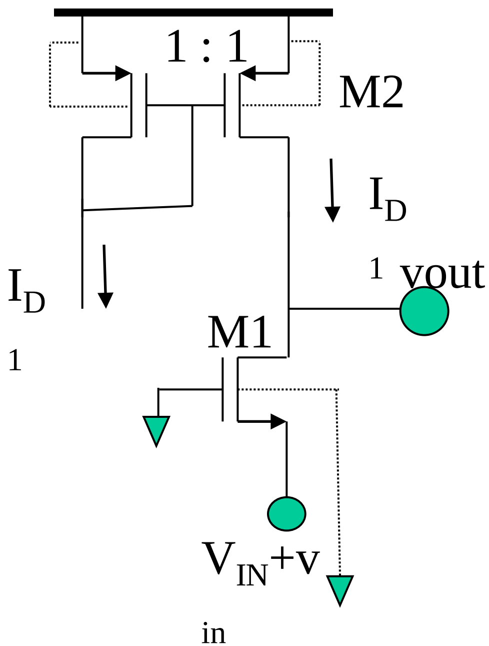


How this is done? Why?



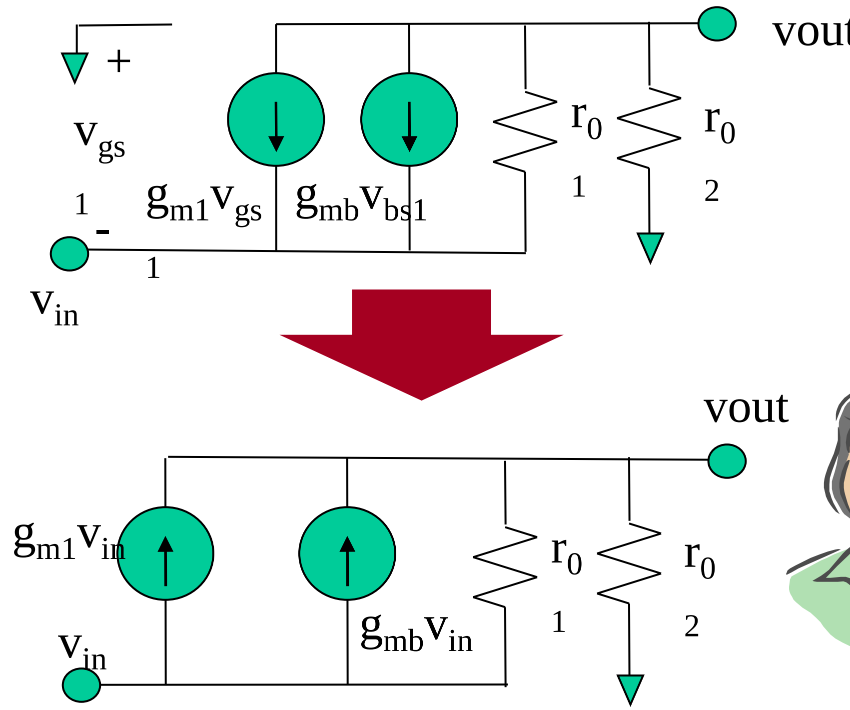
$$\frac{v_{out}}{v_{in}} = \frac{g_{m1}}{g_{m1} + g_{mb} + g_{01} + g_{02}}$$

Small signal analysis: Common-gate amplifier (cascode)



$$\frac{v_{out}}{v_{in}} = \frac{g_{m1} + g_{mb} + g_{01}}{g_{01} + g_{02}}$$

Small signal equivalent circuit

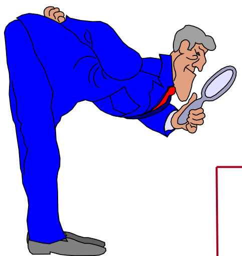


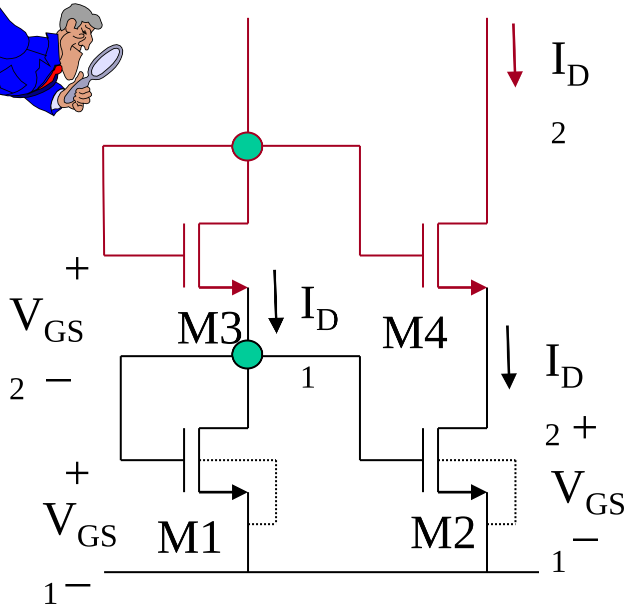
Impedance seen at Vin and Vout?
Are they relevant?

Precise Current Mirrors: Cascode structure

???

$$\text{Error} \approx \lambda_2 V_{DS2} - \lambda_1 V_{DS1}$$





M1 AND M2 ARE ACTING AS CURRENT MIRRORS

FUNDAMENTAL PRINCIPLE:

Error can be reduced if and only $\lambda_2=\lambda_1$ and $V_{DS2}=V_{DS1}$

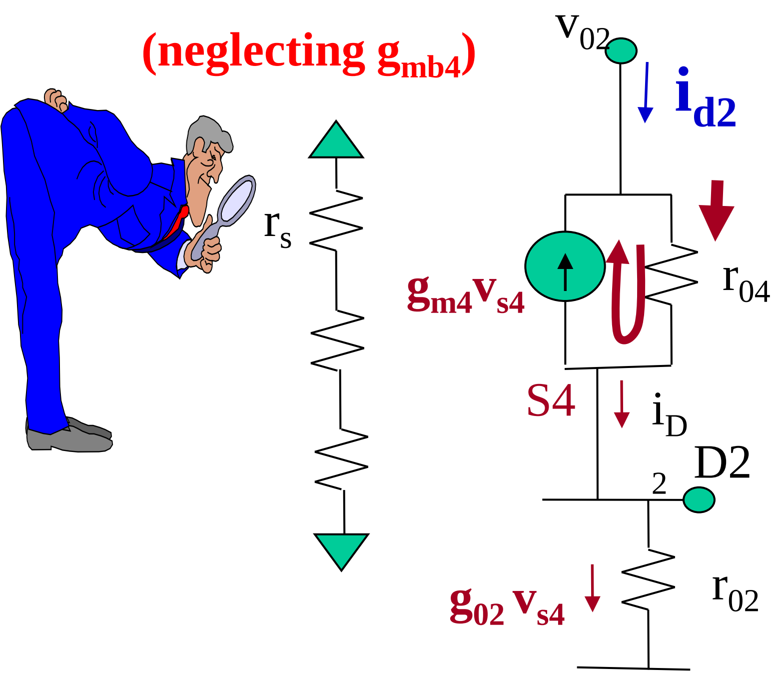
⇨**Transistors M1 and M2 are used as current mirrors**

⇨**Transistors M3 and M4 are used to have $V_{DS1}=V_{DS2}$.**

⇨**L1=L2 and ID1=ID2==>λ1=λ2**

⇨**If M1=M2 then μ1=μ2, and VT1=VT2**

Output impedance: Cascode structure



OUTPUT IMPEDANCE

$$Z_{out} = \frac{v_{02}}{i_{d2}}$$

$$i_{d2} = (v_{02} - v_{s4})g_{04} - g_{m4}v_{s4}$$

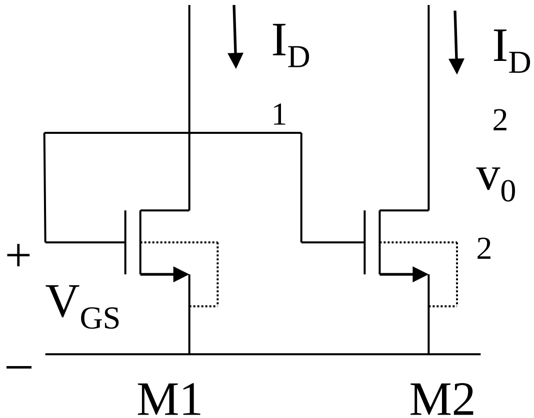
$$i_{d2} = g_{02}v_{s4}$$

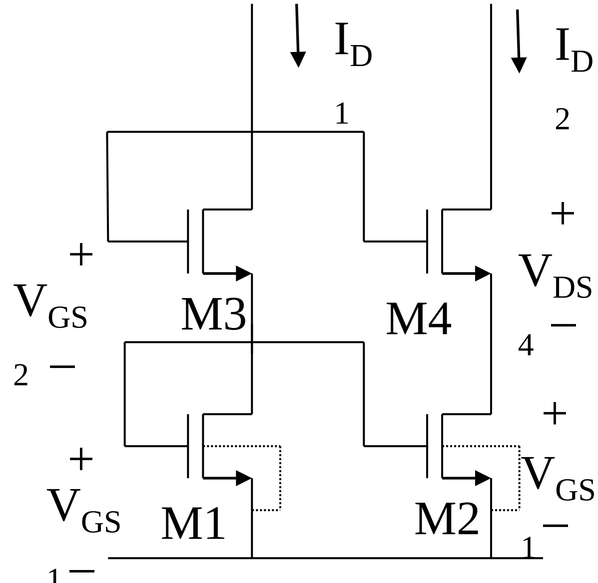
$$\boxed{Z_{out} = r_{02} + r_{04} + g_{m4}r_{02}r_{04}}$$

Notice that most of the AC current re-circulate within the cascode device and only i_{d2} is extracted from v_{02} !!

Compare g_{m4} with g_{02}!

Comparison of current sources: output impedance and headroom





~ **100-400 mV**

~ **0.9-1.5 V!**

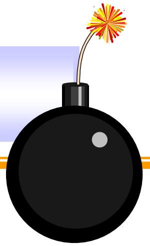
$$r_{out} = r_{02}$$

$$\boxed{r_{out} \cong g_{m4} r_{02} r_{04}}$$

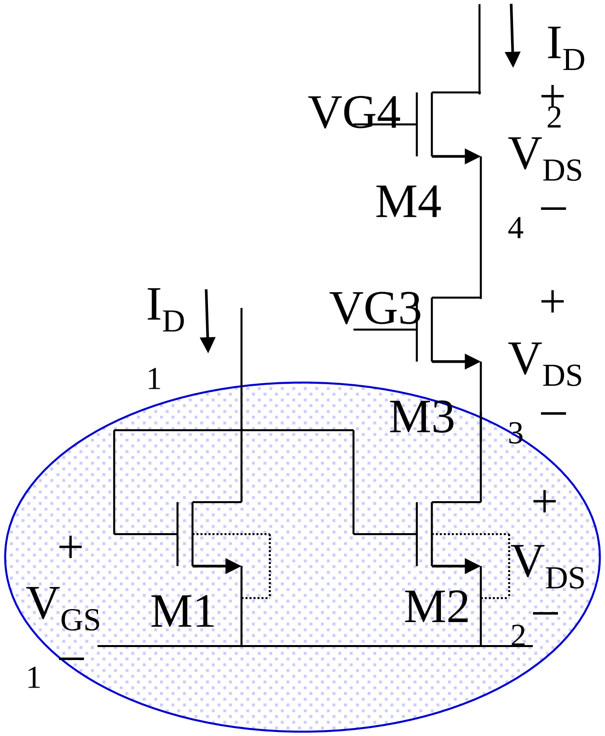
$$V_0 > V_{DSAT2}$$

$$V_0 > V_{GS1} + V_{DSAT4} = V_{T1} + V_{DSAT1} + V_{DSAT4}$$

~ 100-400 mV **~ 1 - 1.5 V!**



Double Cascode Structure: Advantages and drawbacks!



Small signal output resistance:

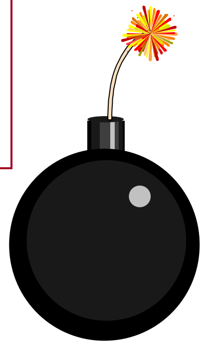
$$r_{out} \cong g_{m4}\left(r_{eq31}\right)r_{04} \cong g_{m4}\left(g_{m3}r_{02}r_{03}\right)r_{04}$$

$$V_0 > V_{DS2} + V_{DSAT3} + V_{DSAT4}$$

Output resistance is increased

Voltage swing is reduced

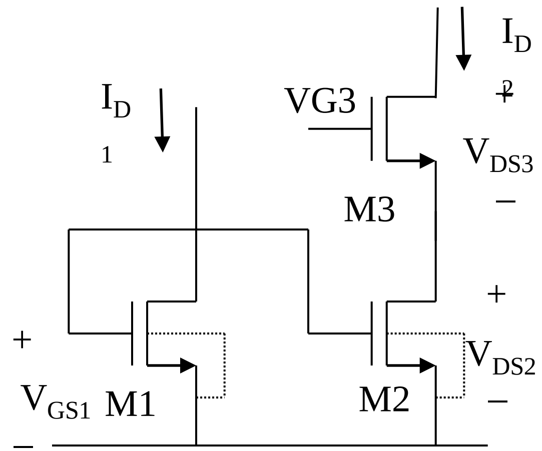
Parasitic poles could be an issue



Usually this section is more complex to ensure VDS is similar in both transistors M1 and M2

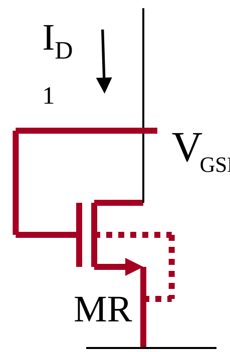
How VG3 and VG4 can be generated????

Voltage references (biasing cascode structures)

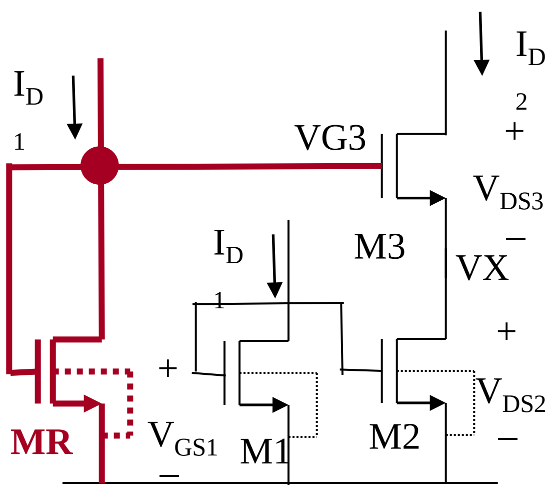


Lets consider the case: $V_{DS2}=V_{DSAT2}$

➢VG3 must be $V_{GS3}+V_{DSAT2}=V_{T3}+V_{DSAT3}+V_{DSAT2}$



$$V_{GSR}=V_{TR}+\underbrace{\sqrt{\frac{2}{\mu_n C_{OX}}\frac{L_R}{W_R}I_{D1}}}_{\text{VDSATR}}$$

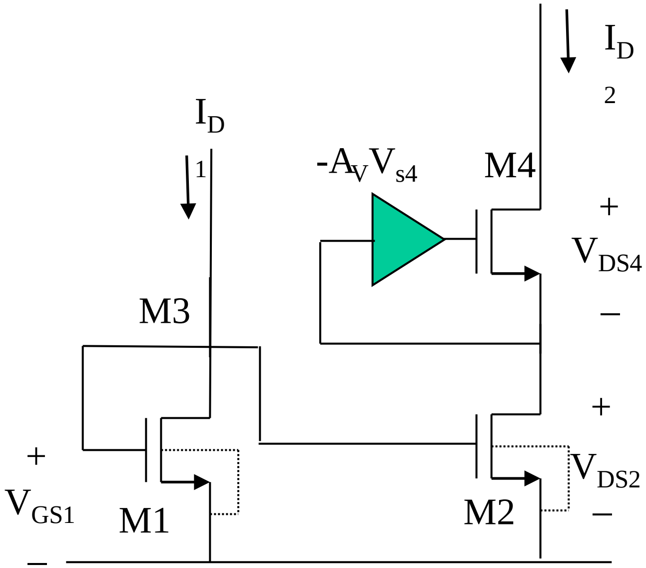


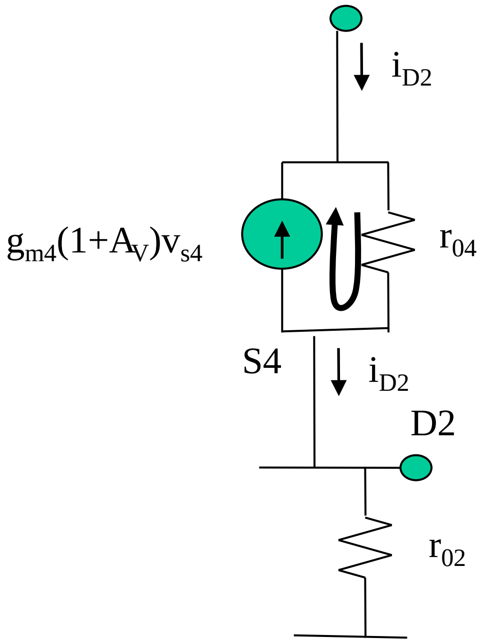
Increasing L/W by 4, VDSAT increases by 2

According to $(W/L)_1$, the gate dimensions for MR $(W/L)_R$ must be designed

Problem: VTR ≠ VT3 due to body effect
Partial solution: $(W/L)_1 > 4(W/L)_R \Rightarrow 9(W/L)_R$

Improved (self regulated) current source



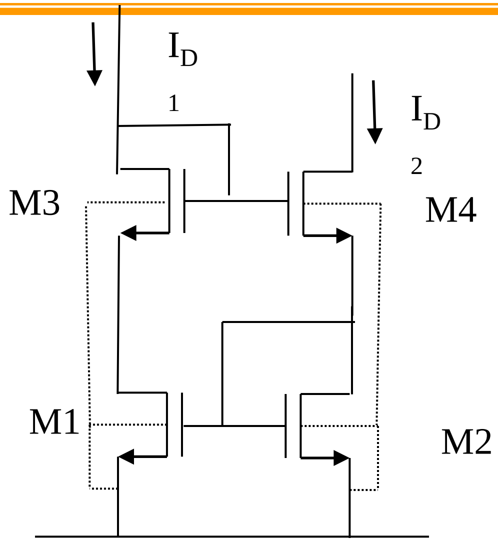


$$r_{out} \cong g_{m4}(1 + A_V)r_{02}r_{04}$$

Similar to double cascode

Key issue: Please understand the concept!!

Other current sources

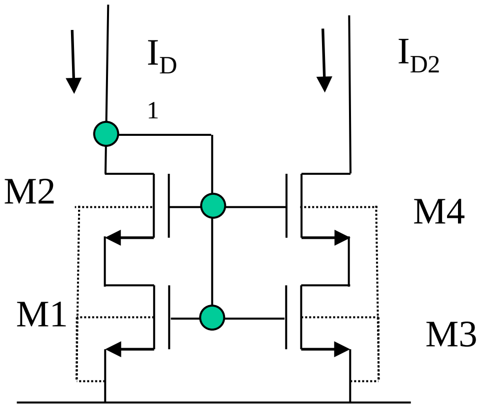


Wilson Current Source

$$r_{out} \cong g_{m4}(1 + A_V)(''r_{eq2}'')r_{04}$$

$$''r_{eq2}'' = 1/g_{m2}$$

Output resistance similar to cascode

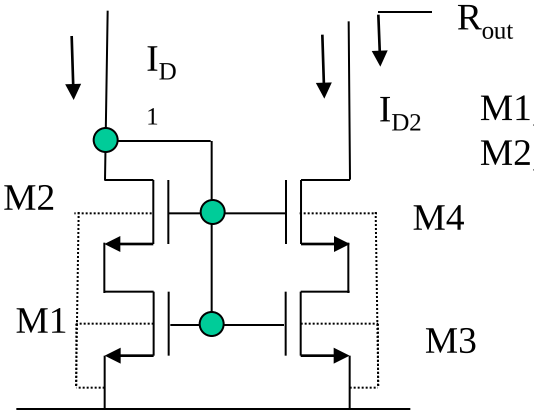


M1, M3 in triode region
M2, M4 are saturated

$\mathbf{r_{out}}$ **= ??**

Vout,min = ???

Other current sources



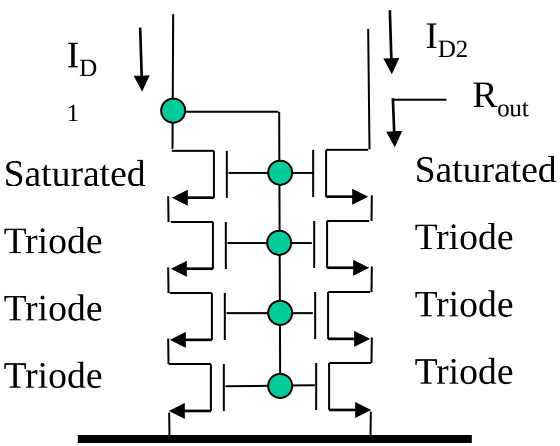
M1, M3 in triode region
M2, M4 are saturated

$$i_D = \mu C_{OX} \frac{W}{L_{eff}} \left[V_{GS} - V_T - 0.5 V_{DS} \right] V_{DS}$$

$$r_{ds\,3} = \frac{L_{eff}}{\mu C_{OX} W \left[V_{GS\,3} - V_T - V_{DS\,3} \right]}$$

$$r_{out} \cong g_{m\,4} r_{04} \left(r_{ds\,3} \right) \cong$$

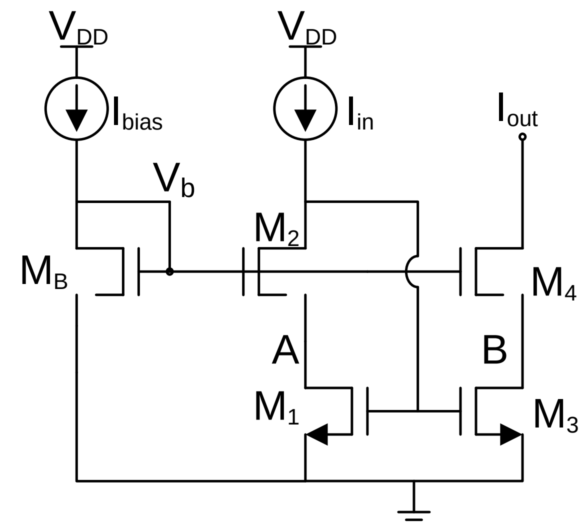
$$V_0 > V_{DS\,3} + V_{DSAT\,4}$$



$$\boxed{r_{out} \cong g_{m\,4} r_{04} \left(\sum r_{dsi} \right)}$$

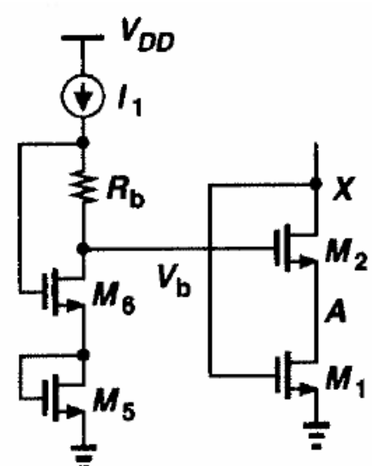
Low-Voltage Cascode Current Mirror

- M2 and M4 should be sized such that
  - $V_{GS2} = V_{GS4}$
- M1 and M3 biased near edge of saturation
  - $V_{DS1} \approx V_{DS3} \approx V_{DSAT}$
  - $V_b = V_{GS2} + (V_{GS1} - V_{T1}) = V_{GS4} + (V_{GS3} - V_{T3})$



$$\boxed{\textbf{Compliance Voltage} = V_{DSAT3} + V_{DSAT4}}$$

- Improved V_b generation circuit
  - M5 sized such that $V_{GS5} \approx V_{GS2}$
    - Some body effect error here
  - Size M6 and Rb such that
    - $V_{DS6} = V_{GS6} - R_b I_1 \approx V_{GS1} - V_{T1}$



[Razavi]

Next Time

- Single-Stage Amplifiers