ECEN474/704: (Analog) VLSI Circuit Design
Spring 2018

Lecture 5: Layout Techniques

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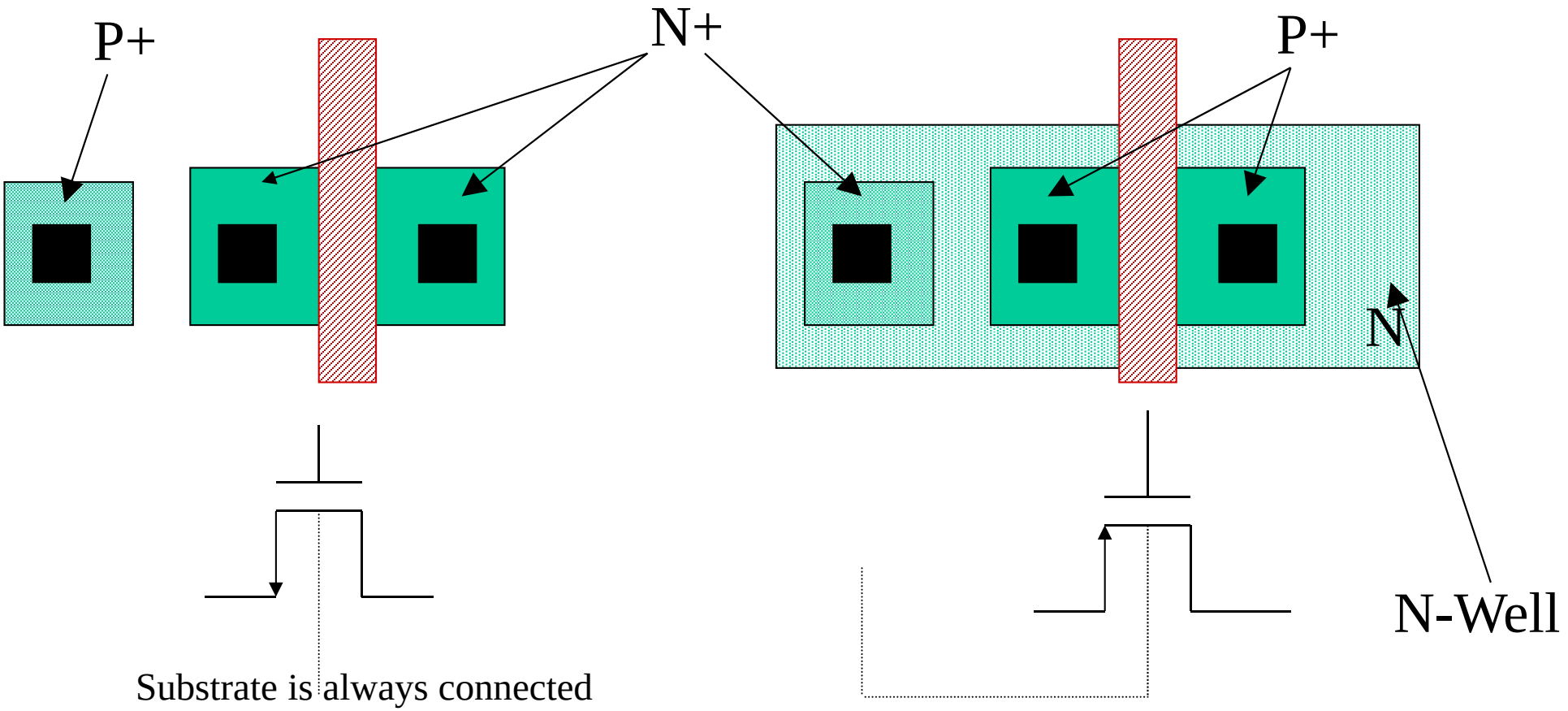
Announcements

- HW1 is due today
- Exam1 is on 2/13
  - 11:10-12:35PM (10 extra minutes)
  - Closed book w/ one standard note sheet
  - 8.5”x11” front & back
  - Bring your calculator
  - Covers material through lecture 5
  - Previous years’ Exam 1s are posted on the website for reference
- Reference Material
  - Razavi Chapter 18 & 19

Agenda

- MOS Fabrication Sequence
- CMOS Design Rules
- Layout Techniques
- Layout Examples

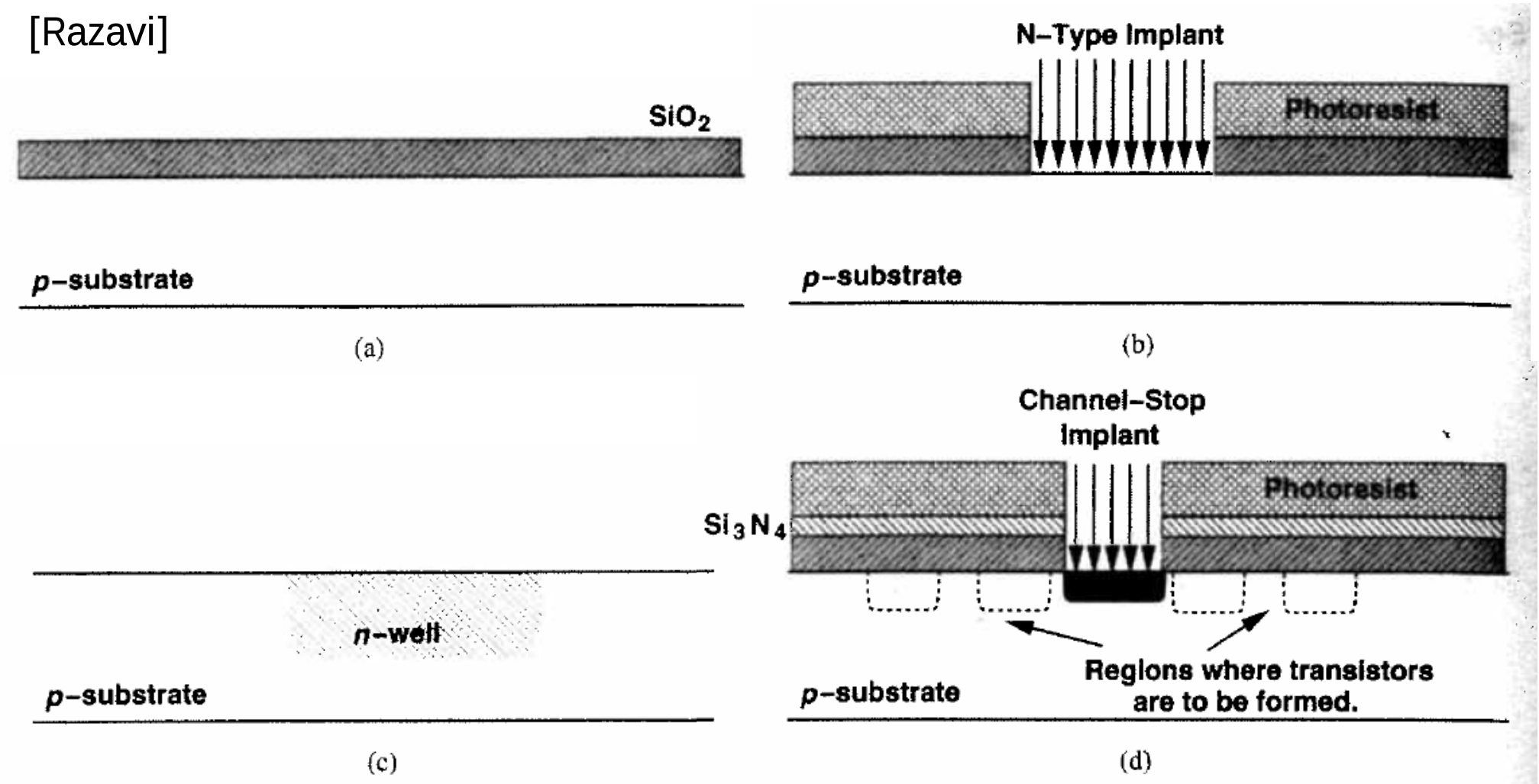
Fundamentals on Layout Techniques: N-Well CMOS Technologies



Substrate is always connected to the most negative voltage, and is shared by all N-type transistors

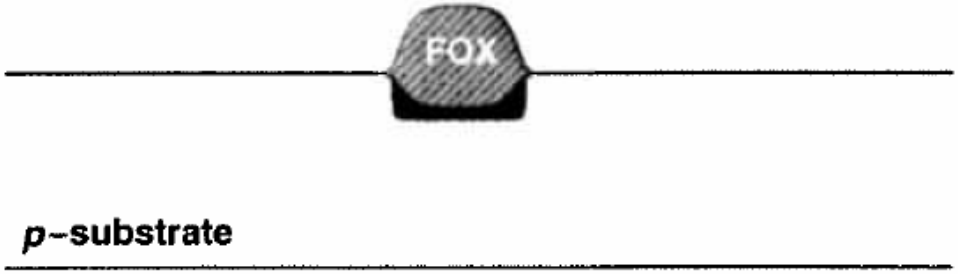
MOS Fabrication Sequence

[Razavi]

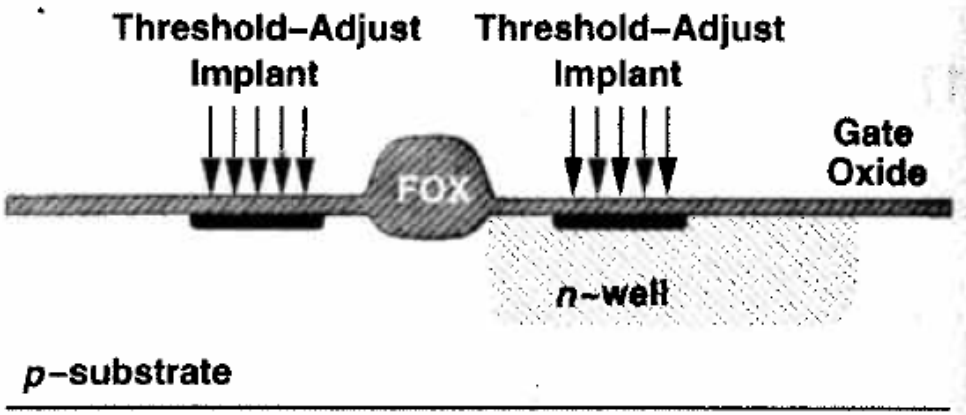


MOS Fabrication Sequence

[Razavi]



(e)



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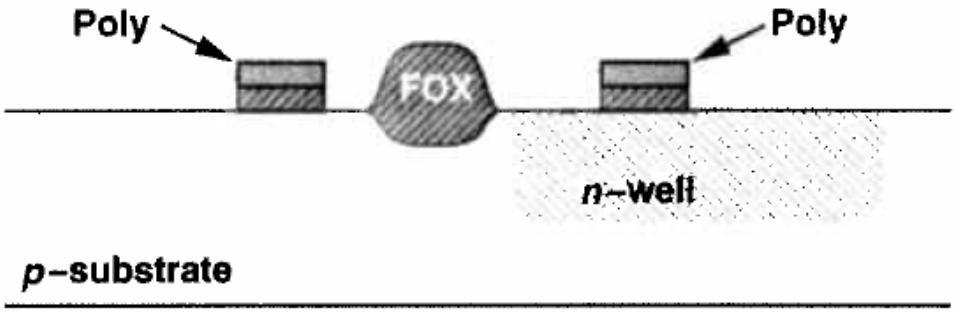

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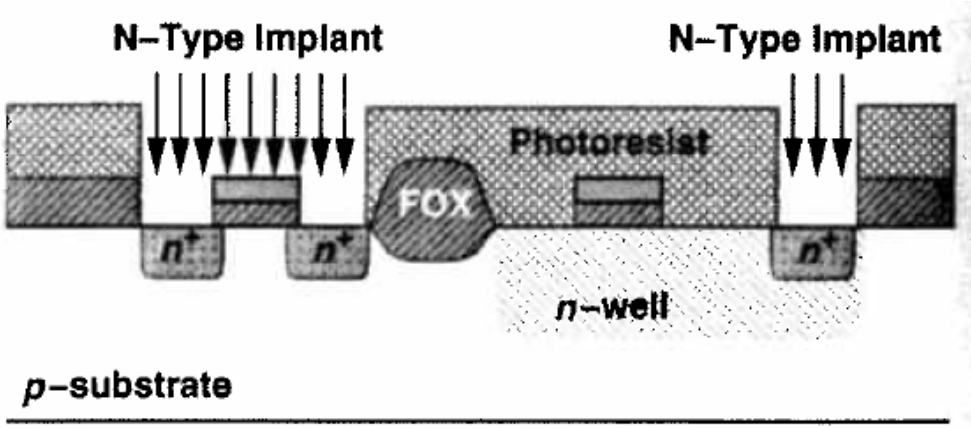
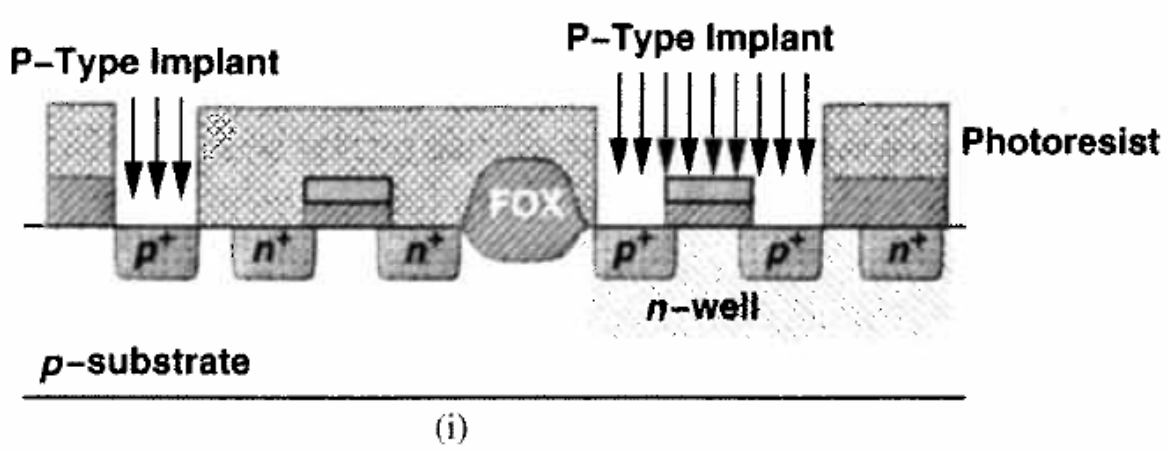


(h)

MOS Fabrication Sequence

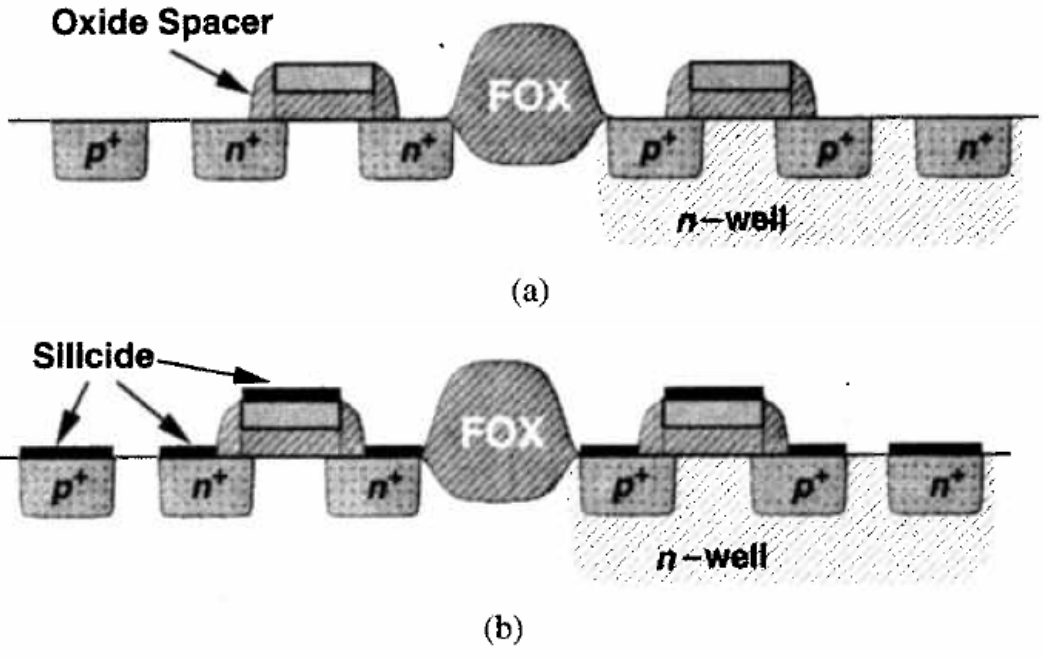
[Razavi]



"Front-End"

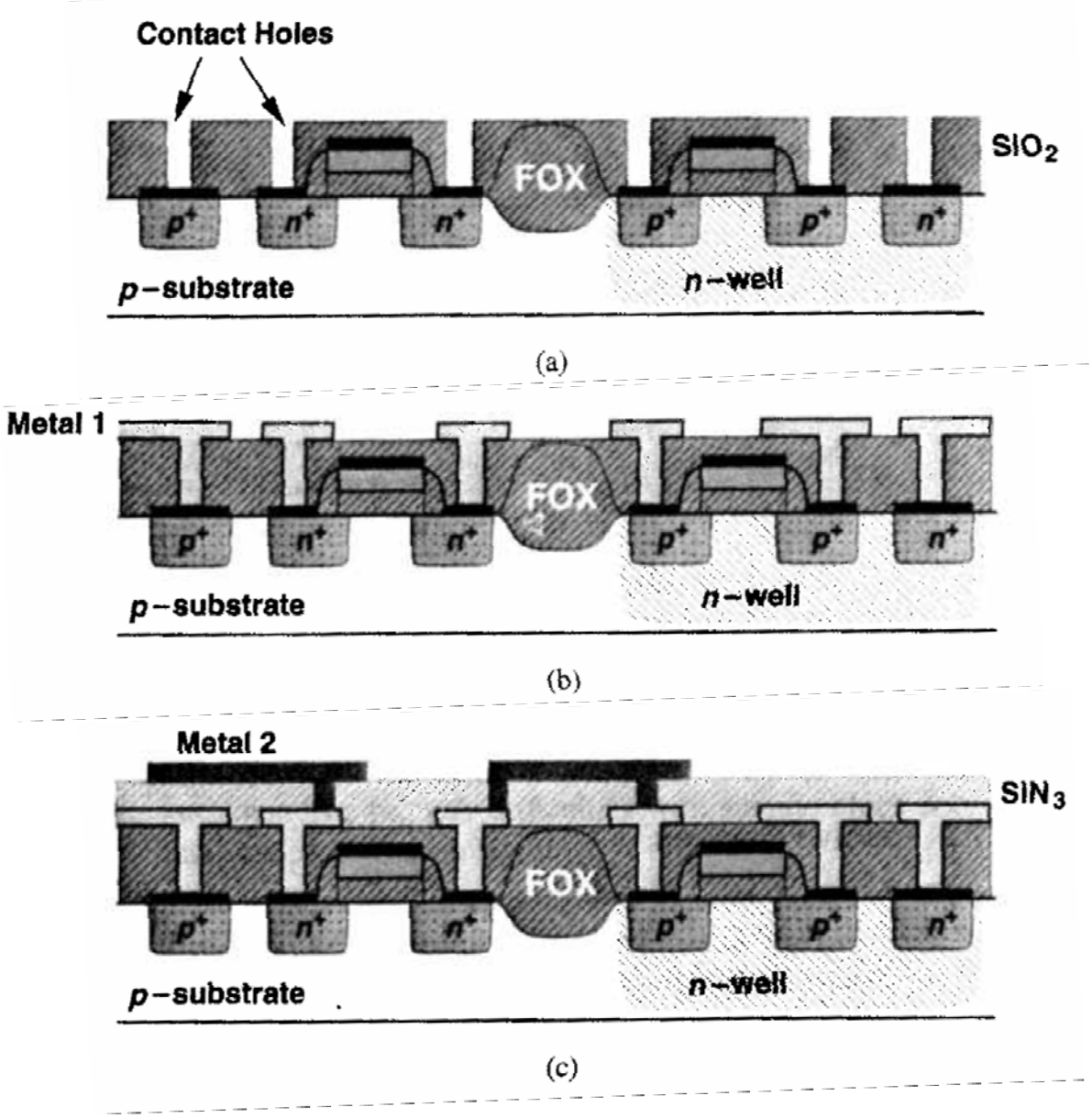
"Back-End"

- A "silicide" step, where highly conductive metal is deposited on the gate and diffusion regions, reduces transistor terminal resistance
- To prevent potential gate-source/drain shorting an "oxide spacer" is first formed before silicide deposition



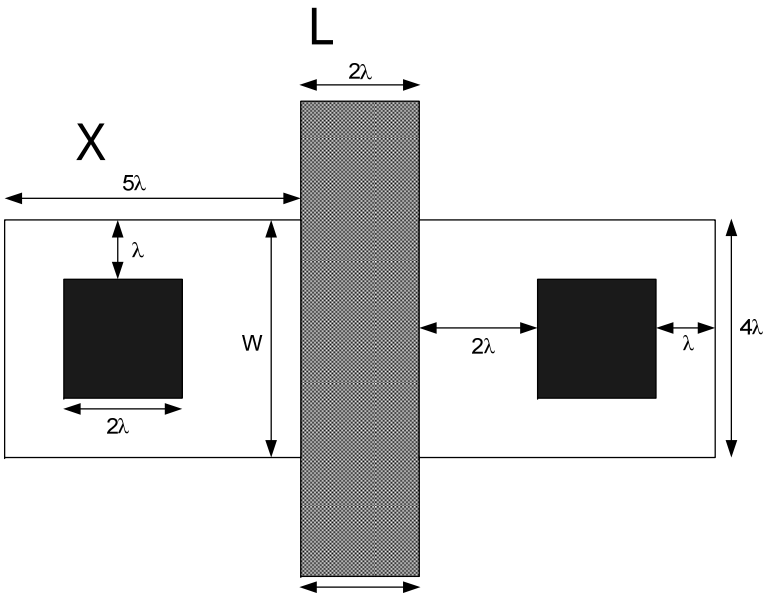
Contact and Metal Fabrication

[Razavi]



Transistor Geometries

- λ-based design rules allow a process and feature size-independent way of setting mask dimensions to scale
  - Due to complexity of modern processing, not used often today



- Minimum drawing feature = λ
  - Assume w.c. mask alignment <0.75λ
  - Relative misalignment between 2 masks is <1.5λ

$$AGate = W * L$$

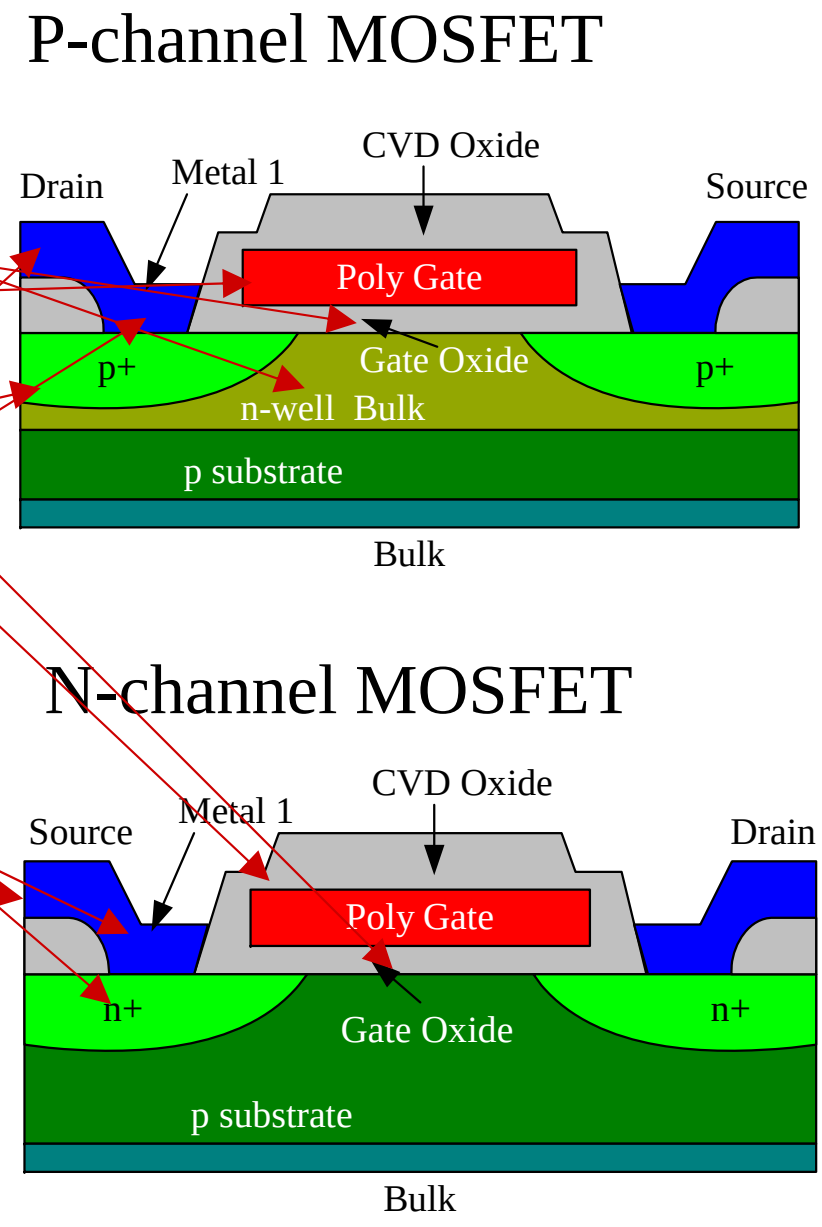
$$AD, AS = W * X$$

$$PS, PS = W + 2X \ \textbf{(3 sides)}$$

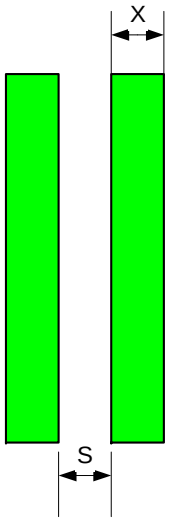
- X depends on contact size
  - 5λ in this example

BASIC SCNA CMOS LAYERS

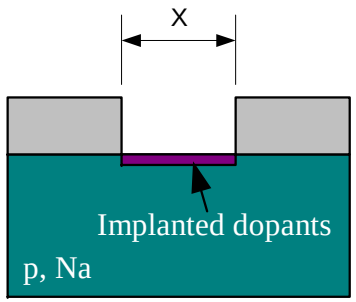
Physical Layer
N-well
Silicon Nitride
Polysilicon Layer 1
Polysilicon Layer 2
P+ Ion Implant
N+ Ion Implant
Contact cut to n+/p_
Metal 1
Via Oxide Cuts
Metal 2
Pad Contact (Overglass)



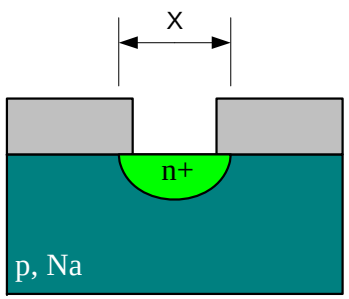
Design Rule Basics



Minimum width and spacing

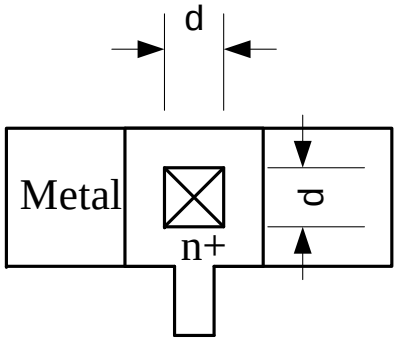


(a) Mask definition

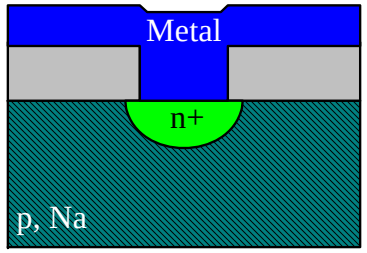


(b) After annealing

Patterning sequence for a doped n+ line.

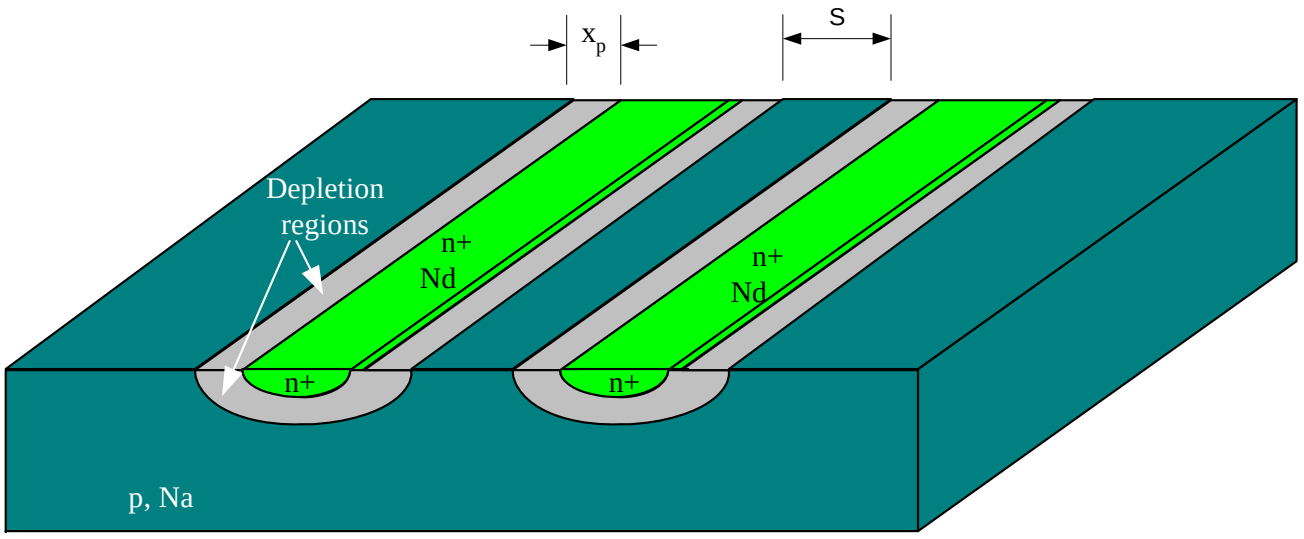


(a) Contact size

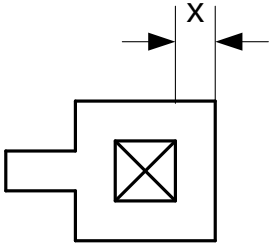


(b) Side view

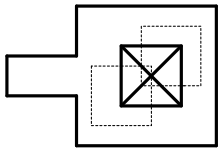
Geometry of a contact cut



Depletion regions due to parallel n+ lines

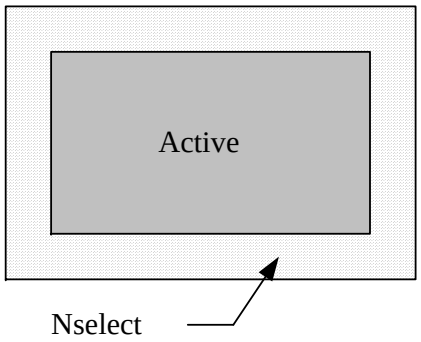


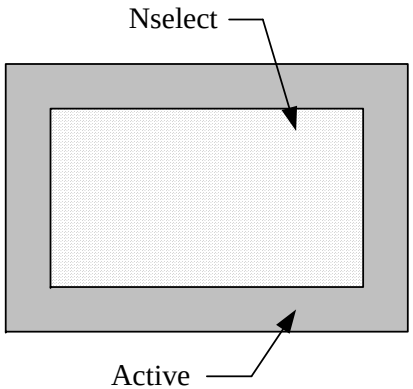
(a) Masking Design

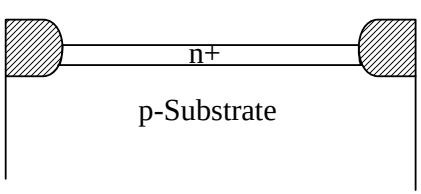


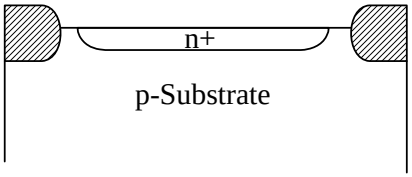
(b) Registration tolerance

Contact spacing rule



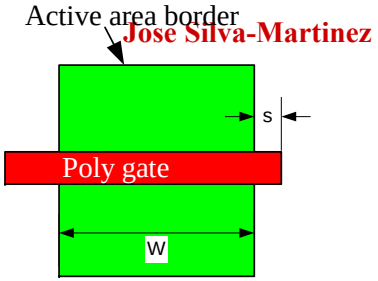




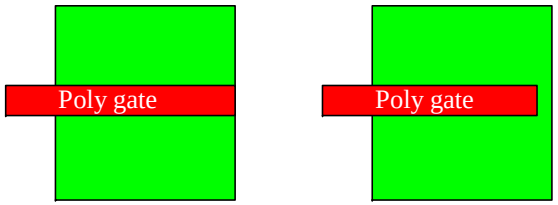


(a) Correct mask sizing (b) Incorrect mask sizing

Formation of n+ regions in an n-channel MOSFET

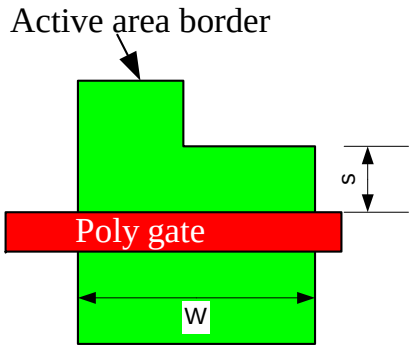


Gate overhang in MOSFET layout

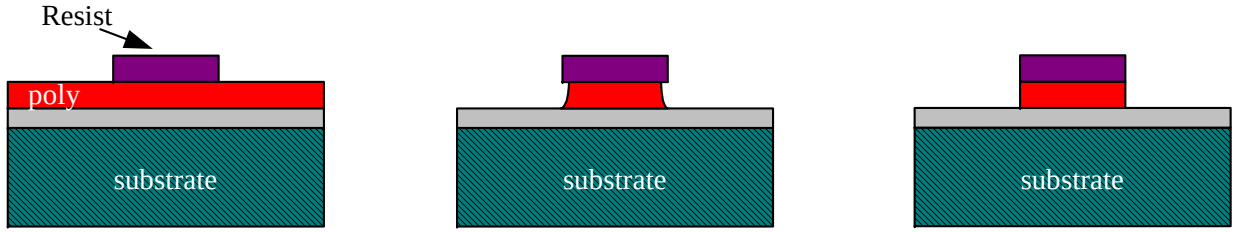


(a) No overhang (b) With misalignment

Effect of misalignment without overhang



Gate spacing form an n+ edge

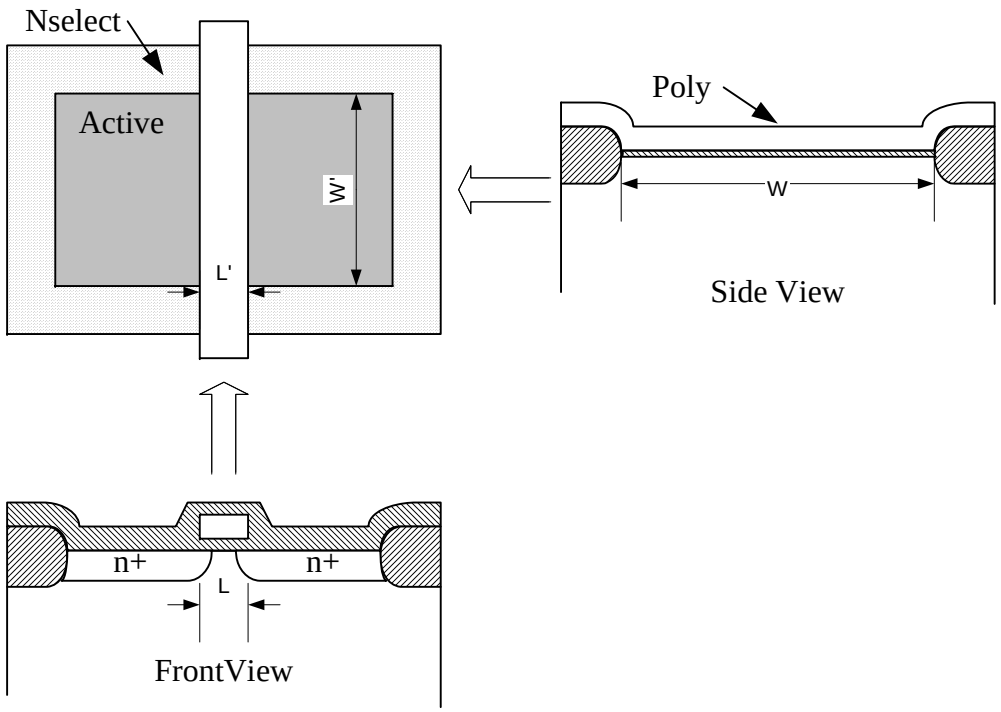


(a) Resist pattern (b) Isotropic etch (c) anisotropic etch

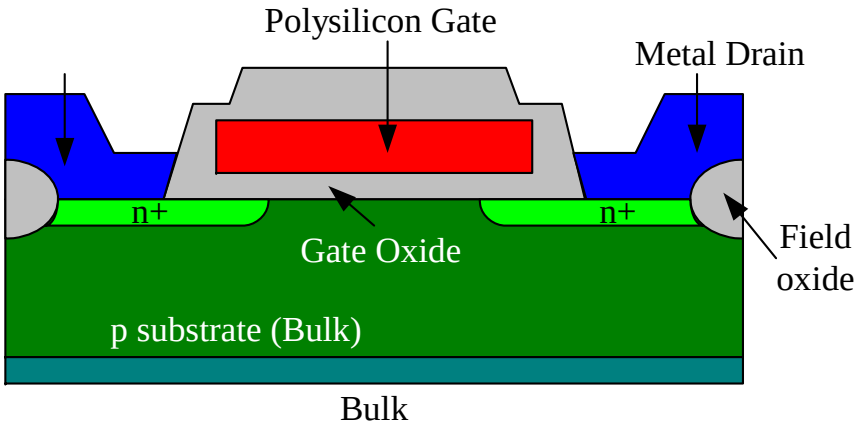
Effect of misalignment without overhang

Mask Number	Mask Layer
1	NWELL
2	ACTIVE
3	POLY
4	SELECT
5	POLY CONTACT
6	ACTIVE CONTACT
7	METAL1
8	VIA
9	METAL2
10	PAD
11	POLY2

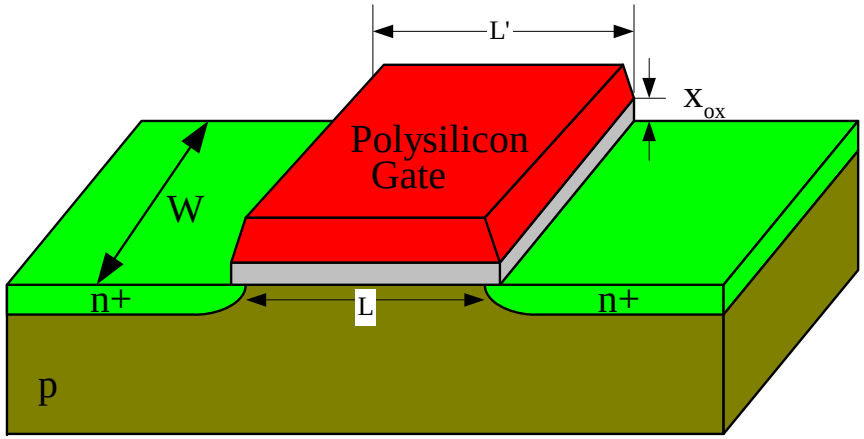
Design Rule Layers



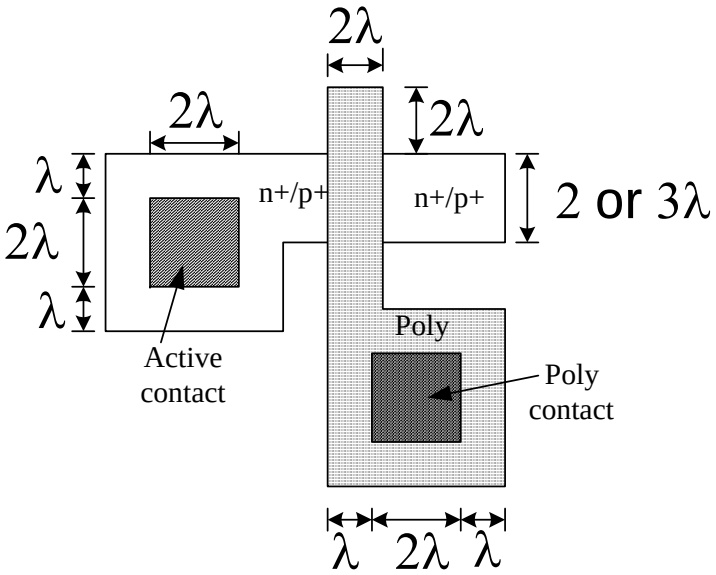
Difference between the drawn and physical values for channel length and the channel width



Structure of a n-channel MOSFET



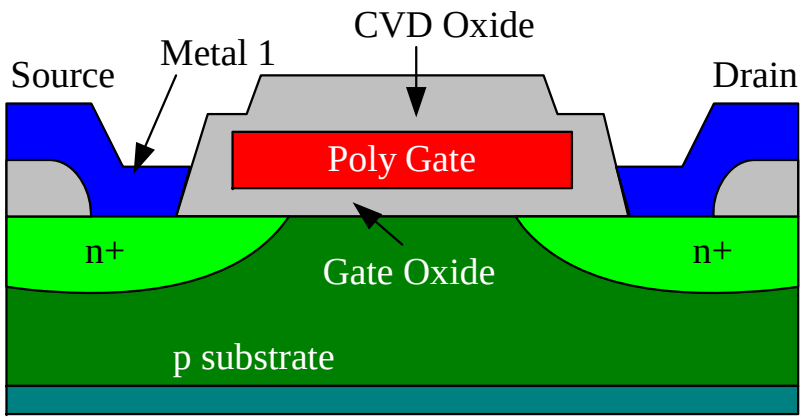
Perspective view of an n-channel MOSFET

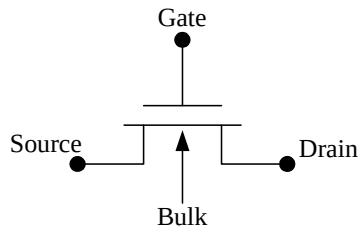


Example of Layout Rules

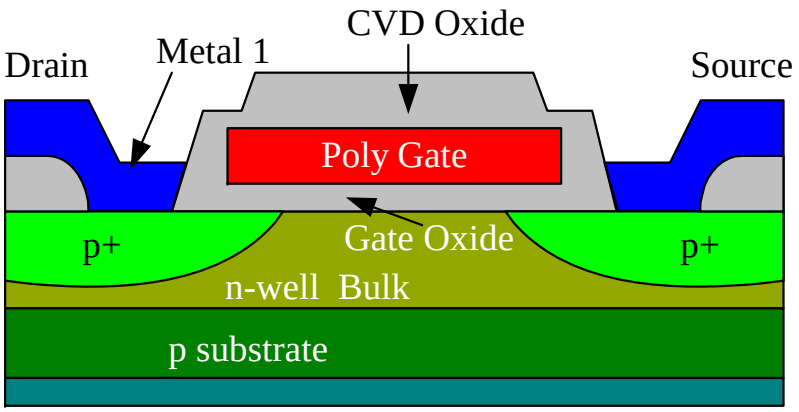
- Minimum transistor width is set by minimum diffusion width
  - 2 or 3λ (check with TA)
- Often, we use a use a slightly larger “minimum” that is equal to the contact height (4λ in this example)

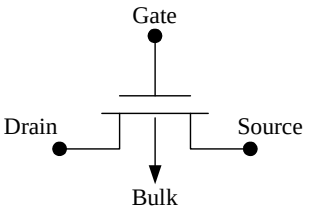
N-channel MOSFET





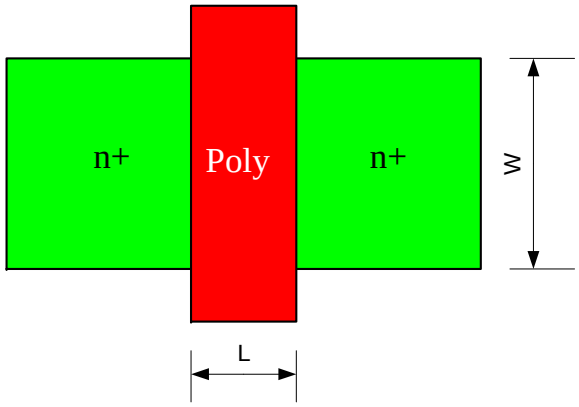
P-channel MOSFET

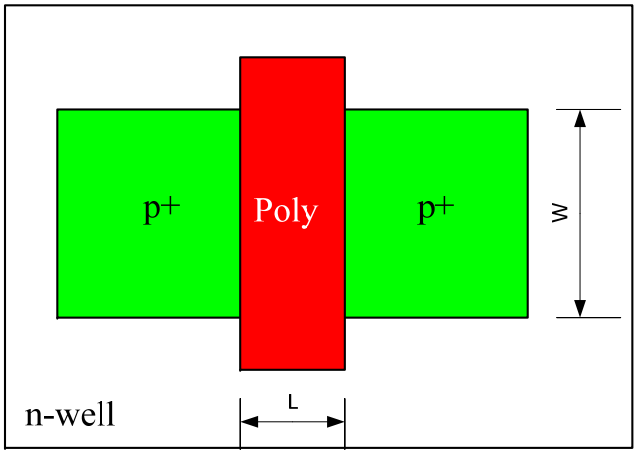




(a) Cross section

(b) Circuit symbol

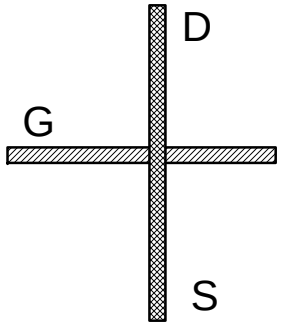




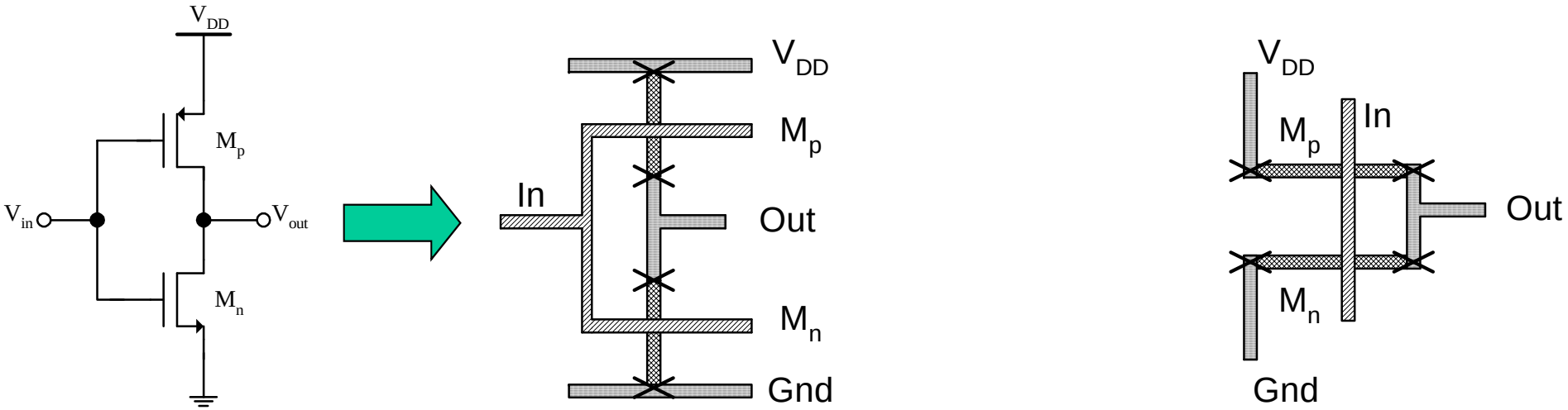
(c) Top view

Stick Diagrams

(a) Definitions

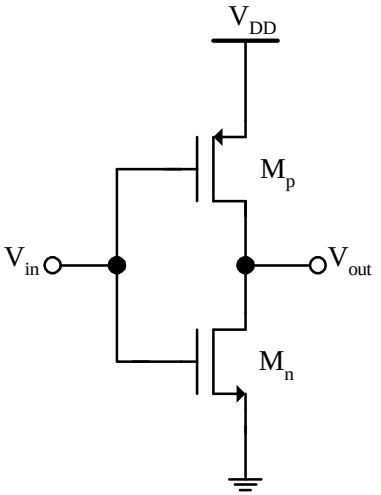


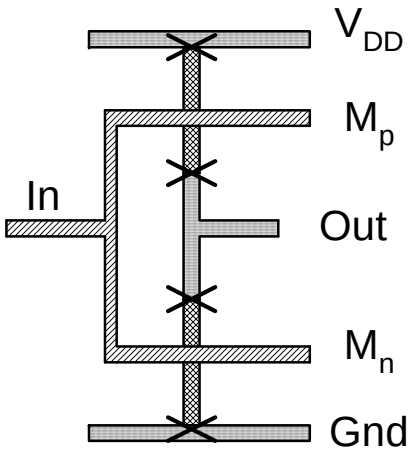
(b) MOSFET

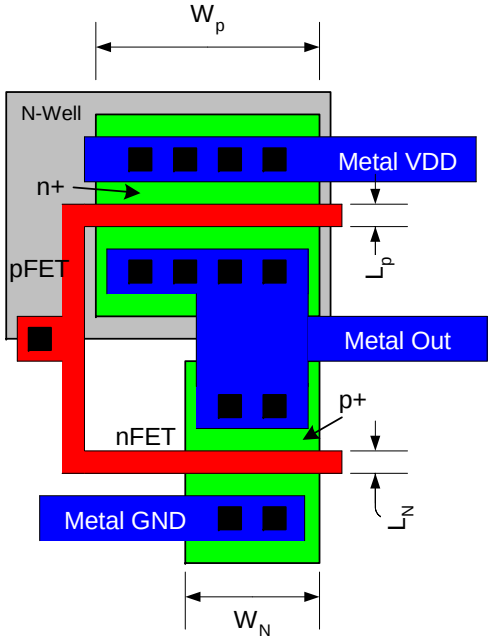


Stick diagrams for the CMOS Inverter

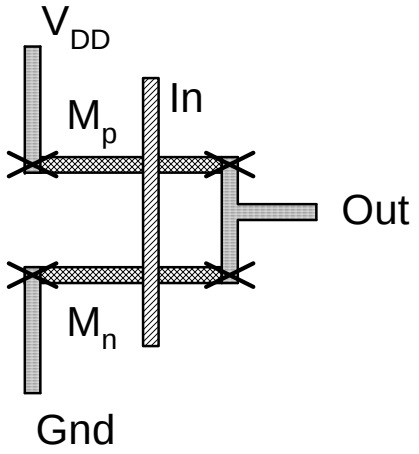
The CMOS Inverter

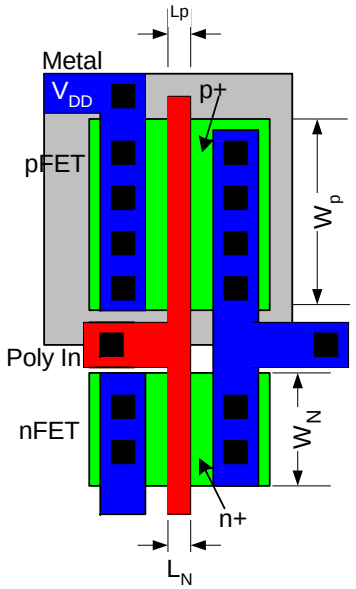






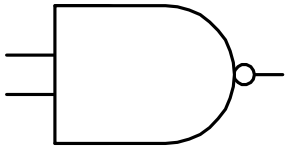
Basic Inverter Layout

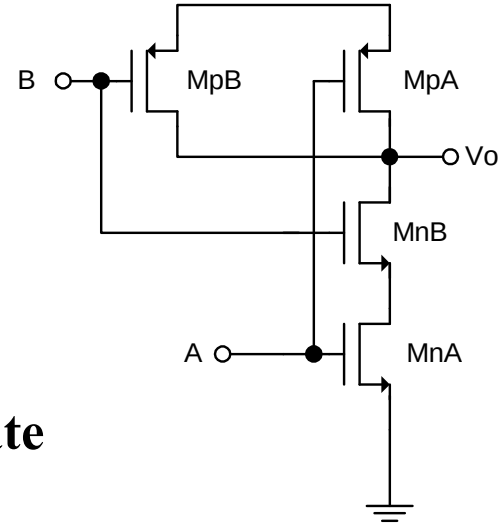


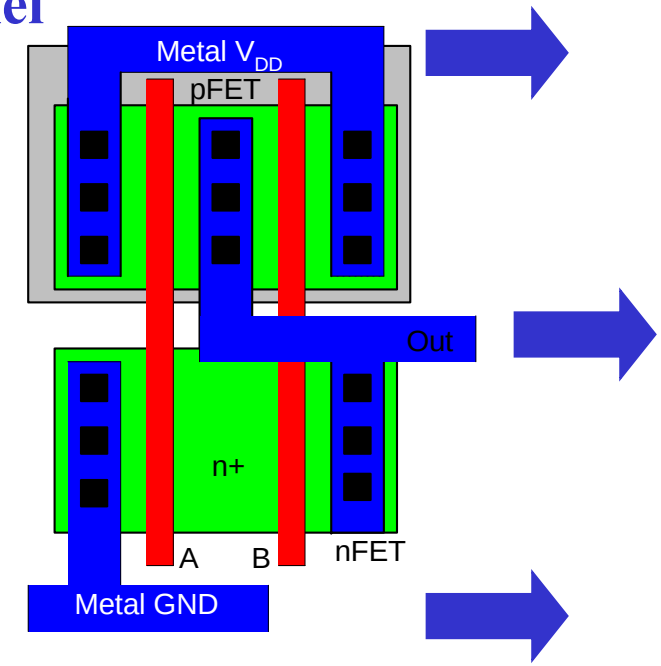


Alternate Inverter Layout

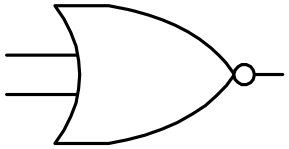
Standard Cells: VDD, VSS and output run in Parallel

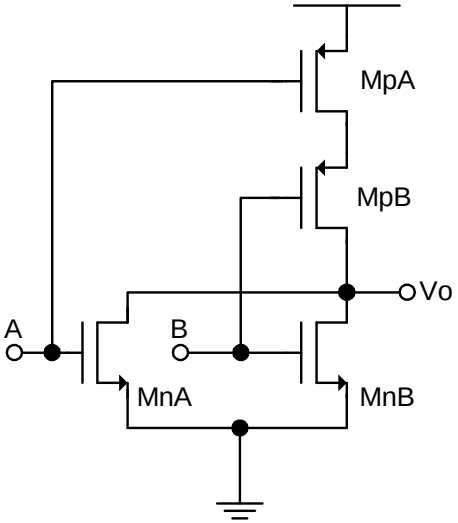


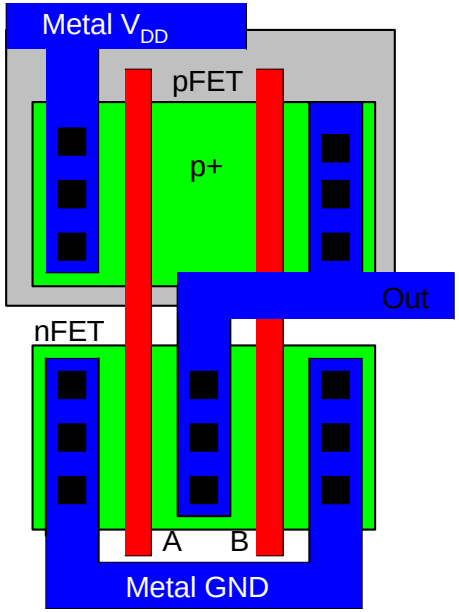




CMOS NAND2 logic gate



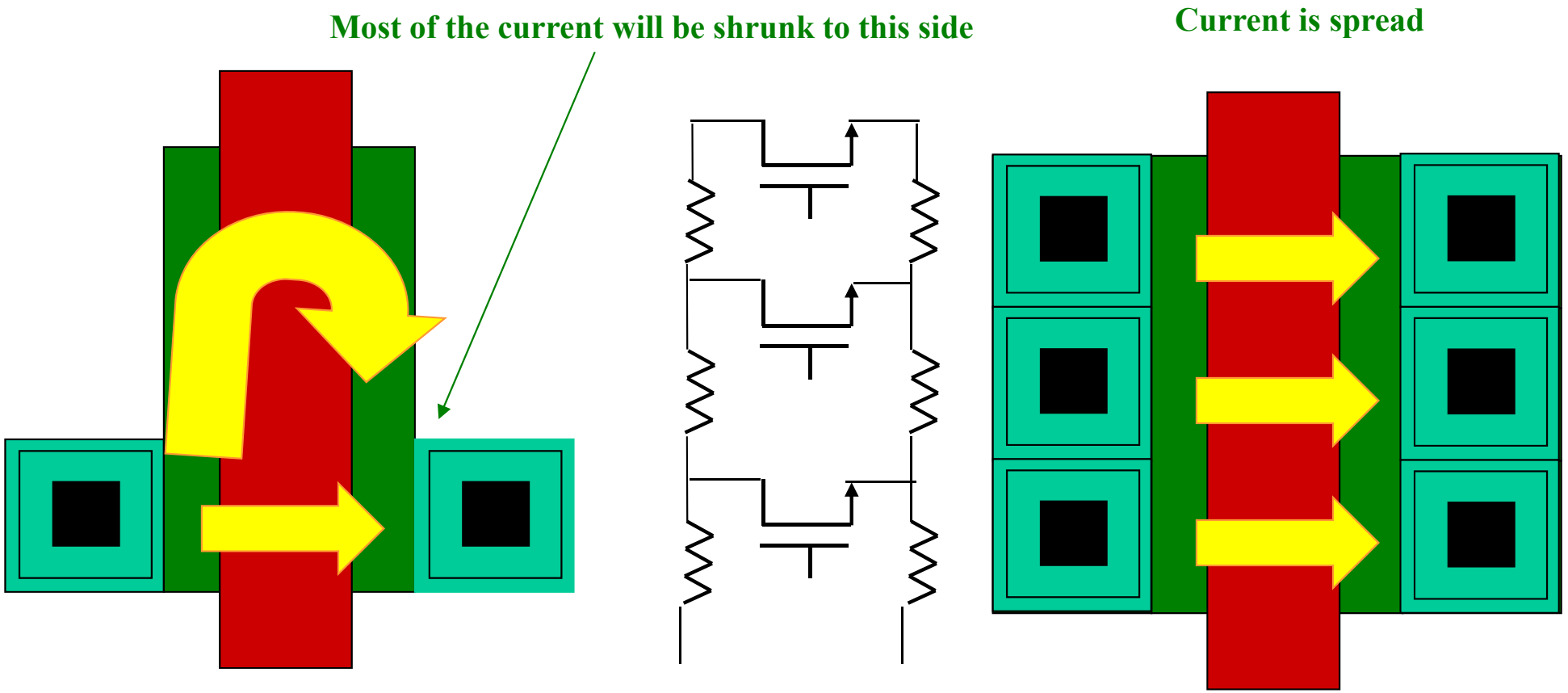




CMOS NOR2 logic gate

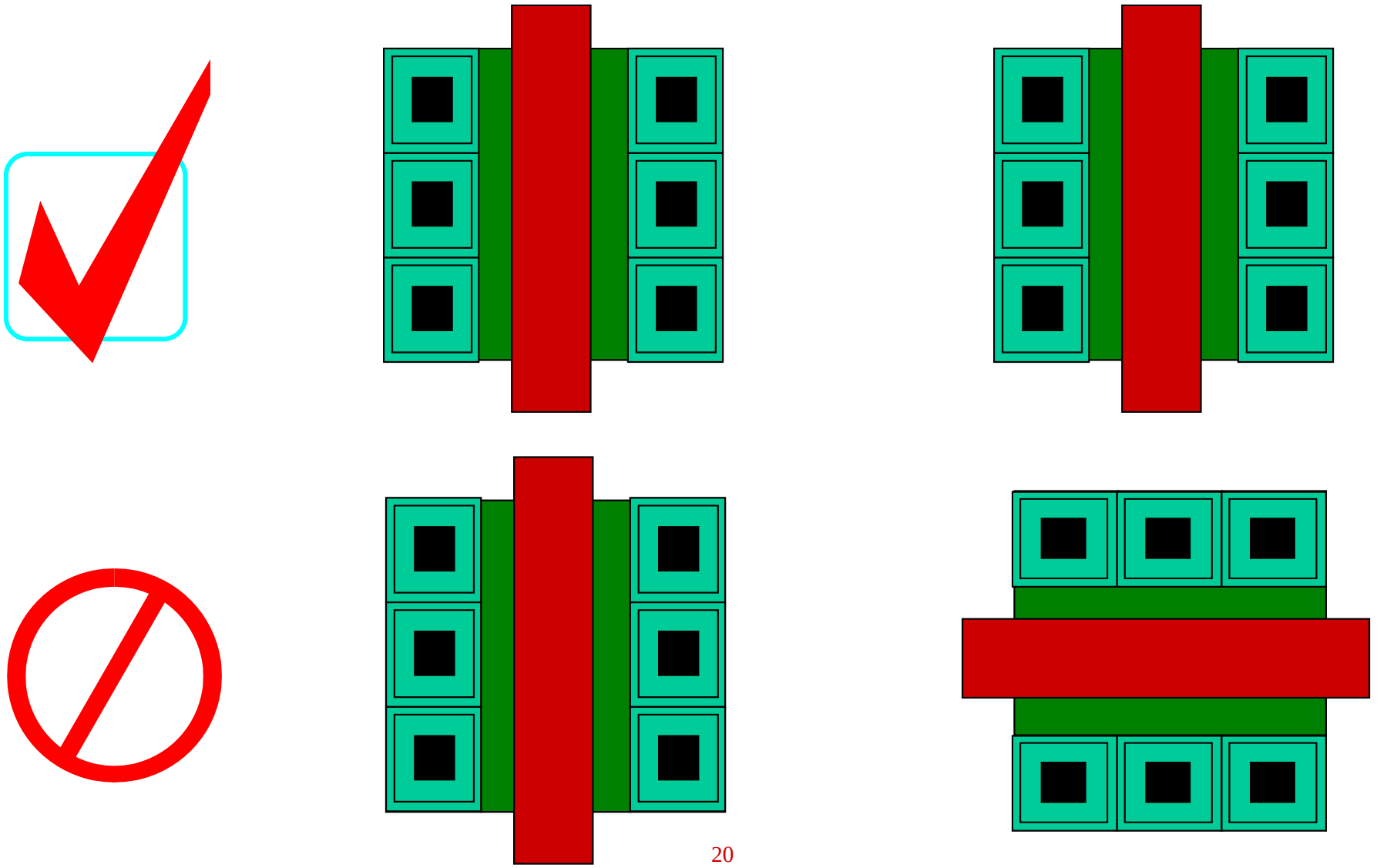
Wide Analog Transistor: Analog techniques

- Unacceptable drain and source resistance
- Stray resistances in transistor structure
- Contacts short the distributed resistance of diffused areas



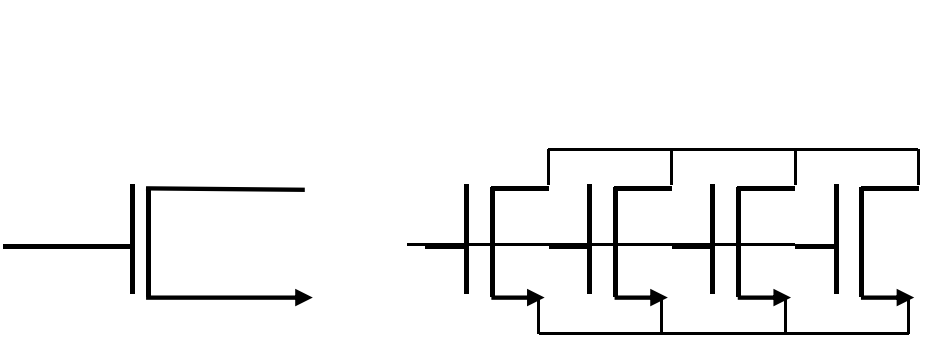
Transistor orientation

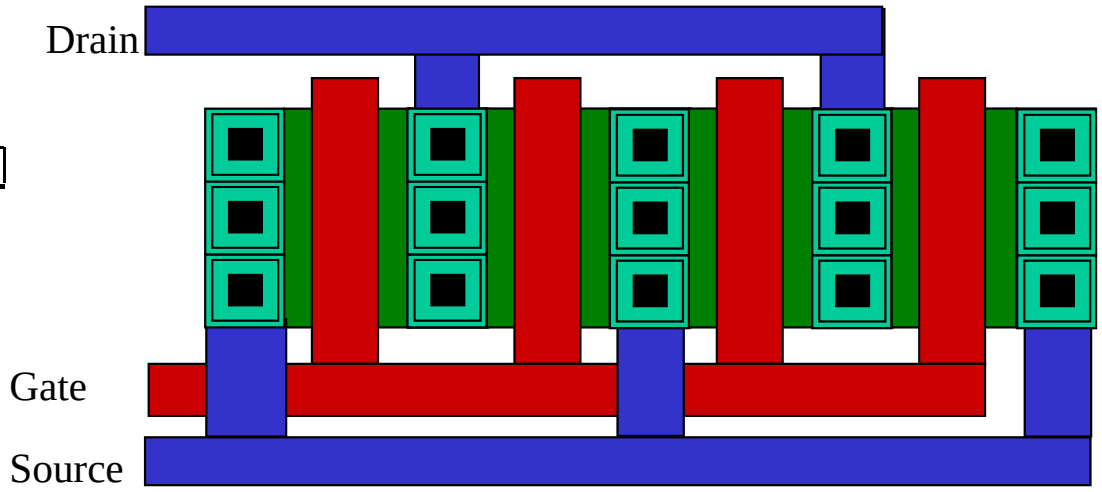
- Orientation is important in analog circuits for matching purposes



Stacked Transistors

- Wide transistors need to be split
- Parallel connection of *n* elements ($n = 4$ for this example)
- Contact space is shared among transistors
- Parasitic capacitances are reduced (important for high speed)
- Gate resistance is reduced

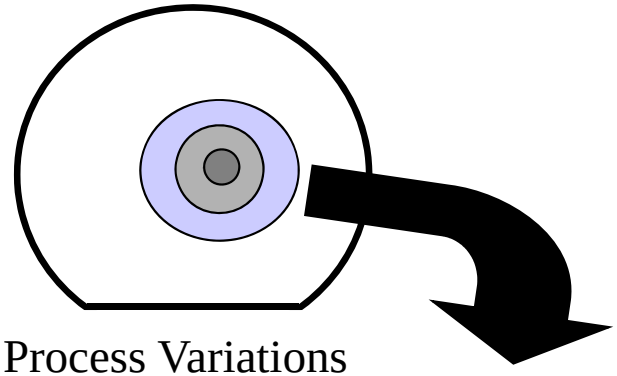




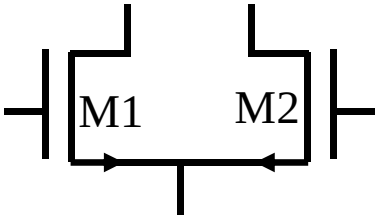
Note that parasitic capacitors are lesser at the drain

Matched Transistors

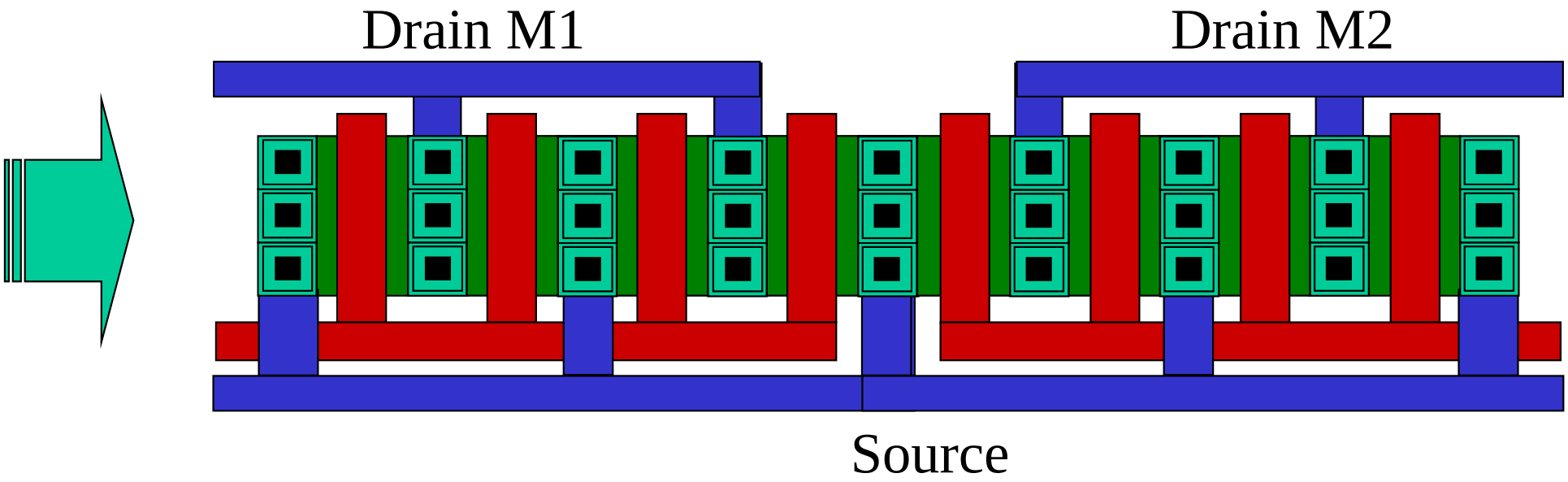
- Simple layouts are prone to process variations, e.g. V_T, KP, C_{ox}
- Matched transistors require elaborated layout techniques



Process Variations

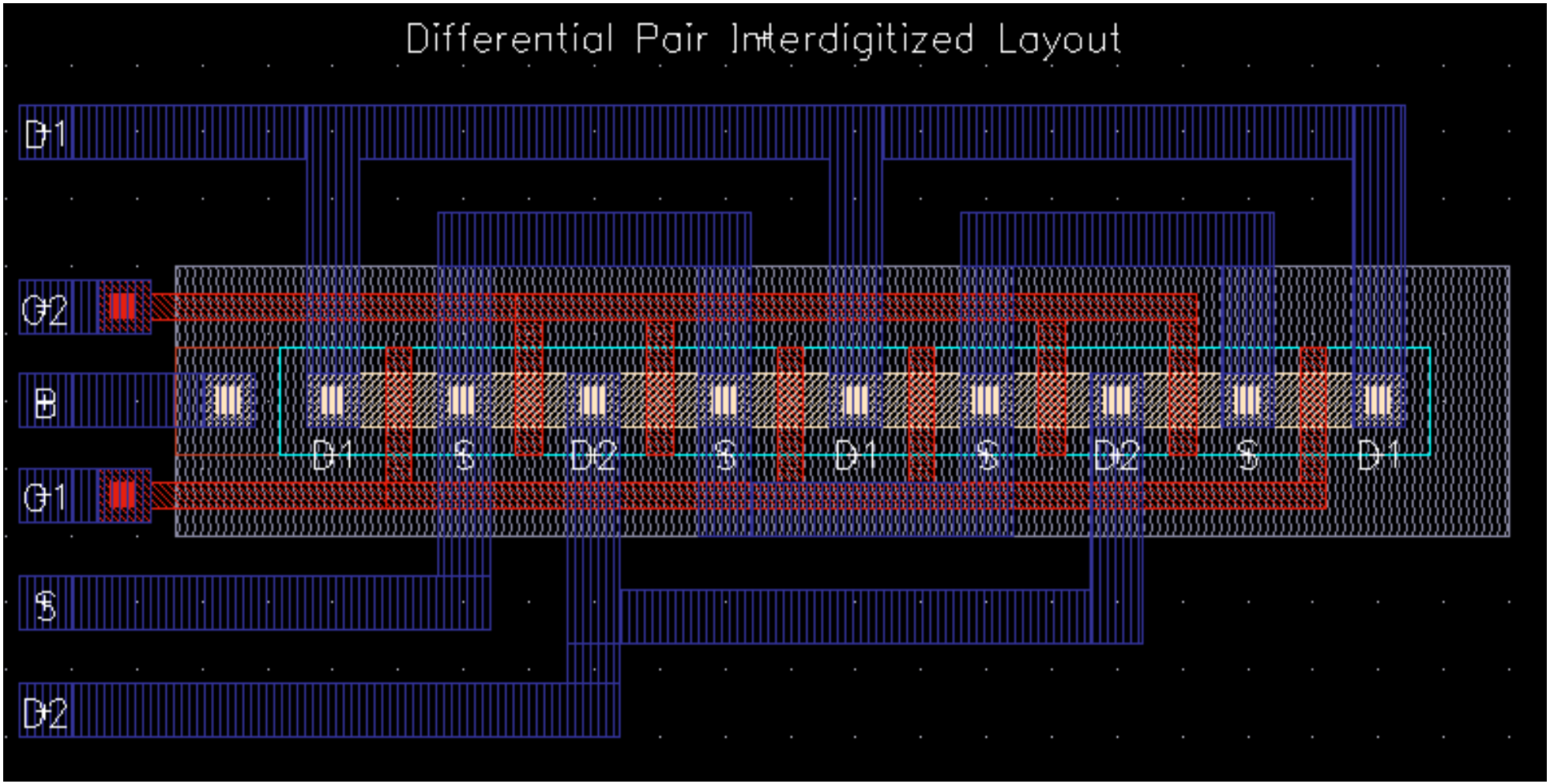


Differential pair requiring “matched transistors”

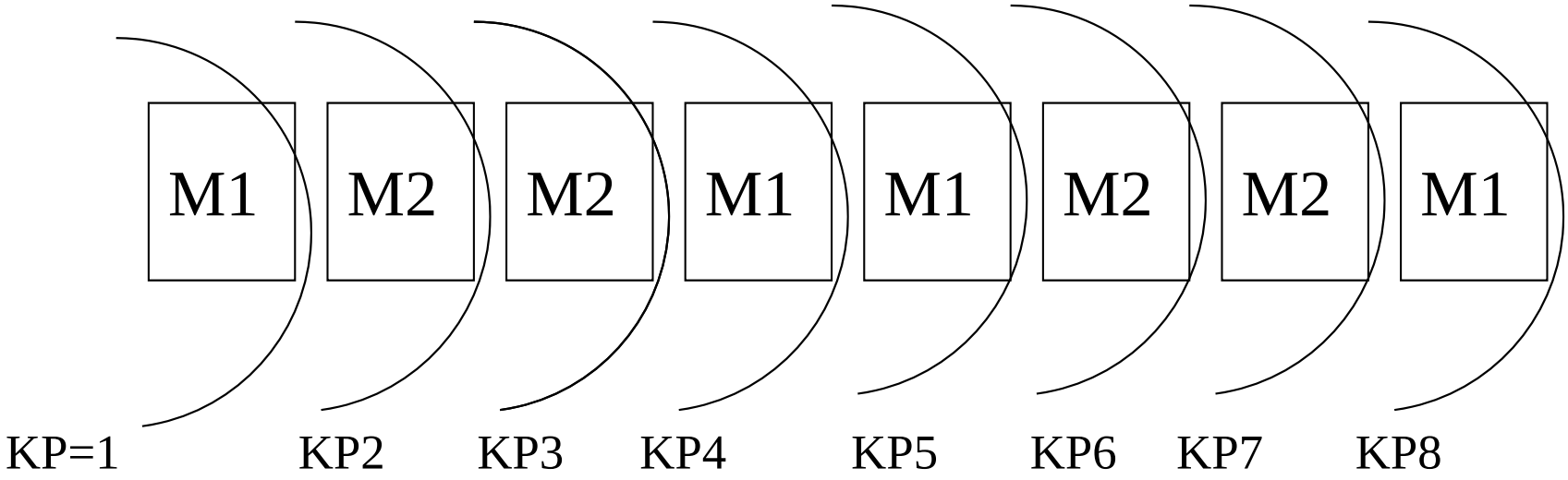


Interdigitized Layout

- Averages the process variations among transistors
- Common terminal is like a serpentine



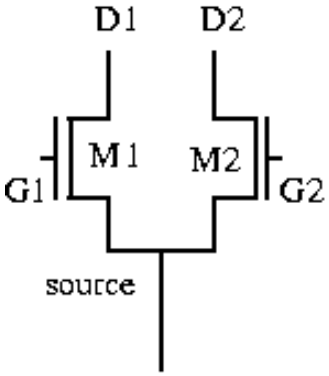
Why Interdigitized?

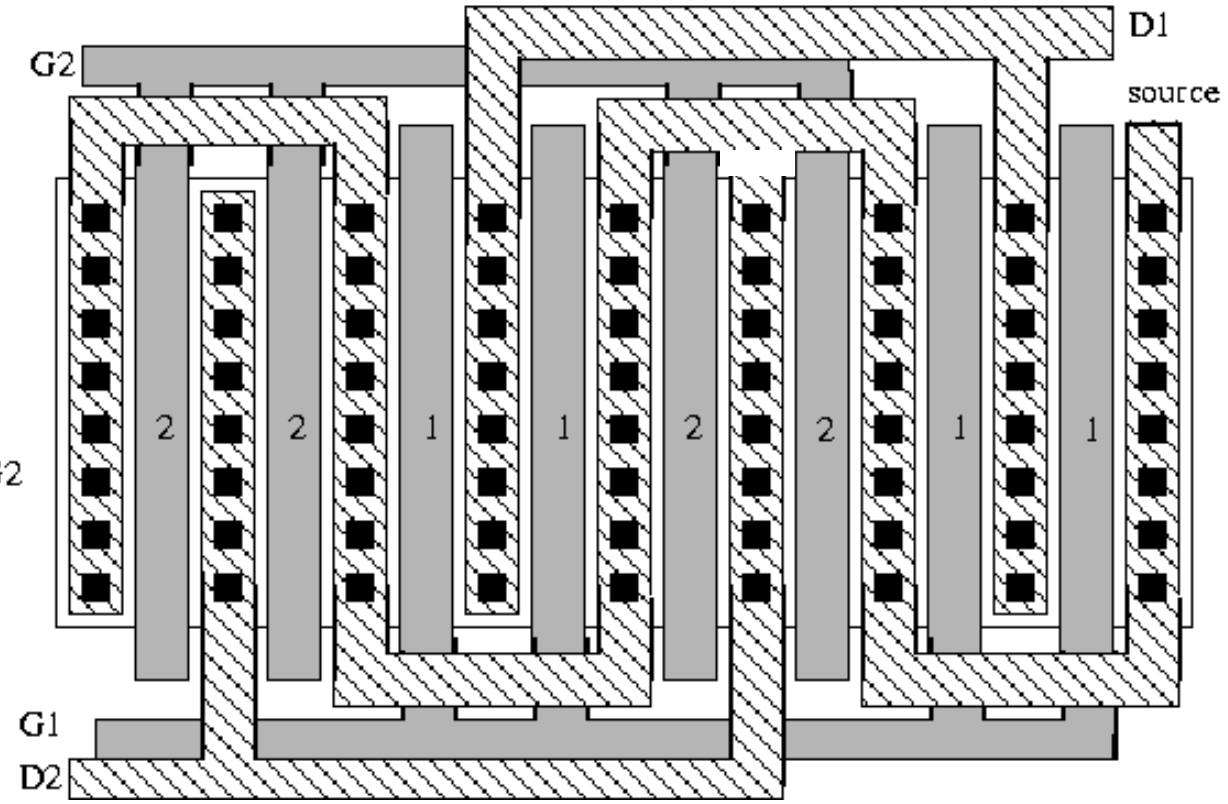


- Process variations are averaged among transistors
  KPs for M1:KP1+KP4+KP5+KP8 (Avg=4.5)
  M2:KP2+KP3+KP6+KP7 (Avg=4.5)
- Technique maybe good for matching dc conditions
- Uneven total drain area between M1 and M2. This is undesirable for ac conditions: capacitors and other parameters may not be equal
- A more robust approach is needed (Use dummies if needed !!)

A method of achieving better capacitive matching :

Using the previous slide values, we would have M2 with KP=3.5 and M1 with KP=5.5





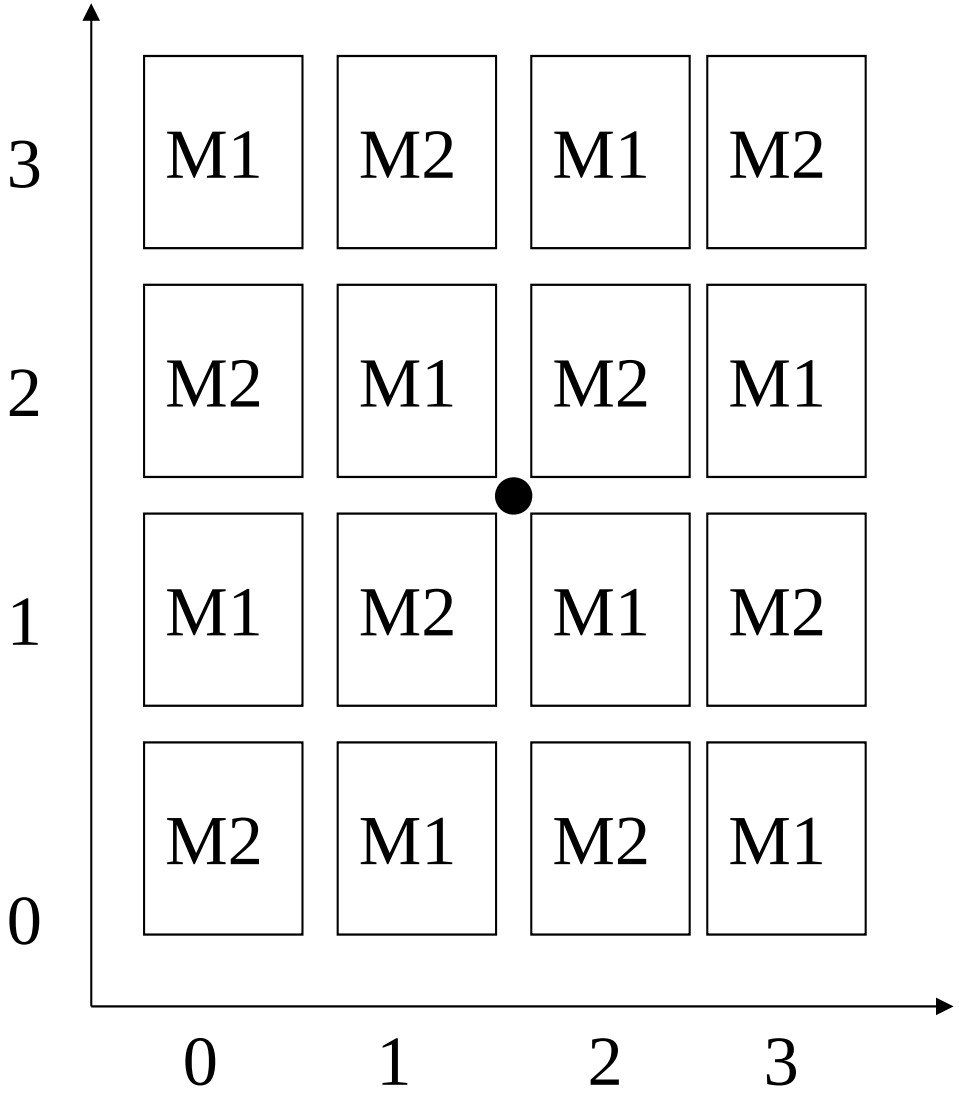
- Each transistor is split in four equal parts interleaved in two by two's.

So that for one pair of pieces of the same transistor we have currents flowing in opposite direction.

- Transistors have the same source and drain area and perimeters, but this topology is more susceptible to gradients (not common centroid)

Common Centroid Layouts

Usually routing is more complex



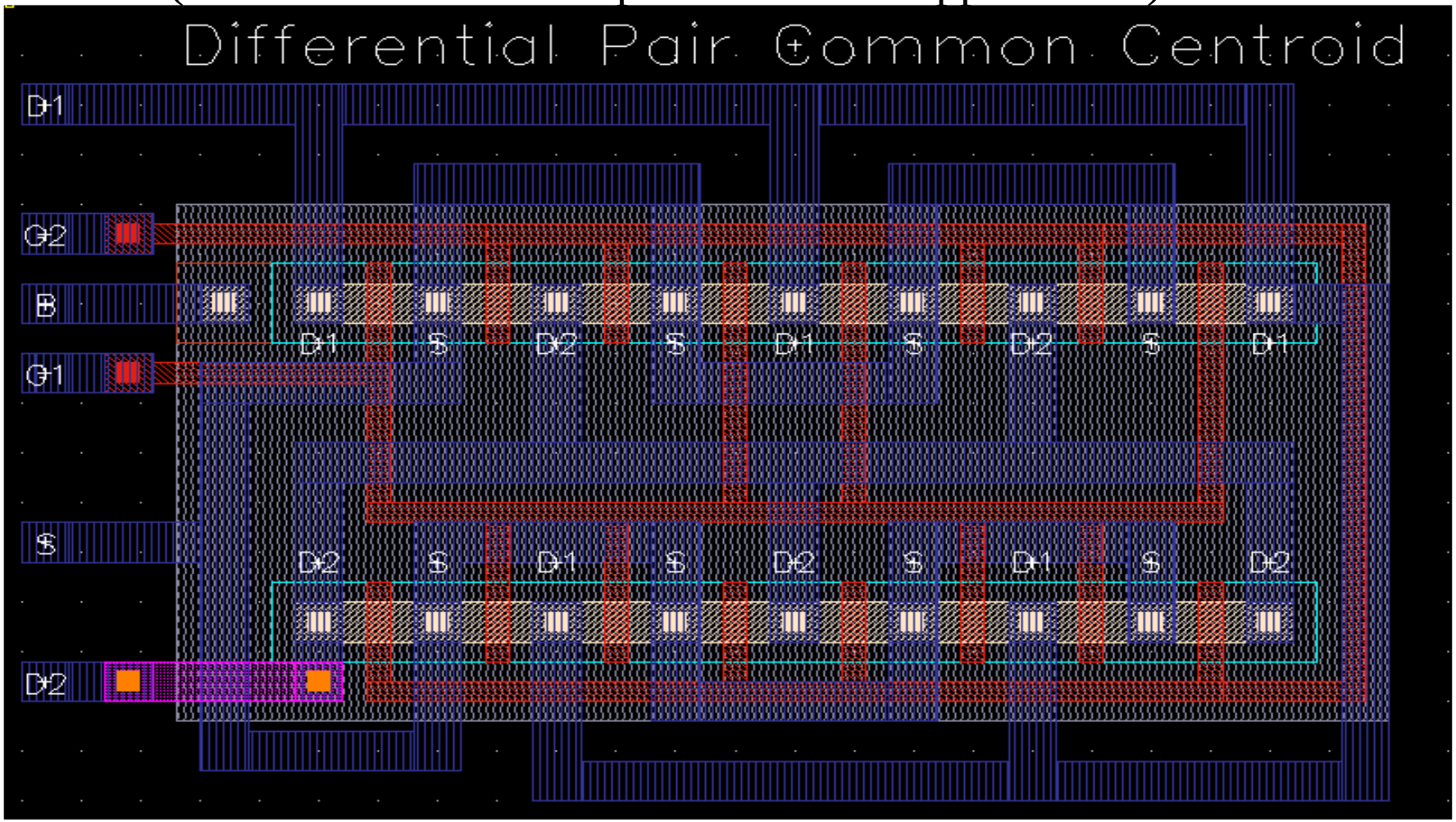
CENTROID
(complex layout)

M1: 8 transistors
(0,3) (0,1)
(1,2) (1,0)
(2,3) (2,1)
(3,2) (3,0)

M2: 8 transistors
(0,2) (0,0)
(1,3) (1,1
(2,2) (2,0)
(3,3) (3,1)

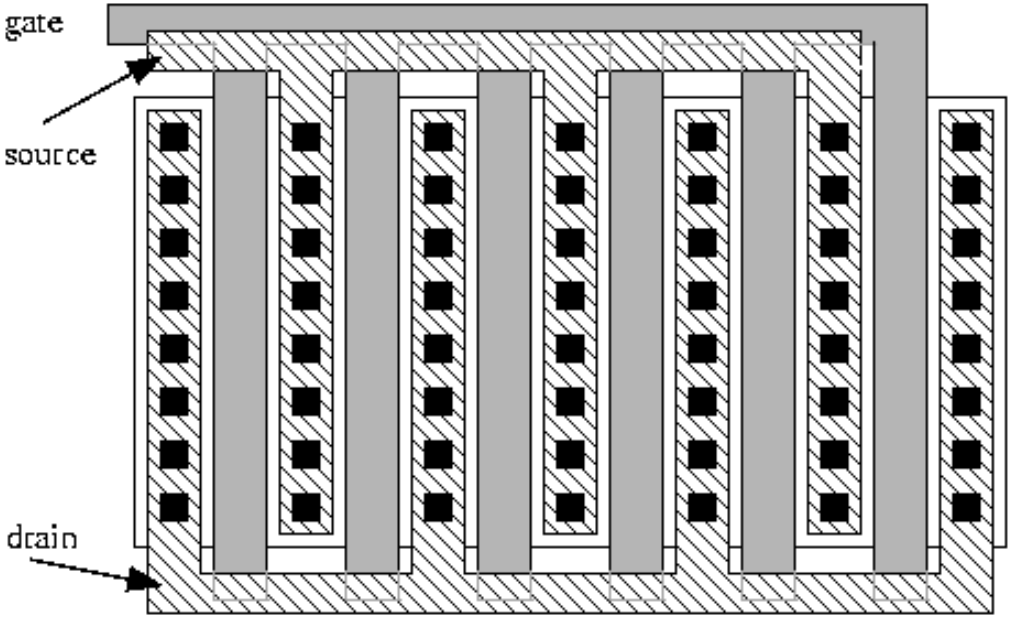
Common Centroid Layouts

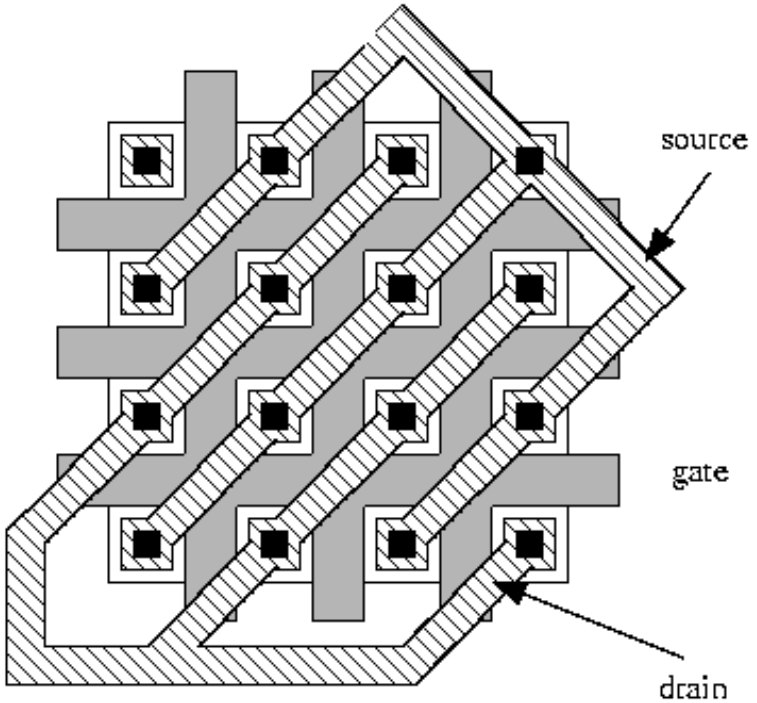
- Split into parallel connections of even parts
- Half of them will have the drain at the right side and half at the left
- Be careful how you route the common terminal
- Cross talk (effect of distributed capacitors ➔ RF applications)!



•Many contacts placed close to one another reduces series resistance and make the surface of metal connection smoother than when we use only one contact; this prevents microcraks in metal;

- Splitting the transistor in a number of equal part connected in parallel reduces the area of each transistor and so reduces further the parasitic capacitances, but accuracy might be degraded!

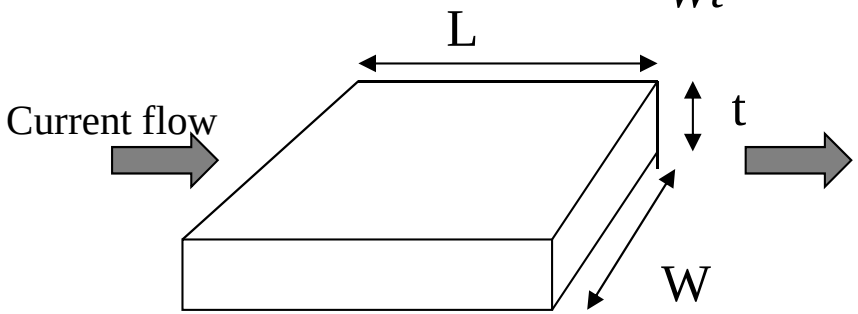




Integrated Resistors

- Highly resistive layers (p^+, n^+, well or polysilicon)
- R defines the resistance of a square of the layer
- Accuracy less than 30%

$$R = \rho \frac{L}{Wt}$$

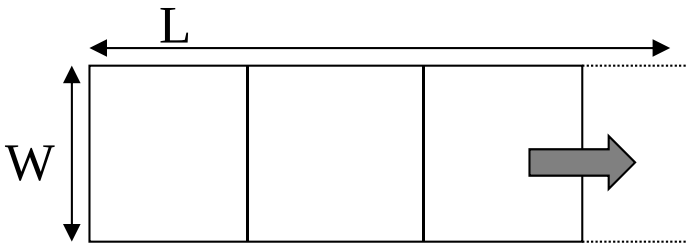


Resistivity (volumetric measure of material's resistive characteristic)

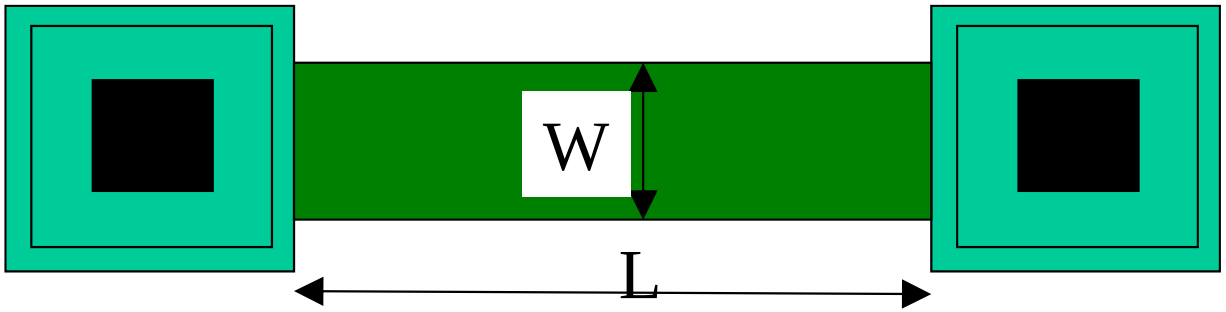
ρ (Ω-cm)

Sheet resistance (measure of the resistance of a uniform film with arbitrary thickness *t*

$R = \rho/t$ (Ω/)

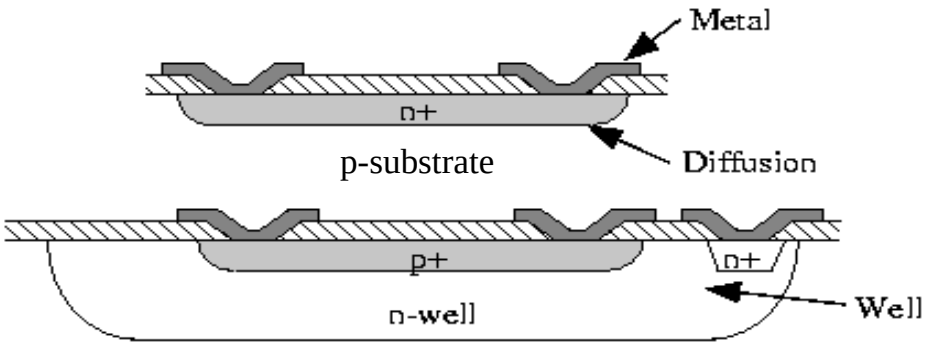


$$\#\,\text{Squares} = \frac{L}{W}$$



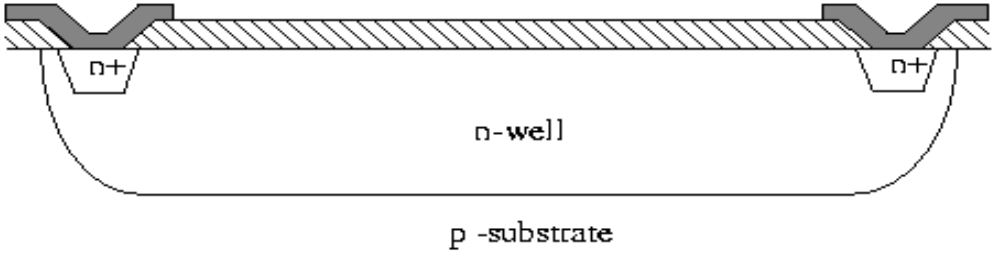
$$R = 2R_{contact} + (L/W)\,R$$

Diffusion/Well Resistors

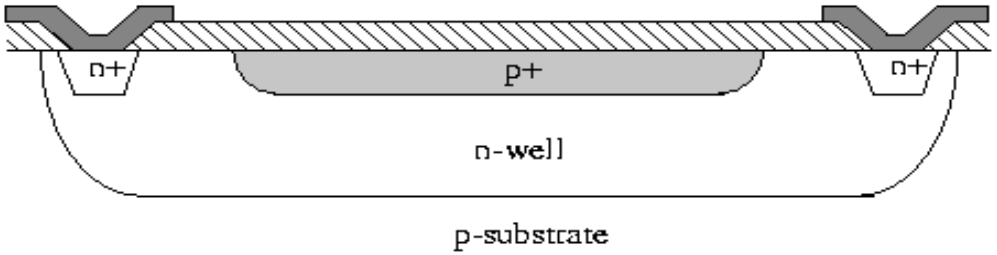


Diffused resistance

Diffused resistance

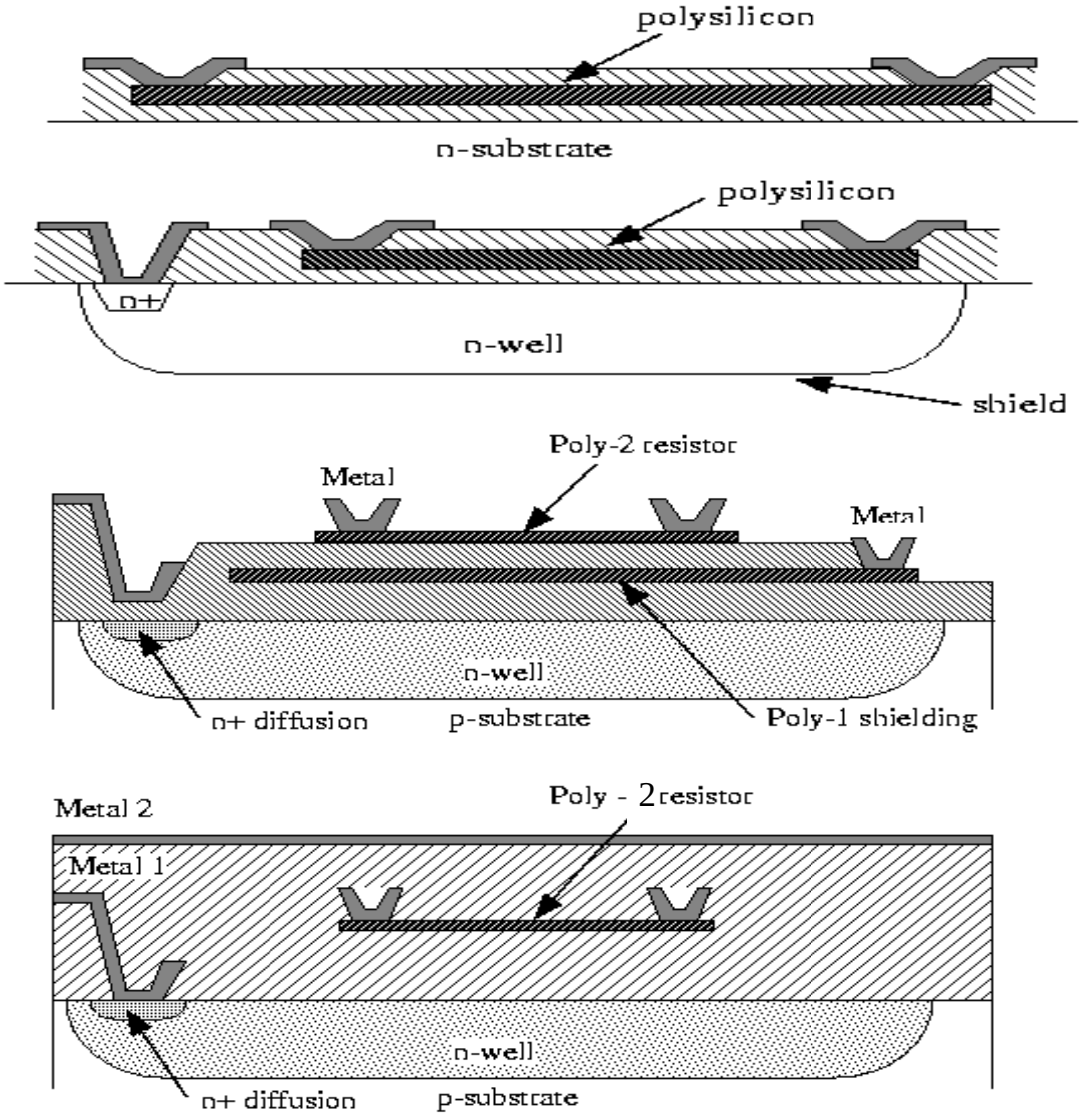


well resistance



Pinched n-well resistance

Poly Resistors



e) First polysilicon resistance

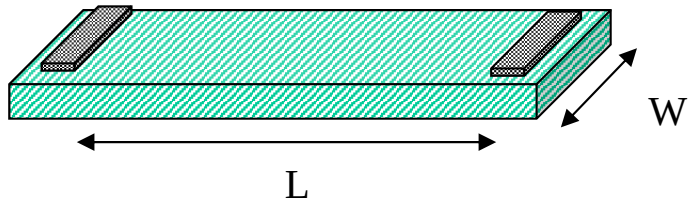
f) First polysilicon resistance with a well shielding

g) Second polysilicon resistance

h) Second polysilicon resistance with a well shielding

TYPICAL INTEGRATED RESISTORS

$$R = 2R_{cont} + \frac{L}{W} R_{\square}$$



Type of layer	Sheet Resistance W/0	Accuracy %	Temperature Coefficient ppm/°C	Voltage Coefficient ppm/V
n + diff	30 - 50	20 - 40	200 - 1K	50 - 300
p + diff	50 -150	20 - 40	200 - 1K	50 - 300
n - well	2K - 4K	15 - 30	5K	10K
p - well	3K - 6K	15 - 30	5K	10K
pinched n - well	6K - 10K	25 - 40	10K	20K
pinched p - well	9K - 13K	25 - 40	10K	20K
first poly	20 - 40	25 - 40	500 - 1500	20 - 200
second poly	15 - 40	25 - 40	500 - 1500	20 - 200

Special poly sheet resistance for some analog processes might be as high as 1.2 KΩ/

Large Resistors

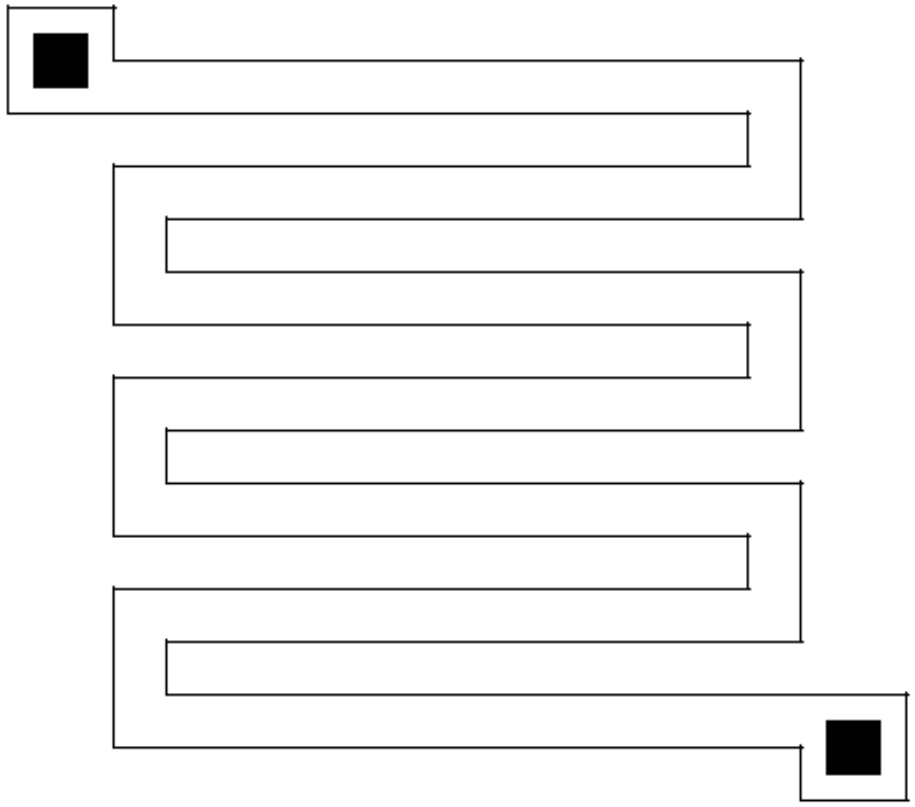
In order to implement large resistors :

- Use long strips (large L/W)
- Use layers with high sheet resistance (bad performances – see previous table)
  - High temperature coefficient and non-linearityt

Layout : rectangular “serpentine”

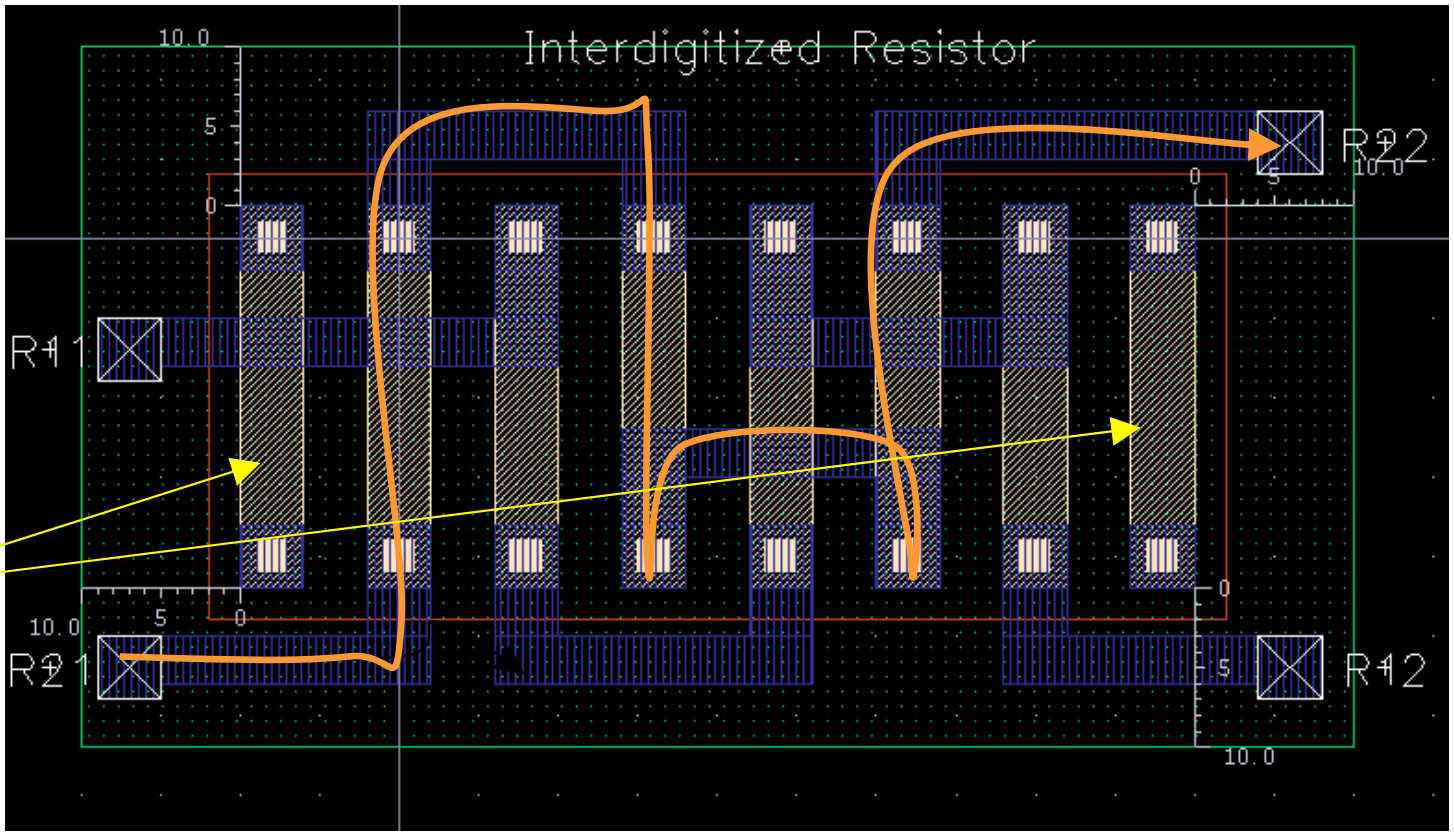
$$R = \frac{L}{W} R_{\square} = \frac{L}{W} \cdot \frac{\bar{\rho}}{x_j}$$

- Estimating the resistance in the corners can be difficult



Well-Diffusion Resistor

- Example shows two long resistors for KΩ range
- Alternatively, “serpentine” shapes can be used
- Noise problems from the body
  - Substrate bias surrounding the well
  - Substrate bias between the parallel strips



Dummies

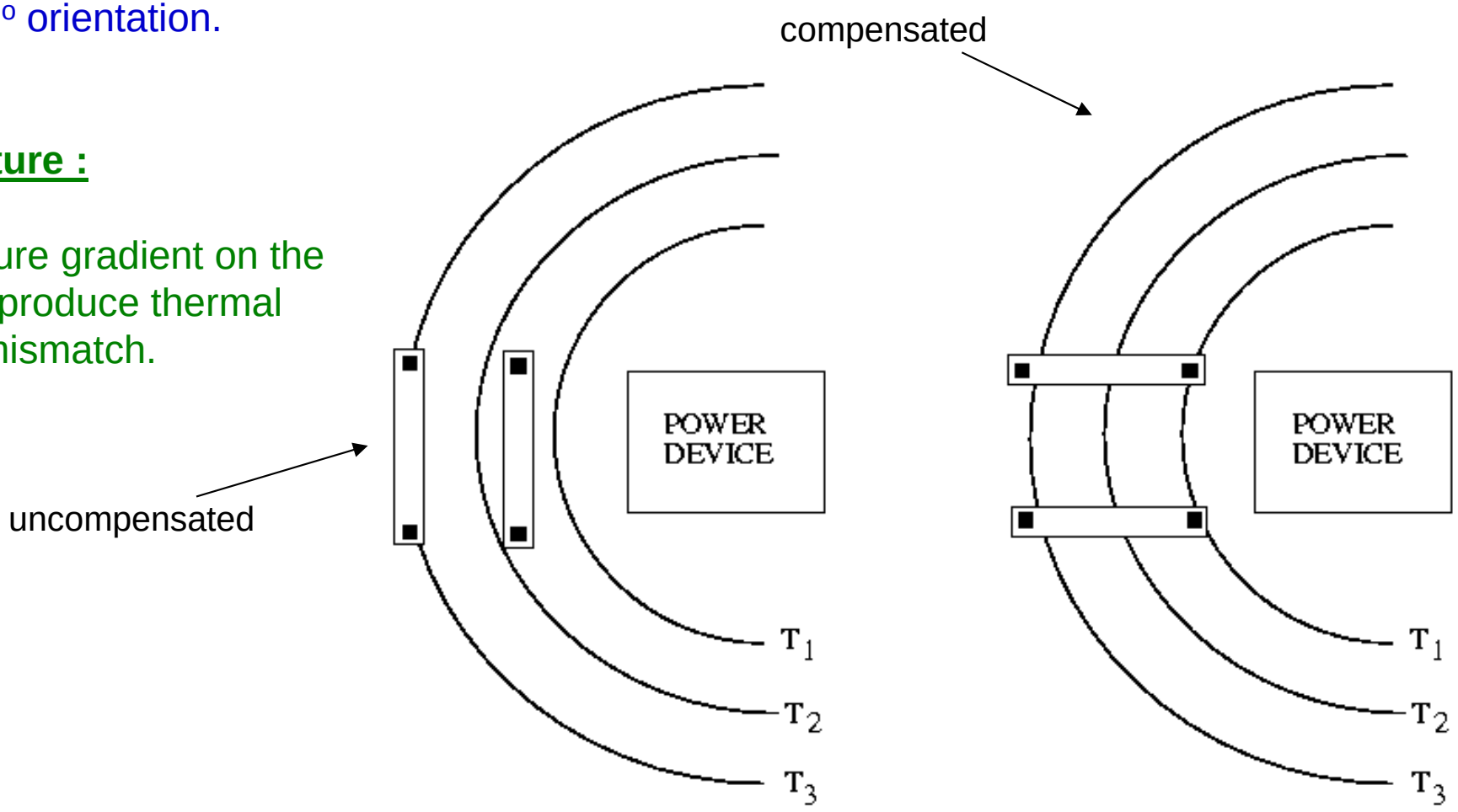
Factors affecting accuracy :

Plastic packages cause a large pressure on the die (= 800 Atm.). It determines a variation of the resistivity.

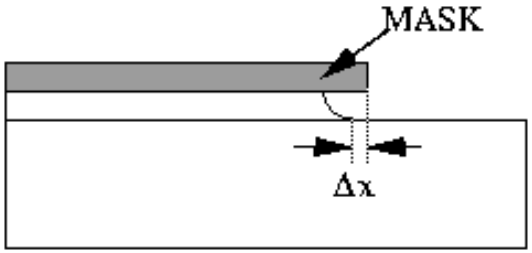
For <100> material the variation is unisotropic, so the minimum is obtained if the resistance have a 45^{o} orientation.

Temperature :

Temperature gradient on the chip may produce thermal induced mismatch.



Etching



Wet etching : isotropic (undercut effect)

HF for SiO_2 ; H_3PO_4 for Al

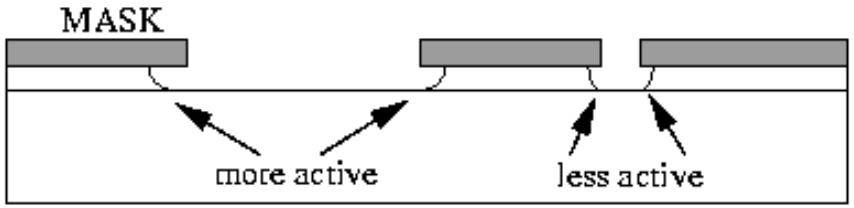
Δx for polysilicon may be 0.2 – 0.4 μm with standard deviation 0.04 – 0.08 μm.

Reactive ion etching (R.I.E.)(plasma etching associated to "bombardment") : anisotropic.

Δx for polysilicon is 0.05 μm with standard deviation 0.01 μm

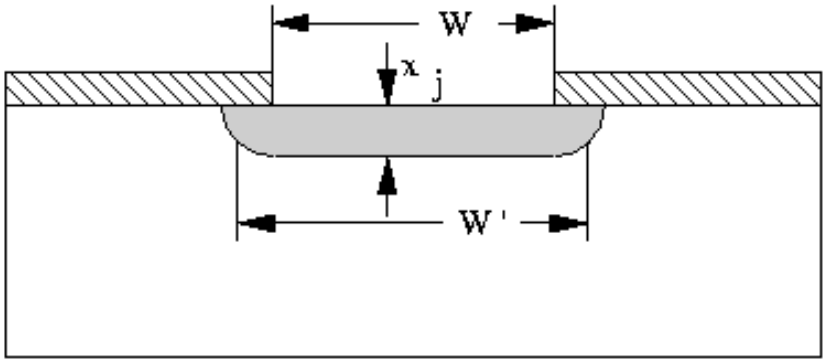
Boundary :

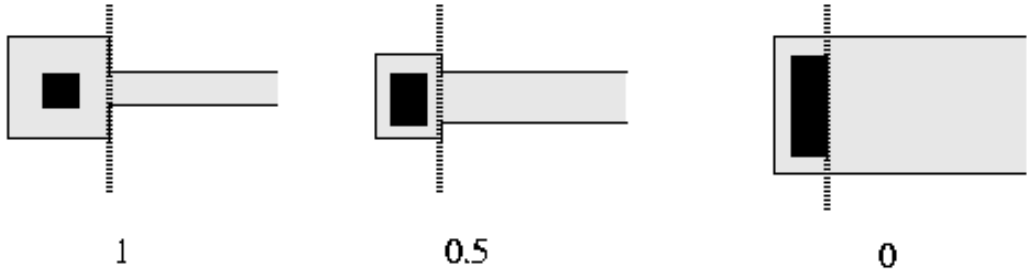
The etching depends on the boundary conditions



- **Use dummy strips**

Side diffusion effect : Contribution of endings

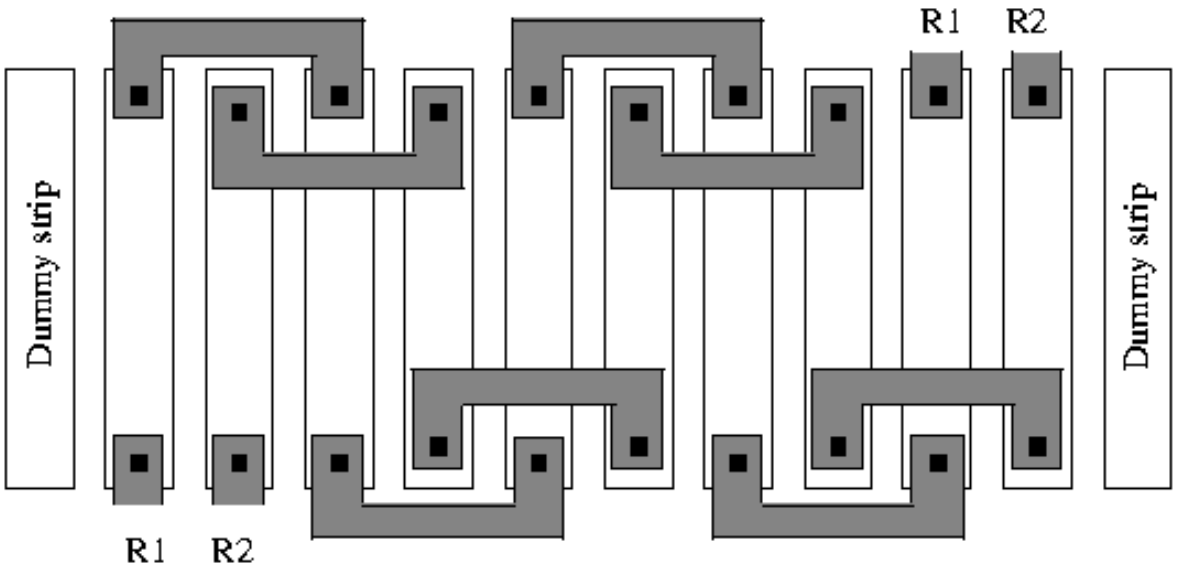




Side Diffusion "widens" R
$R_{\square}$ is not constant with W

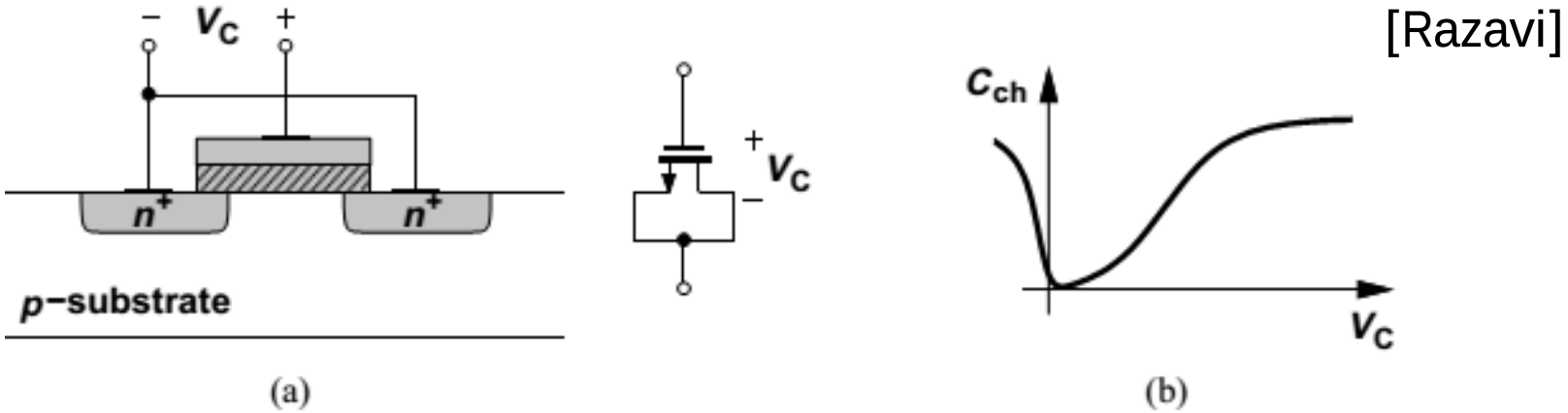
Impact of R_{cont} depends on relative geometry
Best to always use a resistor W that is at least as large as the contact

Interdigitized structure :



MOS Capacitors

[Razavi]

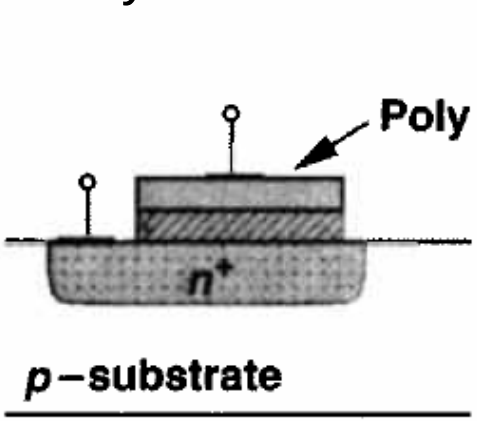


(a) MOSFET configured as a capacitor, (b) nonlinear C/V characteristic.

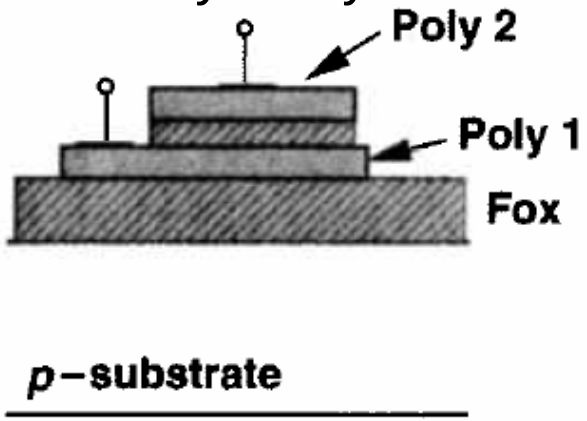
- One of the most dense capacitors available (fF/um^2)
- Often used to de-couple DC power supply and bias signals
- Capacitor non-linearity can be important if used in the signal path

Integrated Capacitors

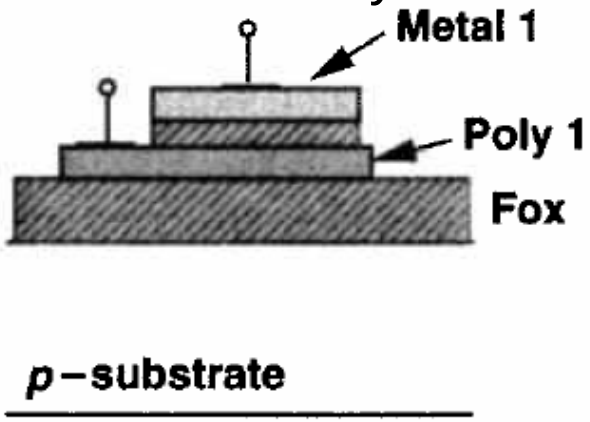
Poly - Diffusion



Poly - Poly

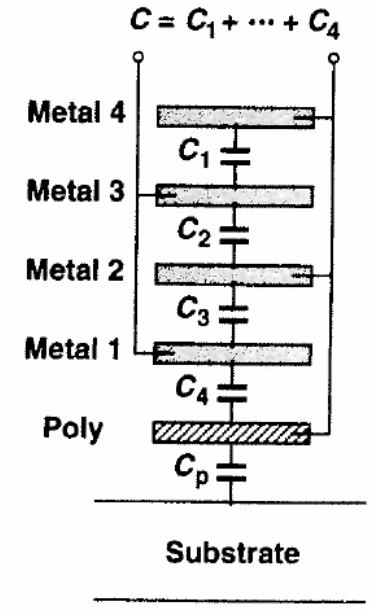


Metal1 - Poly

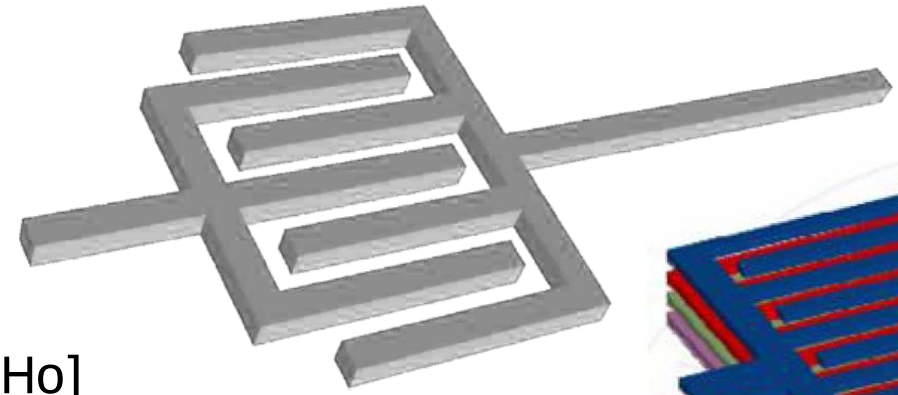


[Razavi]

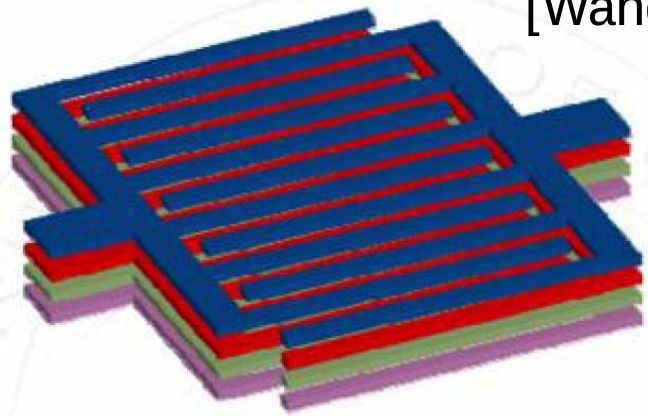
Vertical Metal “Sandwich”



Lateral Metal-Oxide-Metal (MOM)

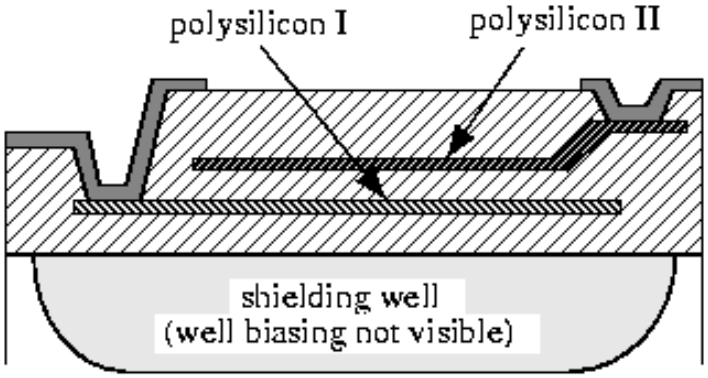


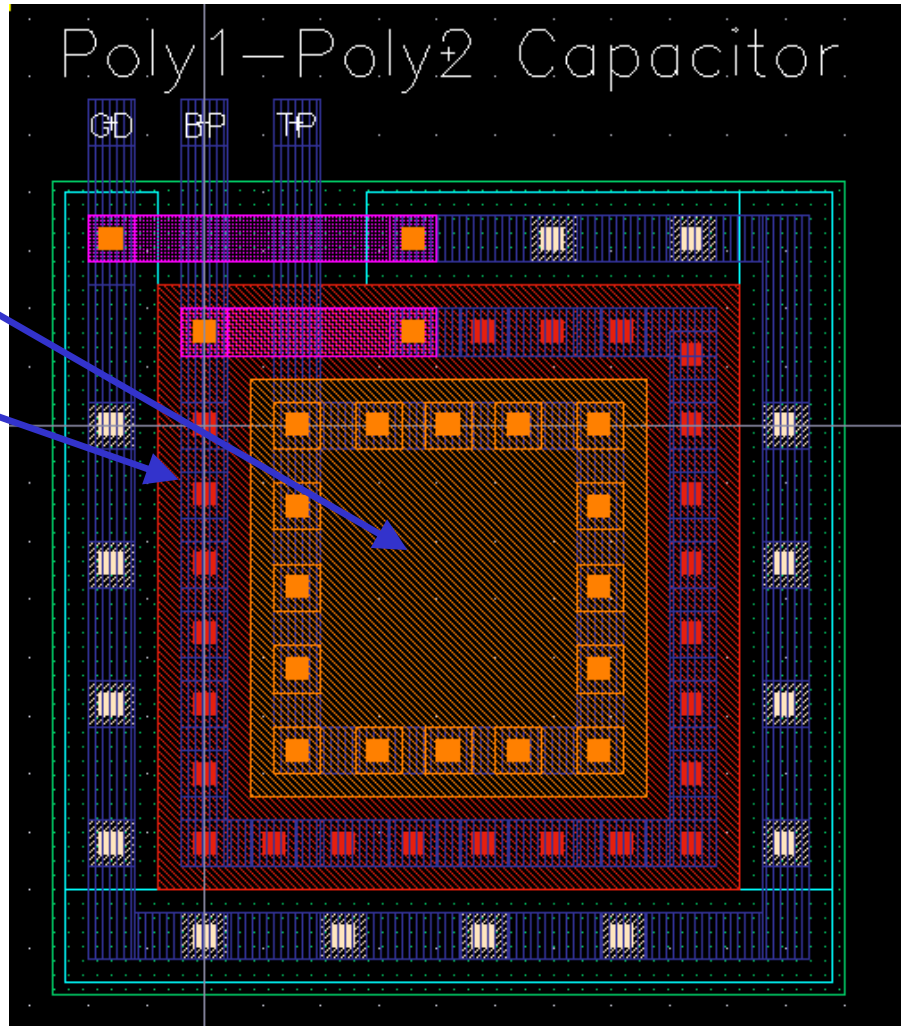
[Ho]



[Wang]

Poly1 - Poly2 Capacitor





- Area is determined by poly2
- Problems
  - undercut effects
  - nonuniform dielectric thickness
  - matching among capacitors

Factor affecting RELATIVE accuracy/matching

- Oxide damage
- Impurities
- Bias condition
- Bias history (for CVD)
- Stress
- Temperature

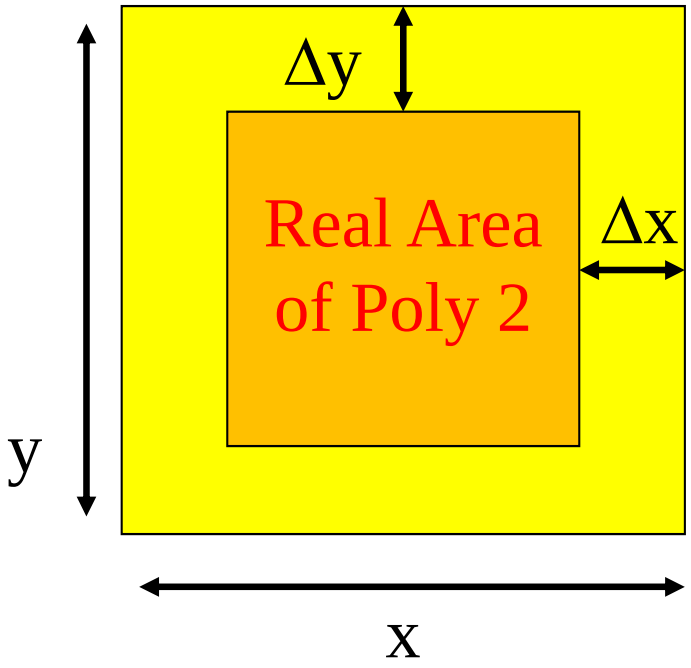
$$\left(\frac{\Delta\varepsilon_{ox}}{\varepsilon_{ox}}\right)$$

- Grow rate
- Poly grain size

$$\left(\frac{\Delta t_{ox}}{t_{ox}}\right)$$

- Etching
- Alignment

$$\left(\frac{\Delta L}{L}\right);\left(\frac{\Delta W}{W}\right)$$



$$\frac{\Delta C}{C} \approx 1 - 0.1\%$$

Note, the absolute C may vary as high as 20% due to process variations

$$\left(\frac{\Delta C}{C}\right)^2 = \left(\frac{\Delta\varepsilon_r}{\varepsilon_r}\right)^2 + \left(\frac{\Delta t_{ox}}{t_{ox}}\right)^2 + \left(\frac{\Delta L}{L}\right)^2 + \left(\frac{\Delta W}{W}\right)^2$$

Accuracy of integrated capacitors

Perimeter imperfections effect the total capacitance:

$C = C_A A$

$A = (x-2\Delta x)(y- 2\Delta y)$

$= xy - 2x\Delta y - 2y\Delta x + 4\Delta x\, \Delta y$

Assuming that $\Delta x = \Delta y = \Delta e$

$A = xy - 2\Delta e(x + y) + 4(\Delta e)^2$

$A \approx xy - 2\Delta e(x + y)$

$\therefore C_e = - 2\Delta e(x + y)$

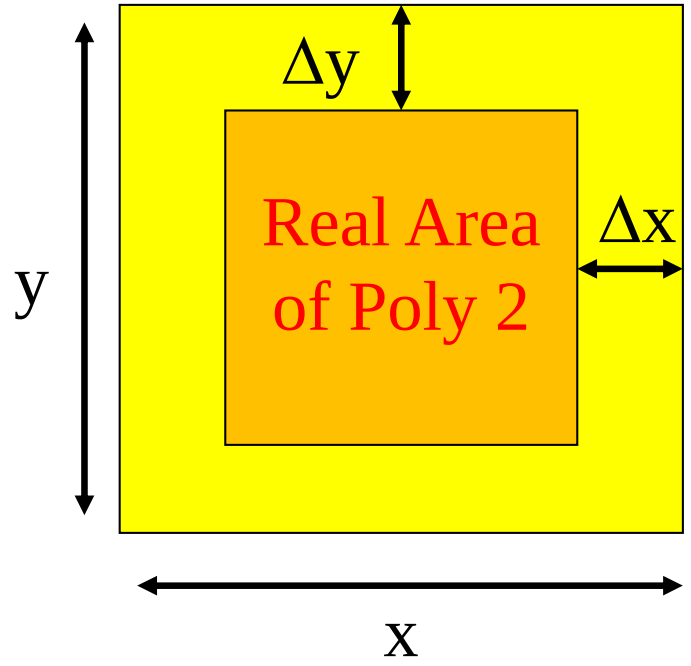
The relative error is

$\varepsilon = C_e/C$

$= -2\Delta e(x + y) / xy$

Then maximize the area and minimize the perimeter ➔ use squares!!!

C_A = capacitance per unit area

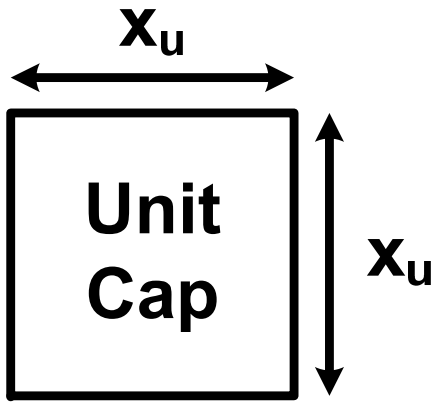


Capacitor Matching

- If we want to match the ratio of two caps C_1 and C_2

$$\frac{C_1}{C_2} = \frac{C_{1,ideal}(1+e_1)}{C_{2,ideal}(1+e_2)}$$

- To minimize the error in the cap ratio, we need to have $e_1=e_2$. This implies that the Perimeter/Area should be equal.
- Generally, we break up both caps C_1 and C_2 into square unit caps, C_u



$$A_u = x_u^2$$

Capacitor Matching

- If both C_1 and C_2 are integer multiples of C_u, then simply use I_1 unit caps for C_1 and I_2 unit caps for C_2

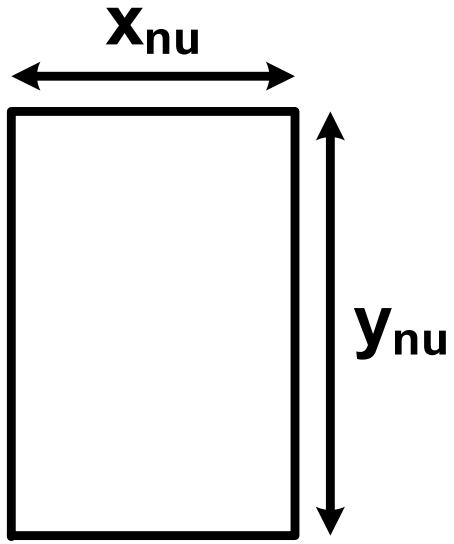
$$\frac{C_1}{C_2} = \frac{I_1 C_u}{I_2 C_u}$$

- If $C_1 = I_1 C_u$ and $C_2 = I_2 C_u + (1+f)C_u$, where f is a fraction, then we want the non-unit cap, $C_{nu} = (1+f)C_u$, to have equal $\frac{\text{Perimeter}}{\text{Area}}$ as a unit cap.
- Why is the non-unit cap $(1+f)C_u$?

  Because we don't want a cap smaller than the unit cap, or bigger than $2C_u$. Overall, we want to use as many unit caps as possible, but none smaller than C_u.

Capacitor Matching

- How to size C_{nu}?



Define $N = 1 + f = \frac{A_{nu}}{A_u} = \frac{x_{nu} y_{nu}}{x_u^2}$

For matching $\frac{P_{nu}}{A_{nu}} = \frac{P_u}{A_u}$

$$\frac{P_{nu}}{P_u} = \frac{A_{nu}}{A_u} = N = \frac{2(x_{nu} + y_{nu})}{4x_u}$$

$$x_{nu} + y_{nu} = 2Nx_u$$

From N definition $\Rightarrow$ $\boxed{x_{nu} = \frac{Nx_u^2}{y_{nu}}}$

Plugging this into the previous expression, we can solve for y_{nu}

$$y_{nu}^2 - 2Nx_u y_{nu} + Nx_u^2 = 0$$

$$\boxed{y_{nu} = x_u\left(N \pm \sqrt{N^2 - N}\right)}$$

If you want $y_{nu} > x_{nu}$ choose "+", $y_{nu} < x_{nu}$ choose "-"

Capacitor Matching

- If $C_1 = I_1 C_u + (1+ f_1) C_u$ and $C_2 = I_2 C_u + (1+ f_2) C_u$
  where $N_1 = 1+ f_1$ and $N_2 = 1+ f_2$

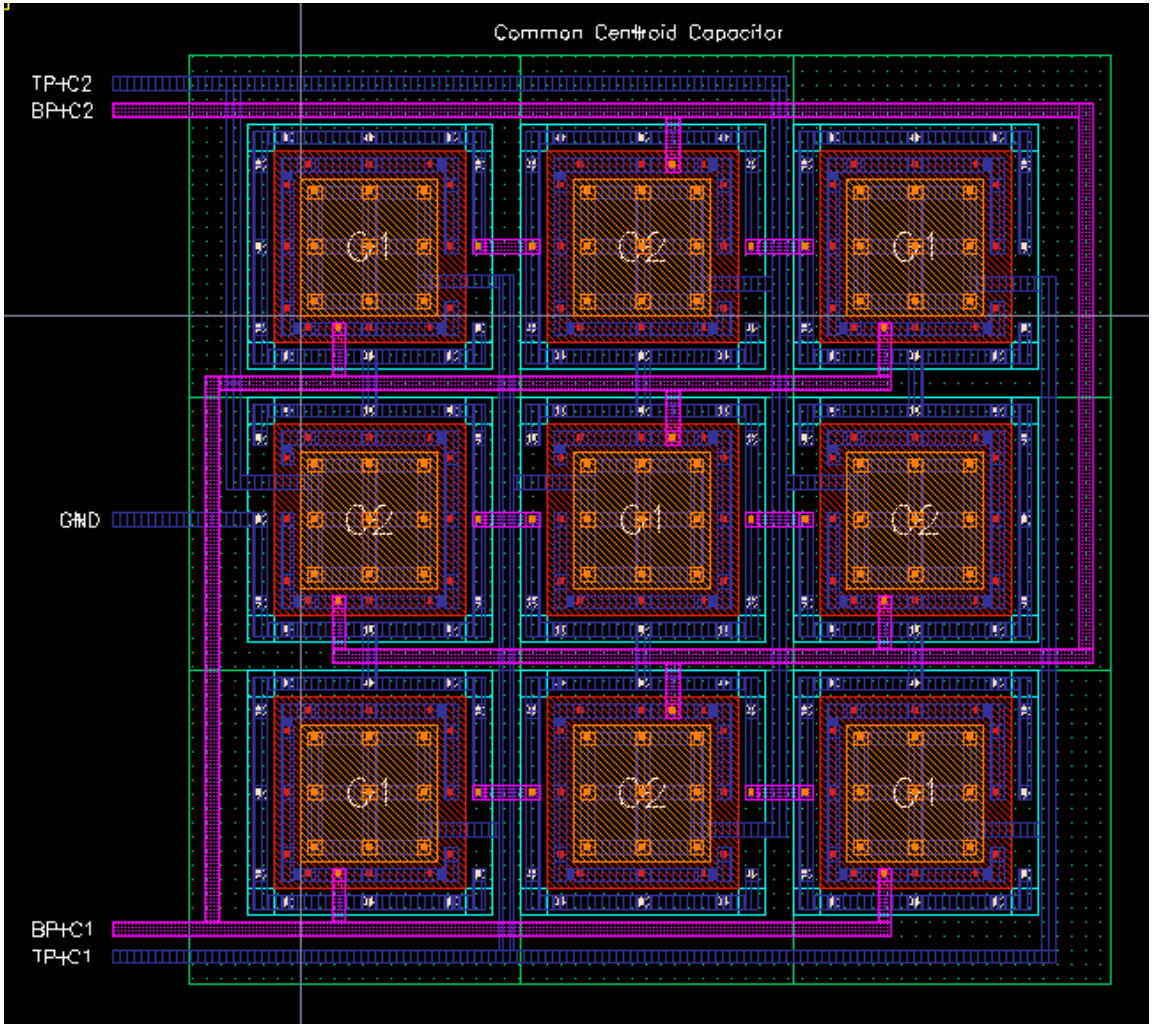
$$x_{nu1} = \frac{N_1 x_u^2}{y_{nu1}} \qquad x_{nu2} = \frac{N_2 x_u^2}{y_{nu2}}$$

$$y_{nu1} = x_u \left(N_1 \pm \sqrt{N_1^2 - N_1} \right) \qquad y_{nu2} = x_u \left(N_2 \pm \sqrt{N_2^2 - N_2} \right)$$

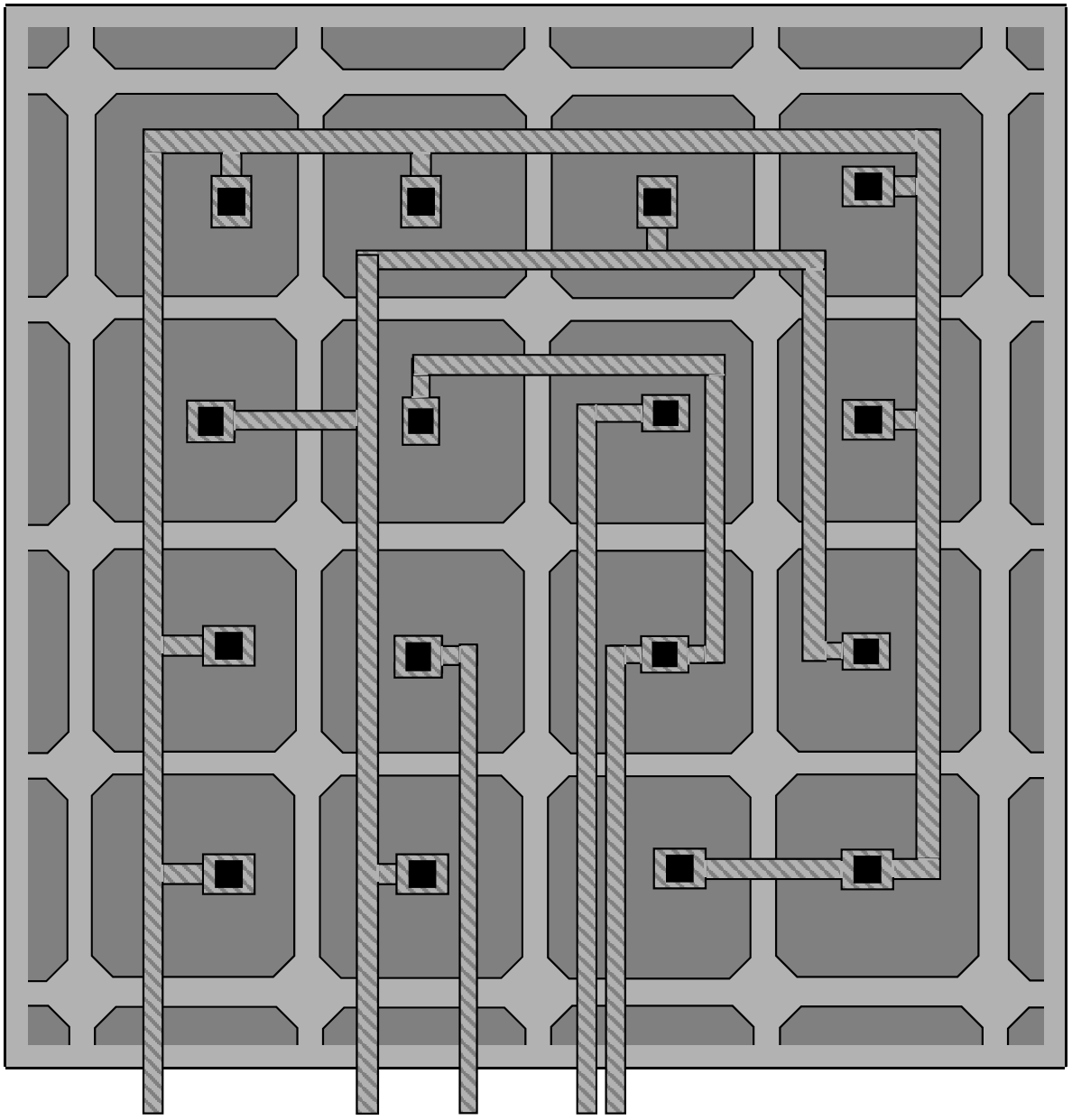
- Although, generally we have the flexibility to size C_u to set
  $C_1 = I_1 C_u$

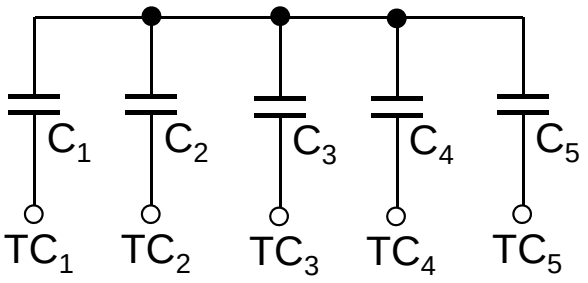
Common Centroid Capacitor Layout

- Unit capacitors are connected in parallel to form a larger capacitance
- Typically the ratio among capacitors is what matters
- The error in one capacitor is proportional to perimeter-area ratio
- Use dummies for better matching (See Razavi Book, page 752)



Approximate Common Centroid Structure



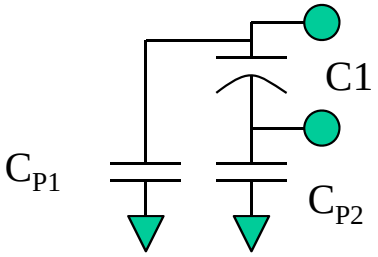


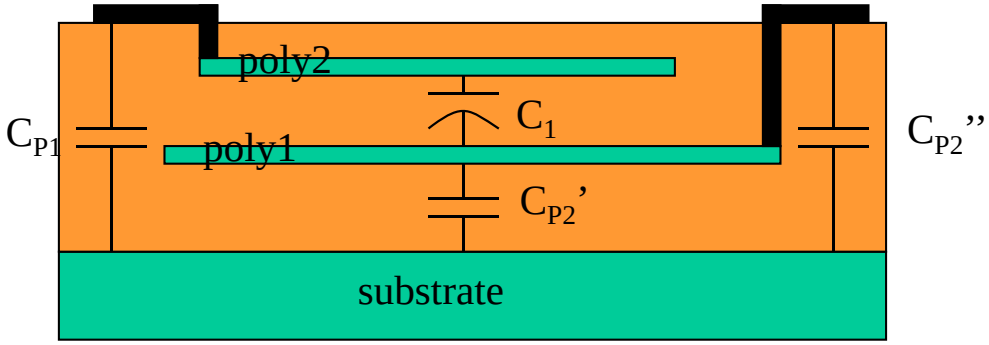
$C_2 = C_1$
$C_3 = 2C_1$
$C_4 = 4C_1$
$C_5 = 8C_1$

"Floating" Capacitors

Be aware of parasitic capacitors

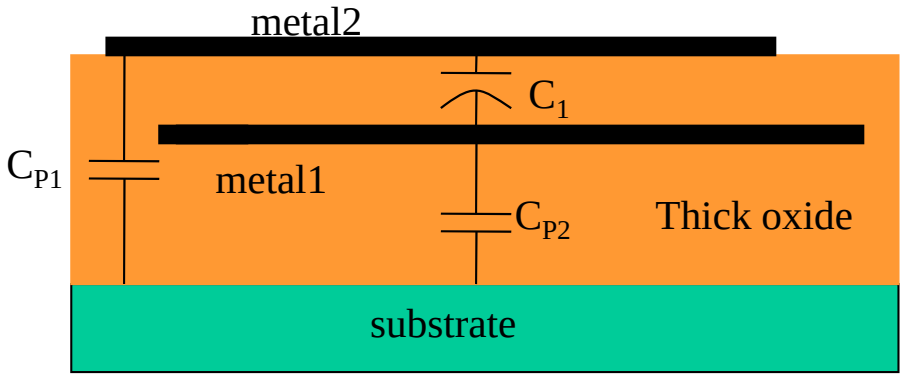
Polysilicon-Polysilicon: Bottom plate capacitance is comparable (10-30 %) with the poly-poly capacitance





CP1, CP2'' are very small (1-5 % of C1)
CP2' is around 10-50 % of C1

➔**Metal1-Metal2: More clean, but the capacitance per micrometer square is smaller.** Good option for very high frequency applications (C~ 0.1-0.3 pF).



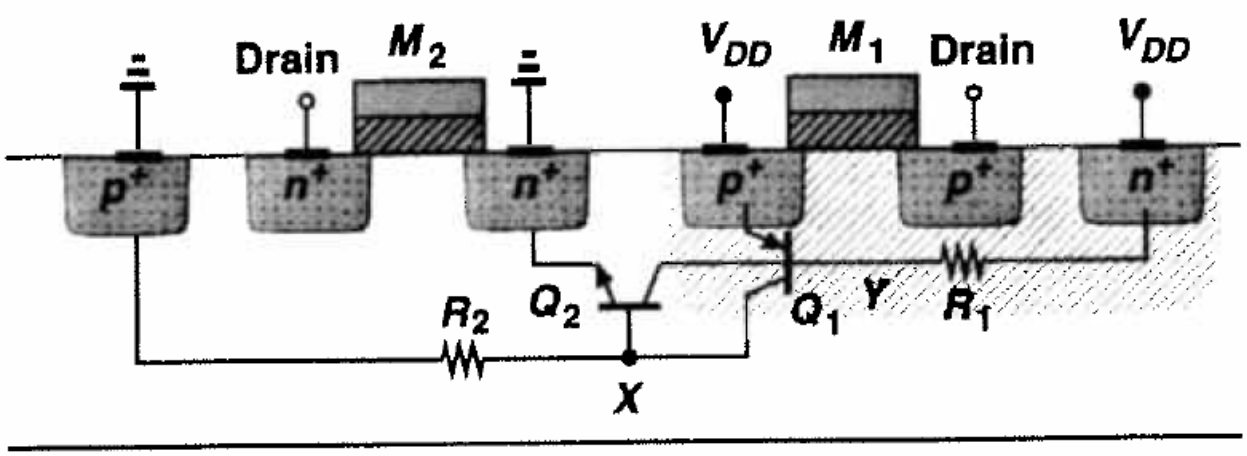
CP2 is very small (1-5 % of C1)

Analog Cell Layout Key Points

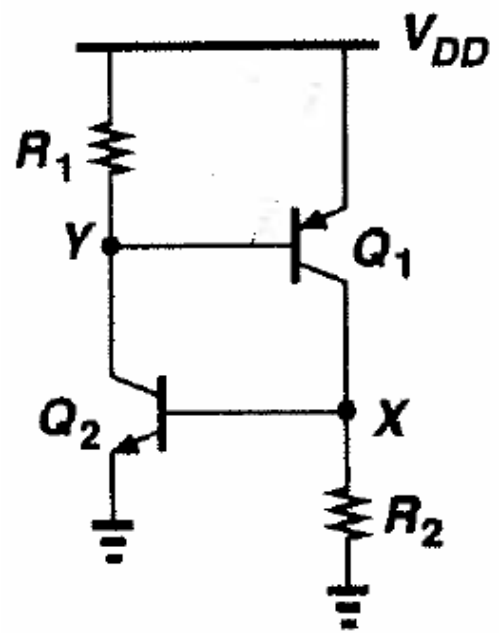
- Use transistors with the same orientation
- Minimize S/D contact area by stacking transistors (to reduce parasitic capacitance to substrate)
- Respect symmetries
- Use low resistive paths when current needs to be carried (to avoid parasitic voltage drops)
- Shield critical nodes (to avoid undesired noise injection)
- Include guard rings everywhere; e.g. Substrate/well should not have regions larger than 50 um without guard protections (latchup issues)

Bipolar Transistors – Latchup

[Razavi]



Equivalent Circuit

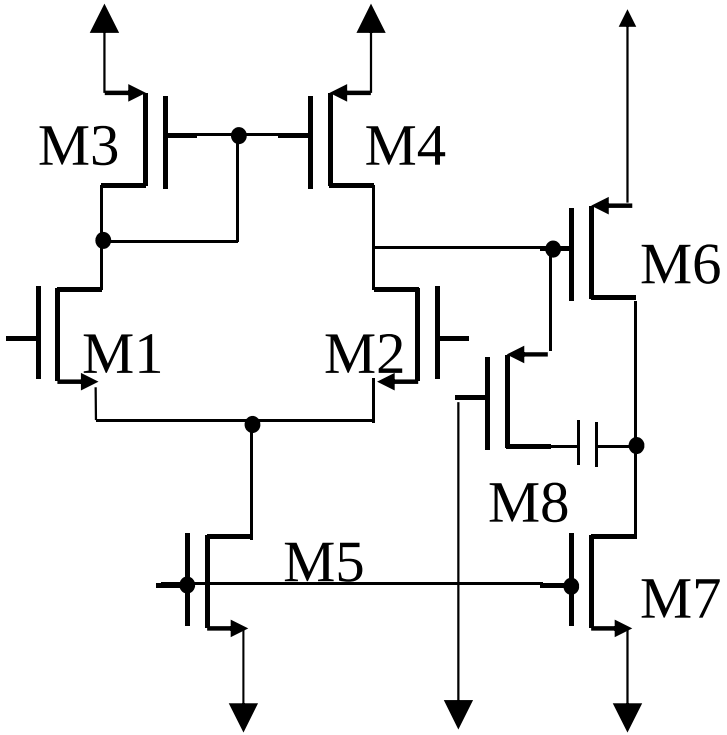


- Potential for parasitic BJTs (Vertical PNP and Lateral NPN) to form a positive feedback loop circuit
- If circuit is triggered, due to current injected into substrate, then a large current can be drawn through the circuit and cause damage
- Important to minimize substrate and well resistance with many contacts/guard rings

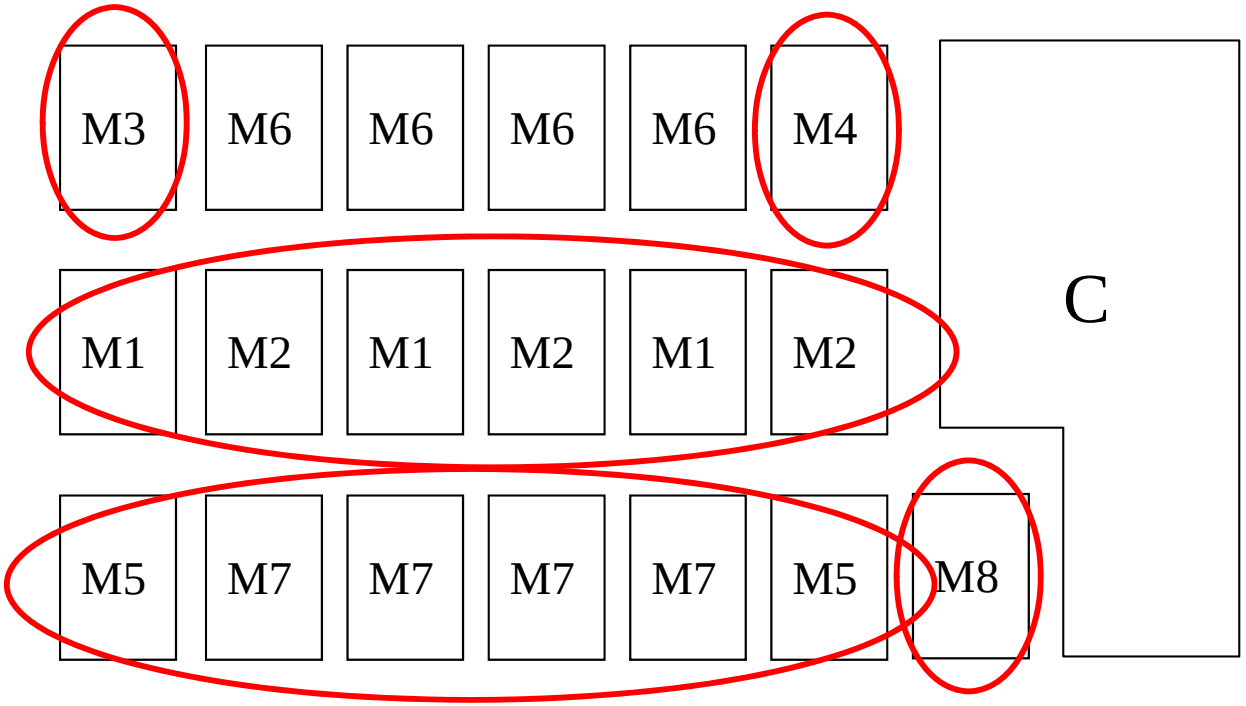
Stacked Layout for Analog Cells

- Stack of elements with the same width
- Transistors with even number of parts have the source (drain) on both sides of the stack
- Transistors with odd number of parts have the source on one end and the drain on the other. If matching is critical use dummies
- If different transistors share a same node they can be combined in the same stack to share the area of the same node (less parasitics)
- Use superimposed or side by side stacks to integrate the cell

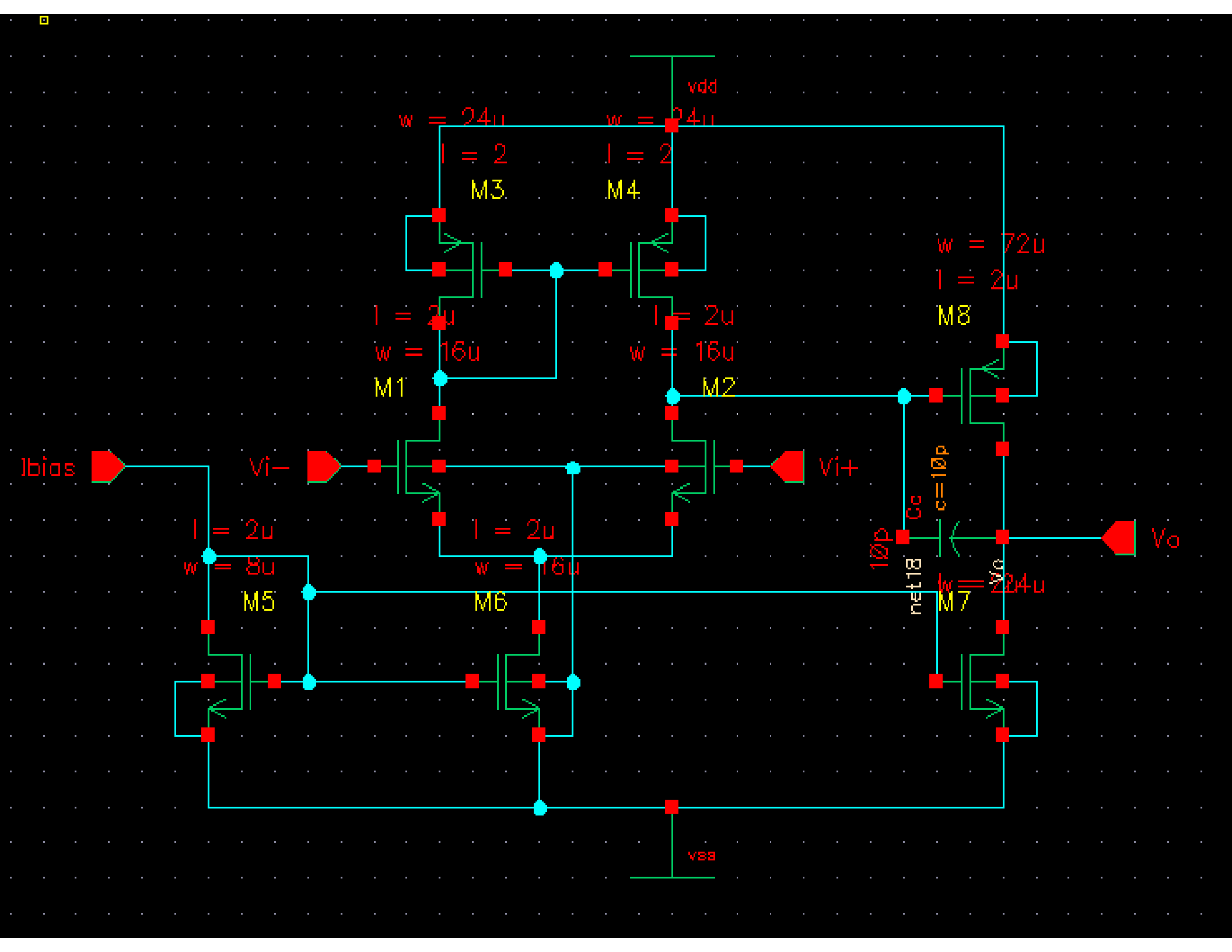
- M1 and M2 must match. Layout is interdigitized
- M3 and M4 must match. M6 must be wider by 4*M3
- M7 must be 2*M5
- Layout is an interconnection of 3 stacks; 2 for NMOS and 1 for PMOS
- Capacitor made by poly-poly

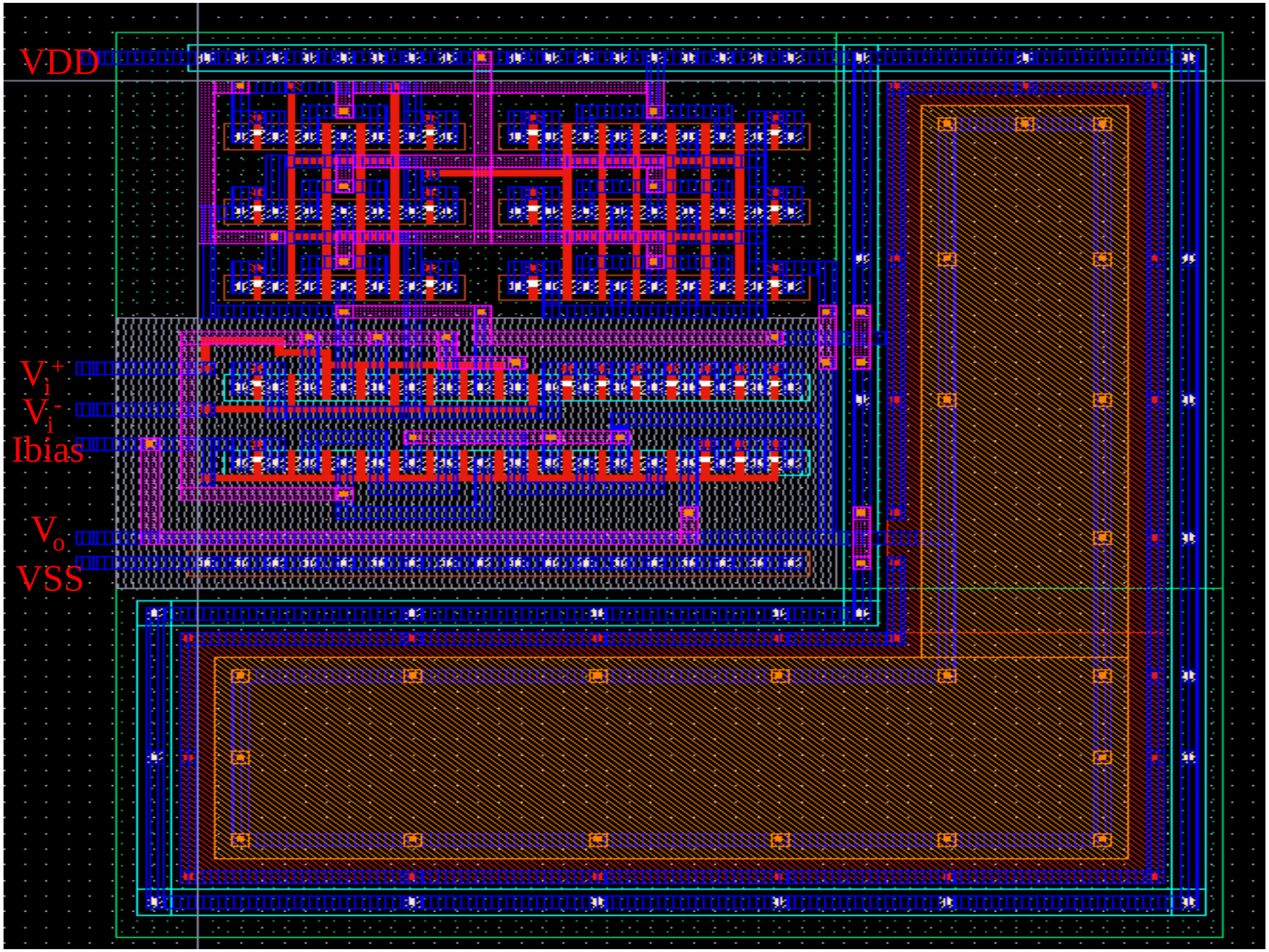


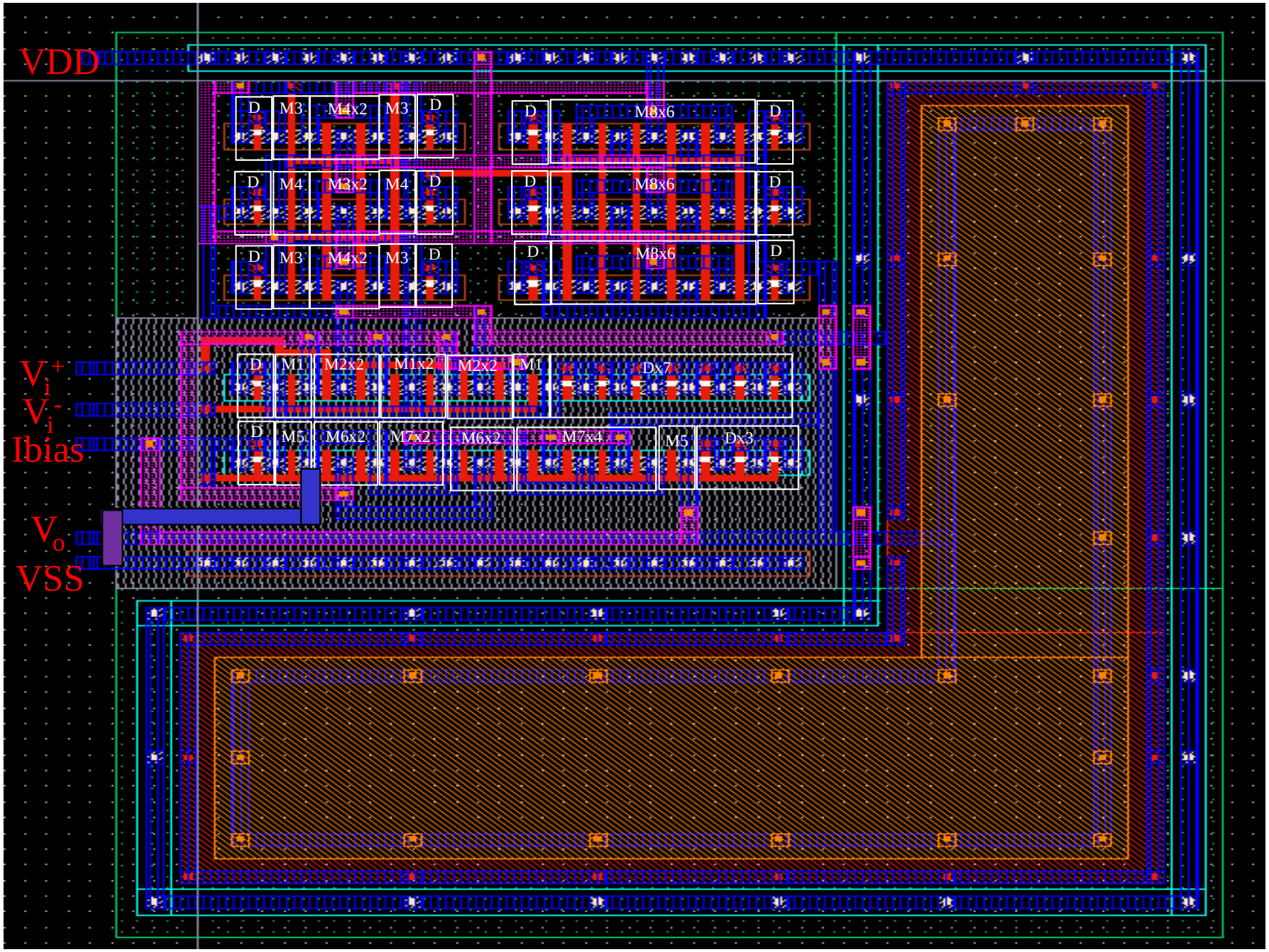
Not the best floorplan, but OK



Pay attention to your floor plan! It is critical for minimizing iterations: Identify the critical elements


vdd
w = 24u
l = 2
M3
w = 24u
l = 2
M4
w = 72u
l = 2u
M8
l = 2u
w = 16u
M1
l = 2u
w = 16u
M2
Ibias
Vi-
Vi+
Cc
c=10p
18p
Vo
l = 2u
w = 8u
M5
l = 2u
w = 16u
M6
net18
w = 24u
M7
vss


VDD
V_i^+
V_i^-
Ibias
V_o
VSS


VDD
V_i^+
V_i^-
Ibias
V_o
VSS
D M3 M4x2 M3 D
D M8x6 D
D M4 M3x2 M4 D
D M8x6 D
D M3 M4x2 M3 D
D M8x6 D
D M1 M2x2 M1x2 M2x2 M1 Dx7
D M5 M6x2 M7x2 M6x2 M7x4 M5 Dx3

Following slides were provided by some of Dr. Silva's graduate students.

Special thanks to Fabian Silva-Rivas, Venkata Gadde, Marvin Onabajo, Cho-Ying Lu, Raghavendra Kulkarni and Jusung Kim

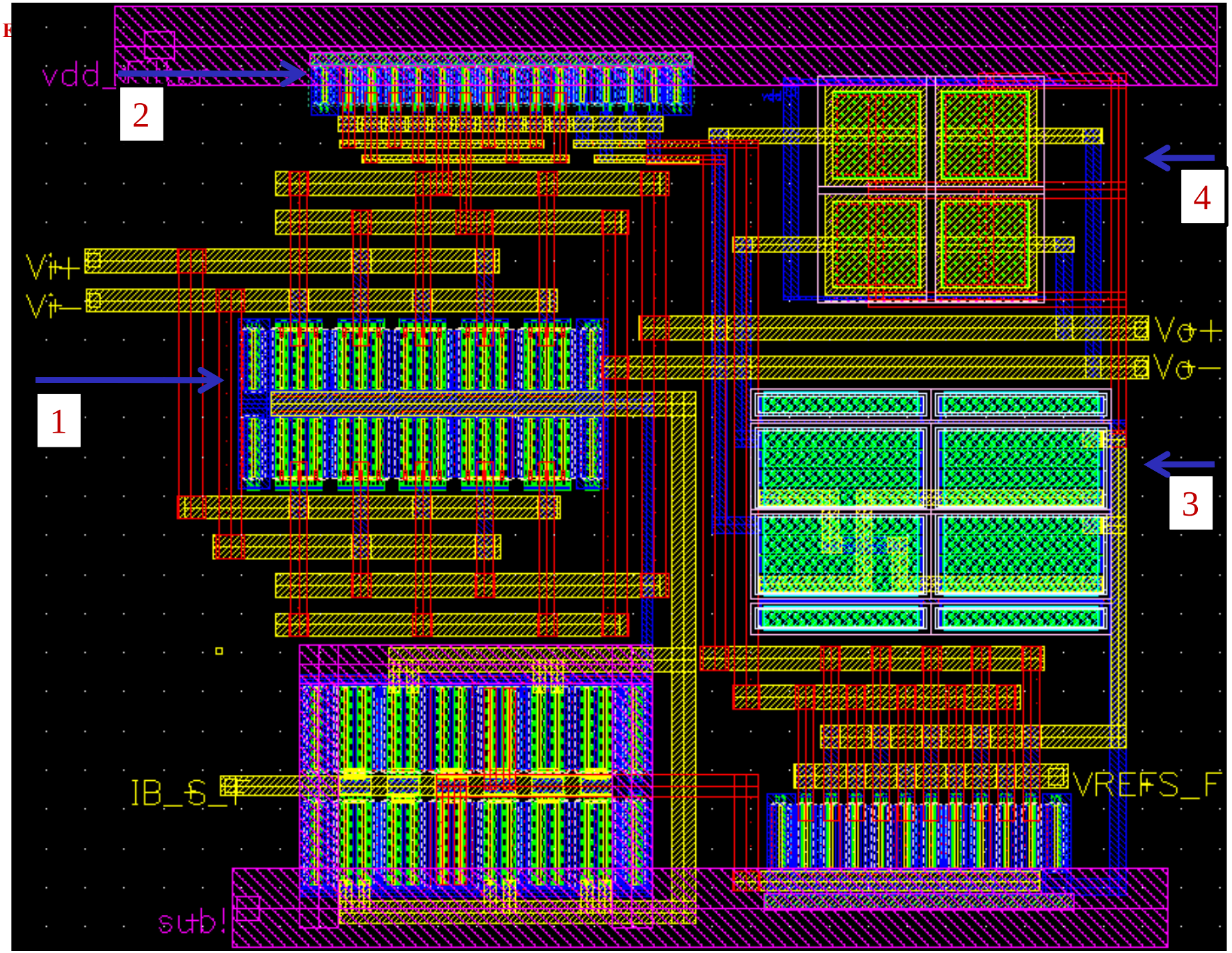


Figure: Layout of a single stage fully differential amplifier and its CMFB circuit.

1. I/p NMOS diff pair 2. PMOS (Interdigitated) 3. Resistors for V_{CM} 4.Capacitors (Common centroid)

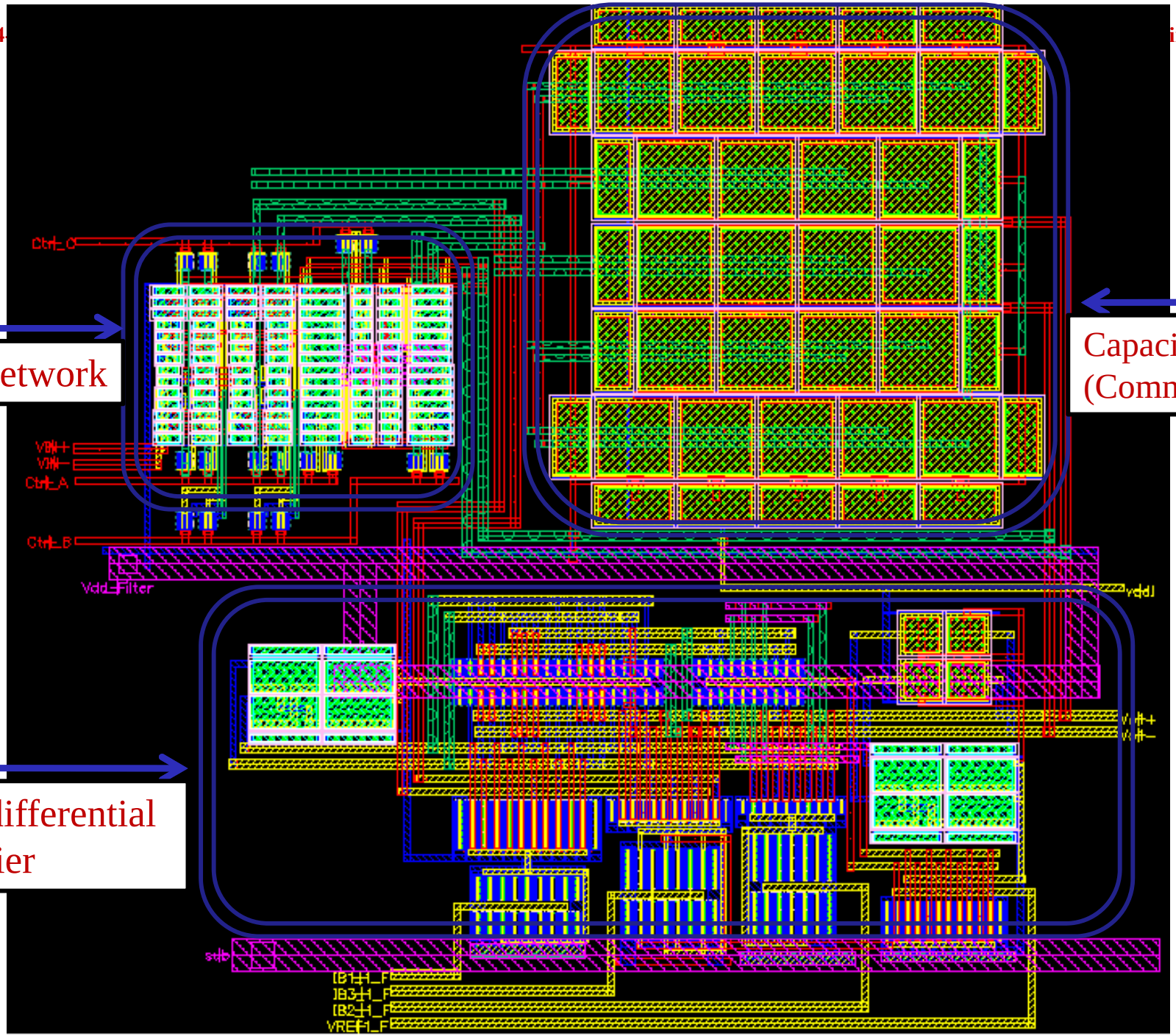
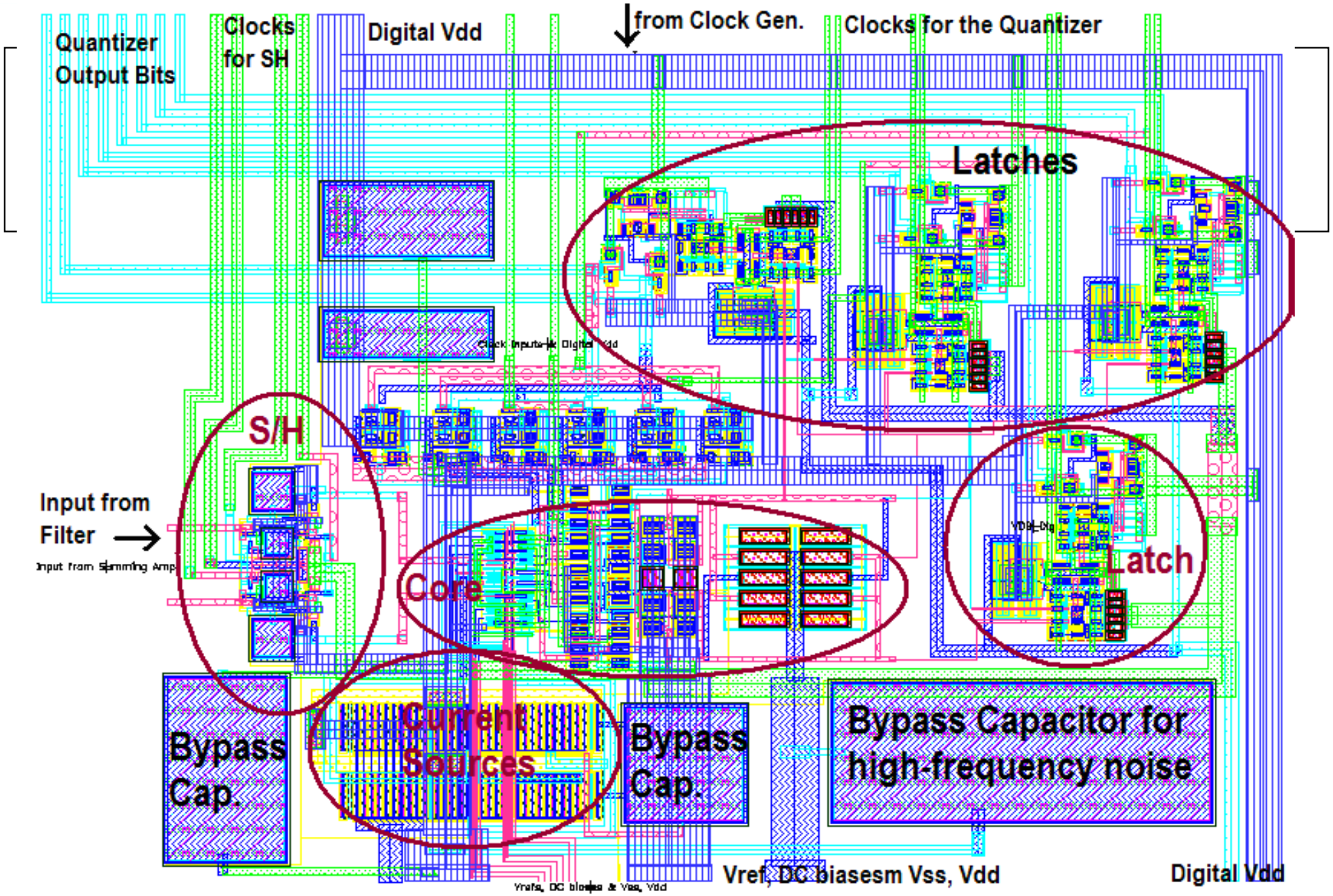
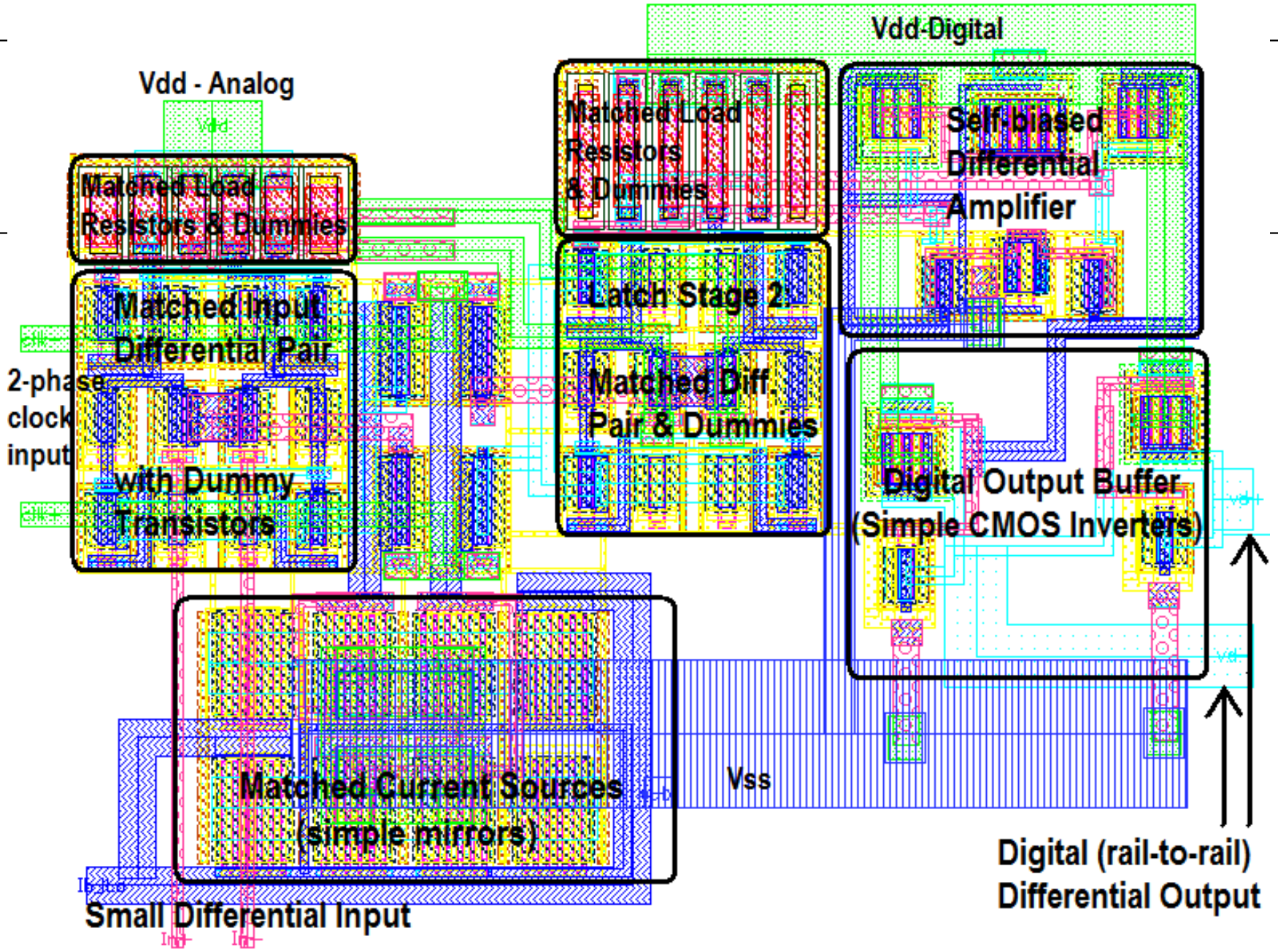


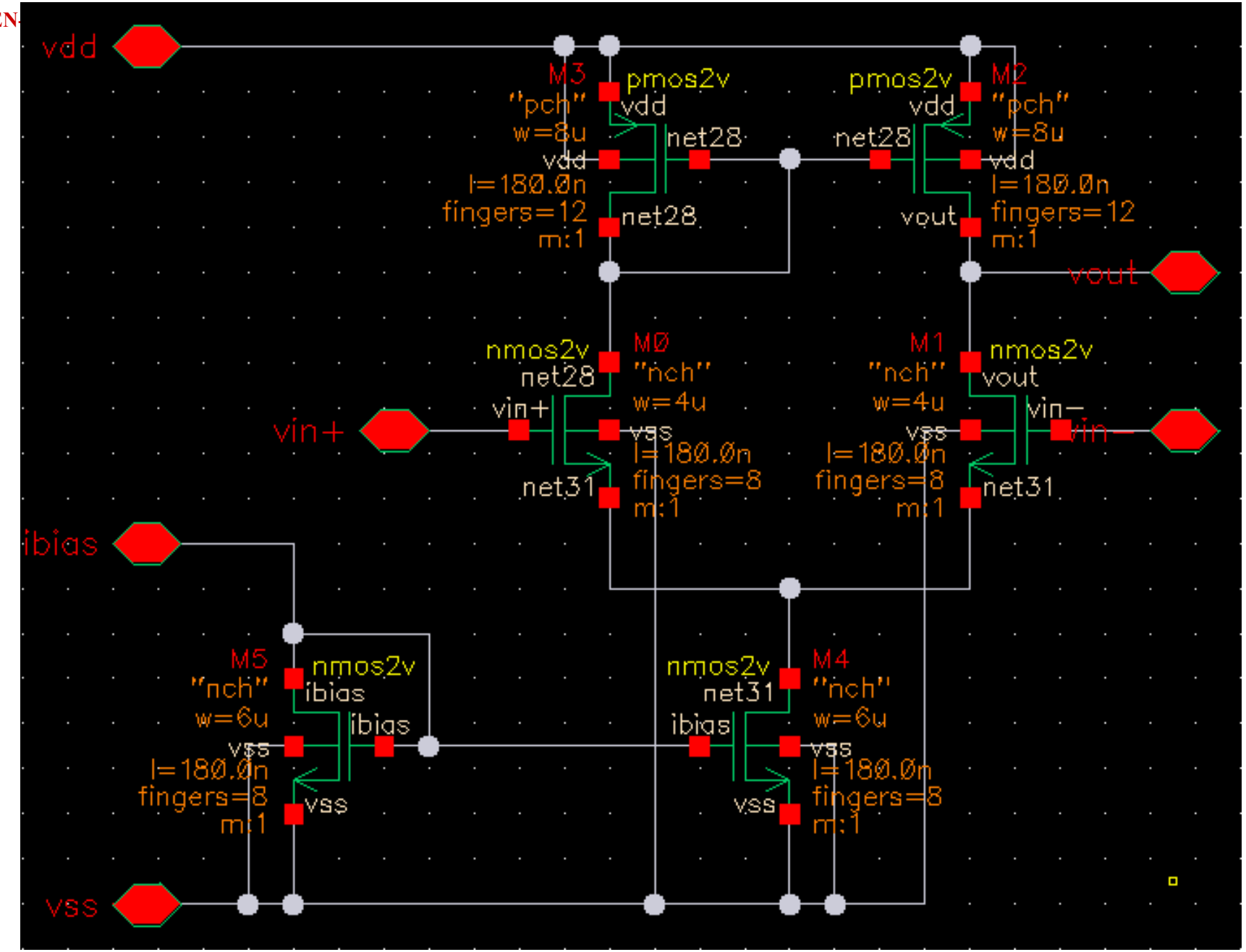
Figure: Layout of a second order Active RC low-pass Filter (Bi-quad)



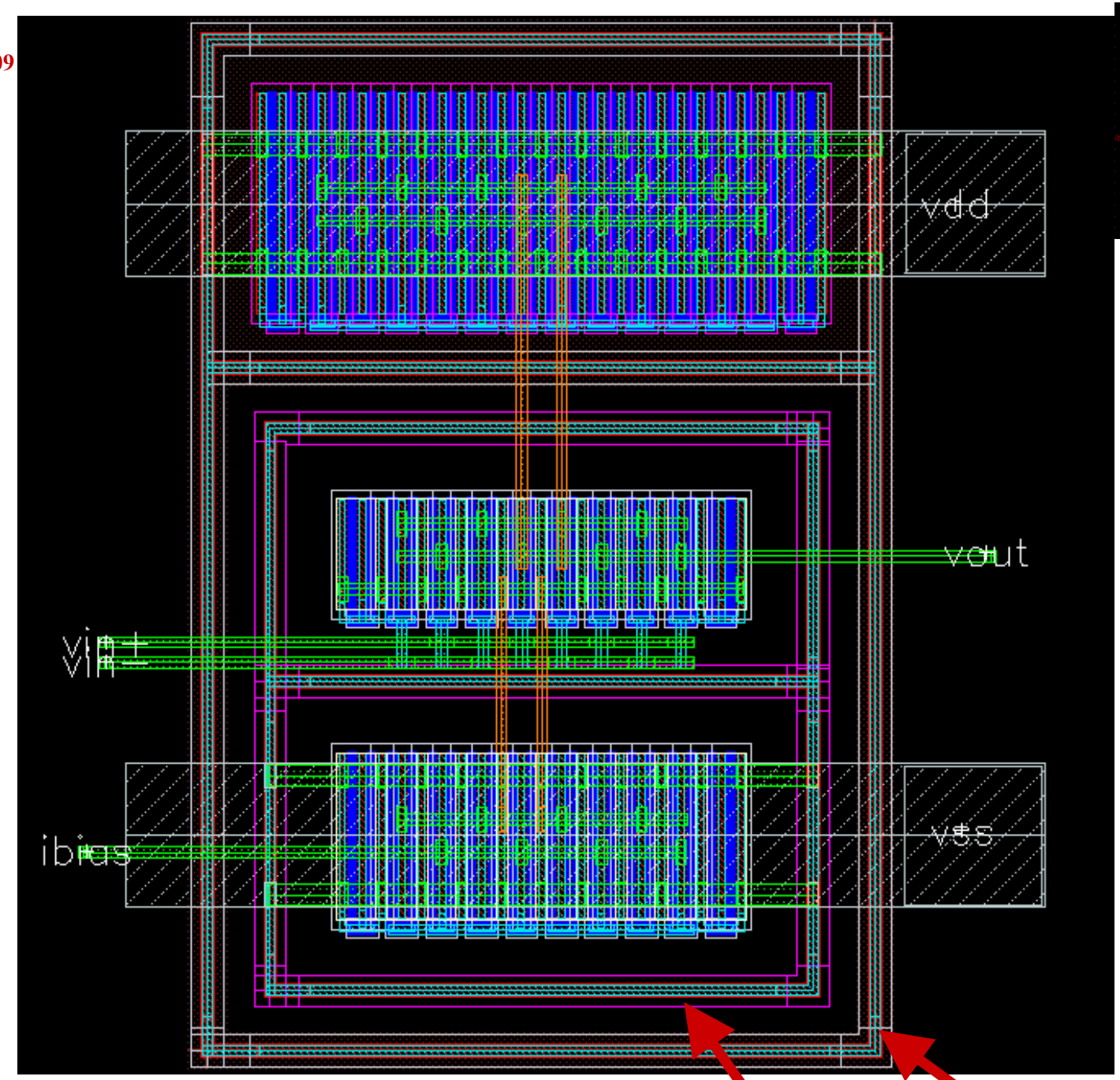
- **3-bit quantizer in Jazz 0.18µm CMOS technology**
- S/H: sample-and-hold circuit that is used to sample the continuous-input signal
- Core: contains matched differential pairs and resistors to create accurate reference levels for the analog-to-digital conversion
- Latches: store the output bits; provide interface to digital circuitry with rail-to-rail voltage levels

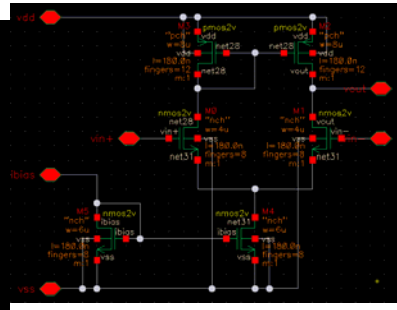


- **High-speed D-Flip-Flop in Jazz 0.18µm CMOS technology**
- Resolves a small differential input with $10mV < V_{p-p} < 150mV$ in less than 360ps
- Provides digital output (differential, rail-to-rail) clocked at 400MHz
- The sensitive input stage (1st differential pair) has a separate “analog” supply line to isolate it from the noise on the supply line caused by switching of digital circuitry

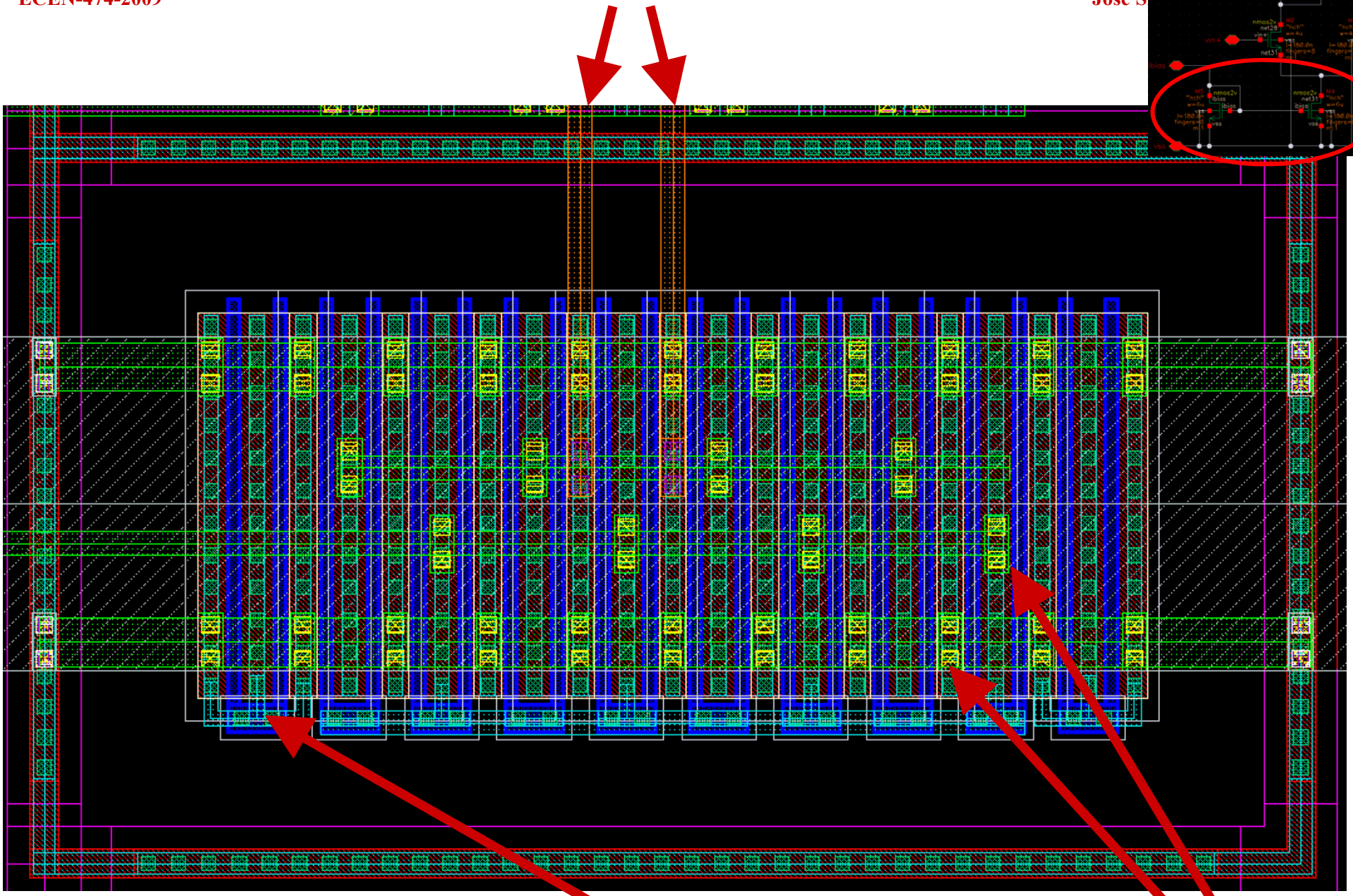


Design example (industrial quality): Simplest OTA

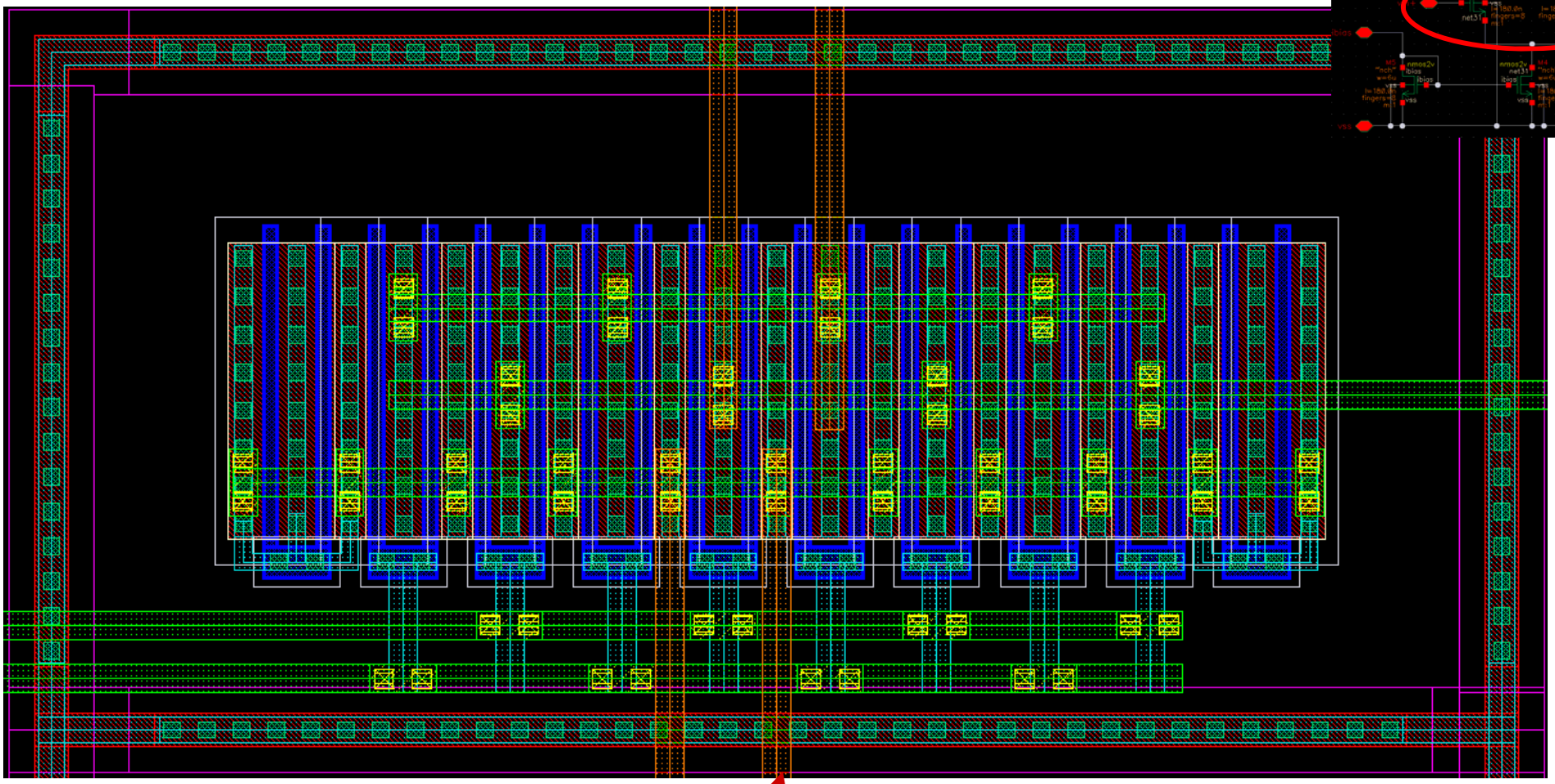




Overall amplifier: Have a look on the guard rings and additional well!

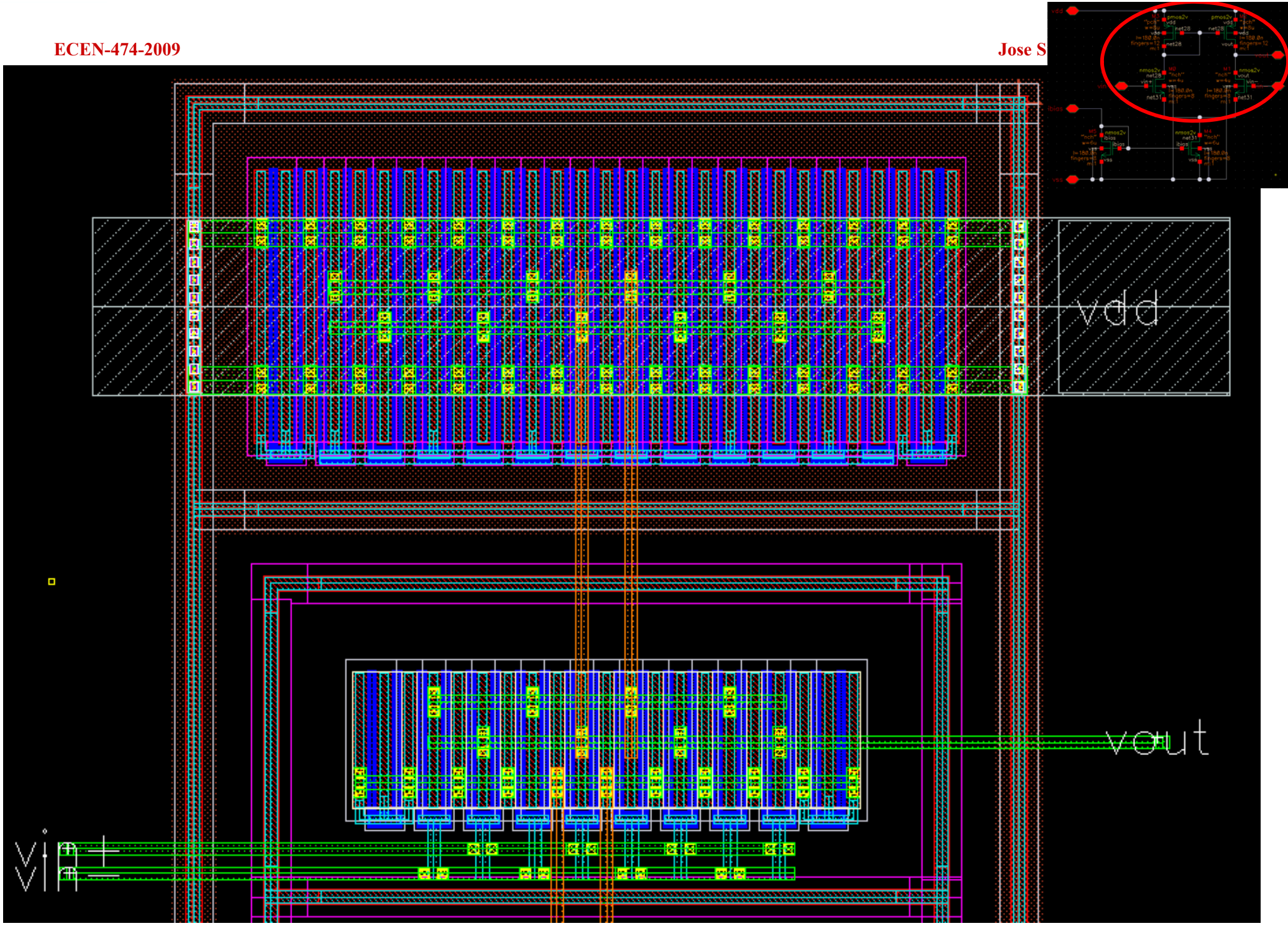


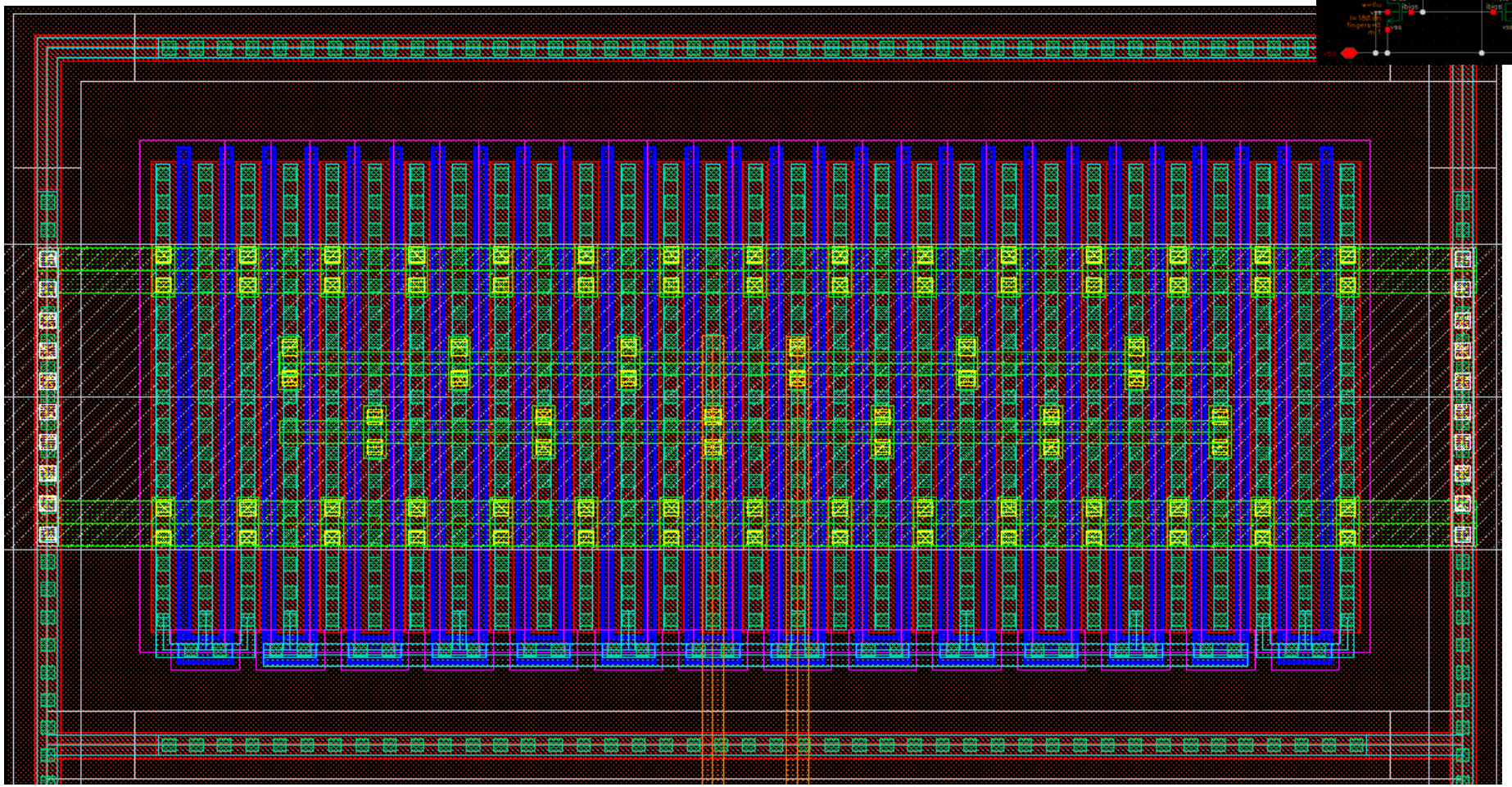
BIAS: you may be able to see the dummies, symmetry and S/D connections



From downstairs

Differential pair


vdd
vout
vin+
vin-



Details on the P-type current mirrors

Q-value of Spiral Inductors in CMOS Process

Most of the following slides were taken from

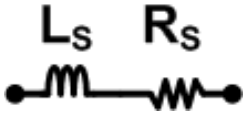
Seminar by: Park, Sang Wook

TAMU, 2003

What is Q?

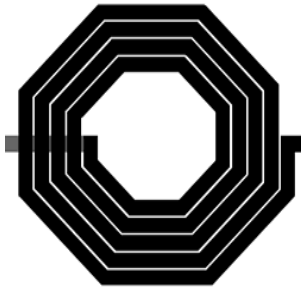
$$Q \equiv \omega \frac{\text{energy stored}}{\text{average power dissipated}}$$

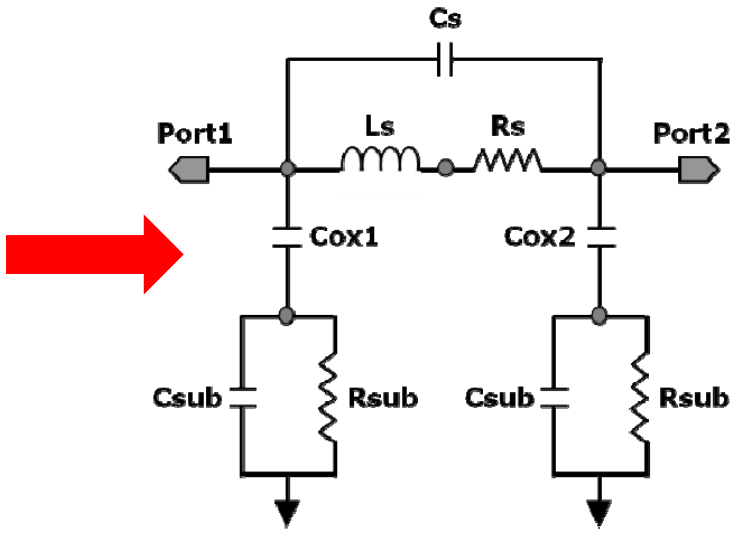
Simple Inductor Model:

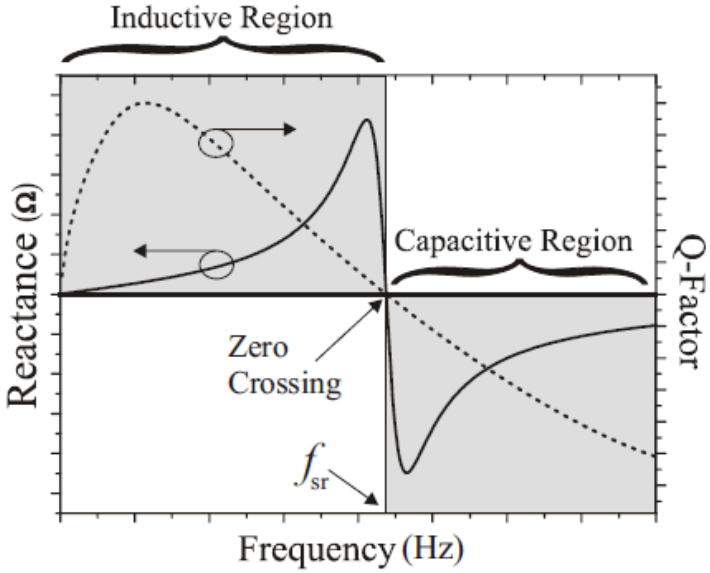


$$Q = \frac{\omega L_s}{R_s}$$

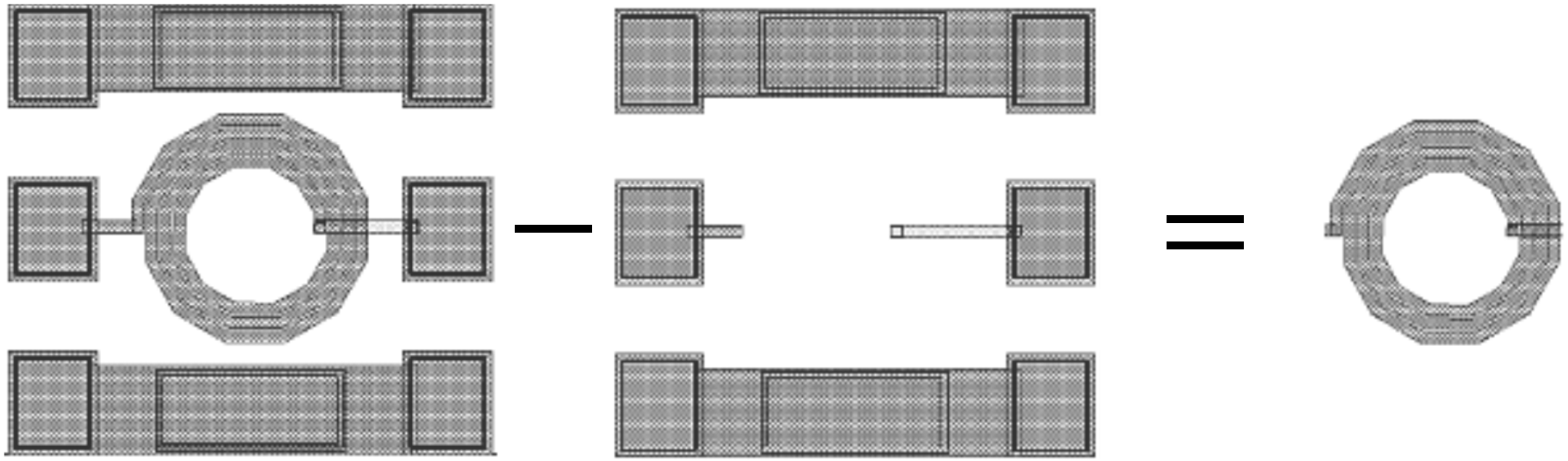
Integrated Spiral Inductor “Pi” Model

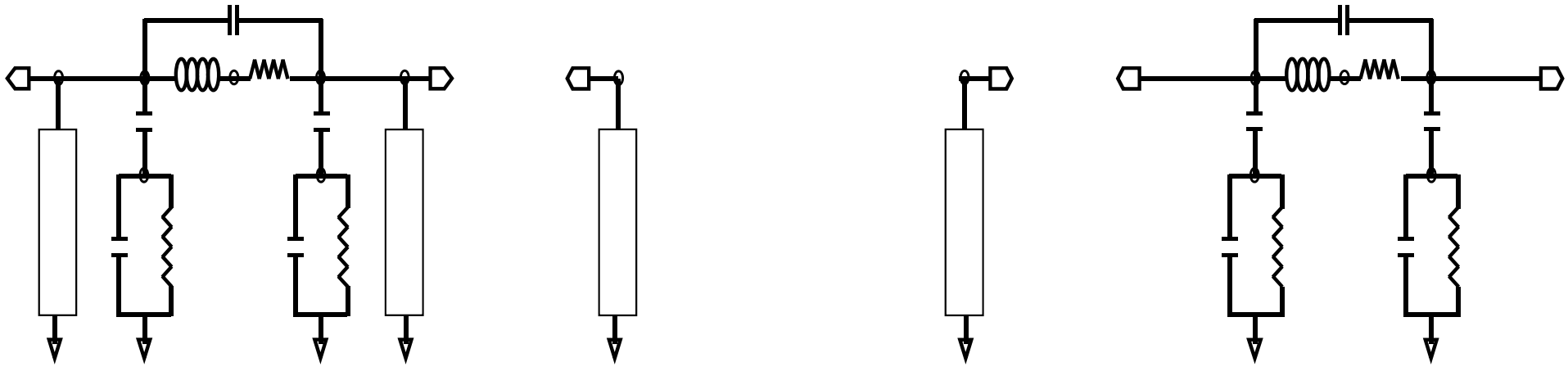




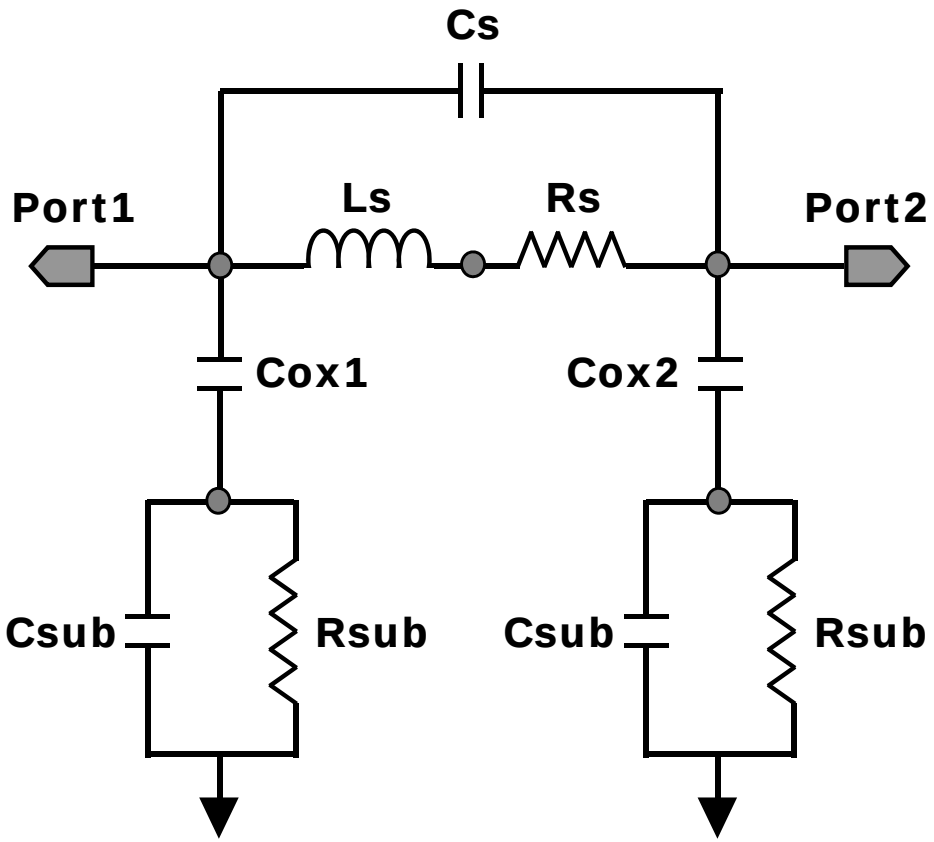


De-Embedding

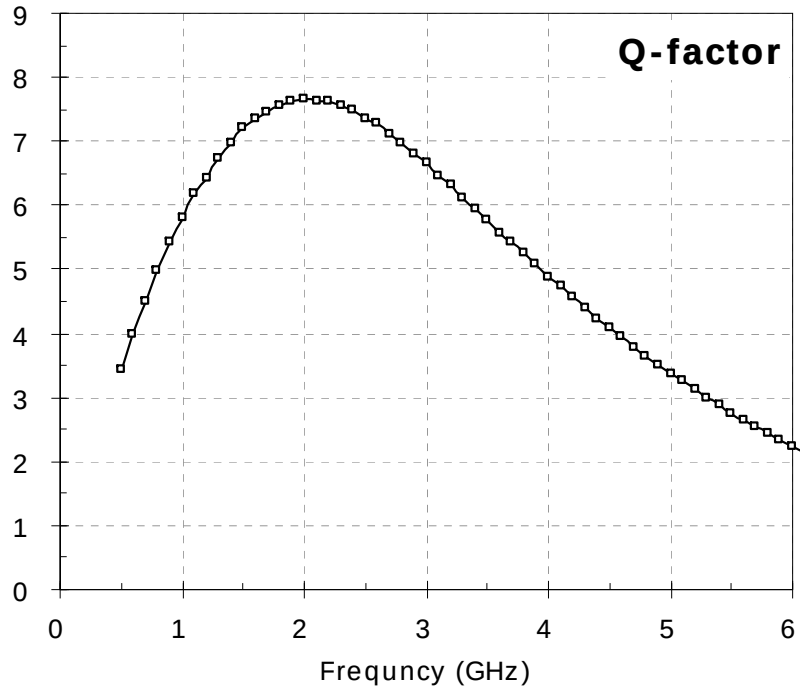




Equivalent Circuit & Calculation

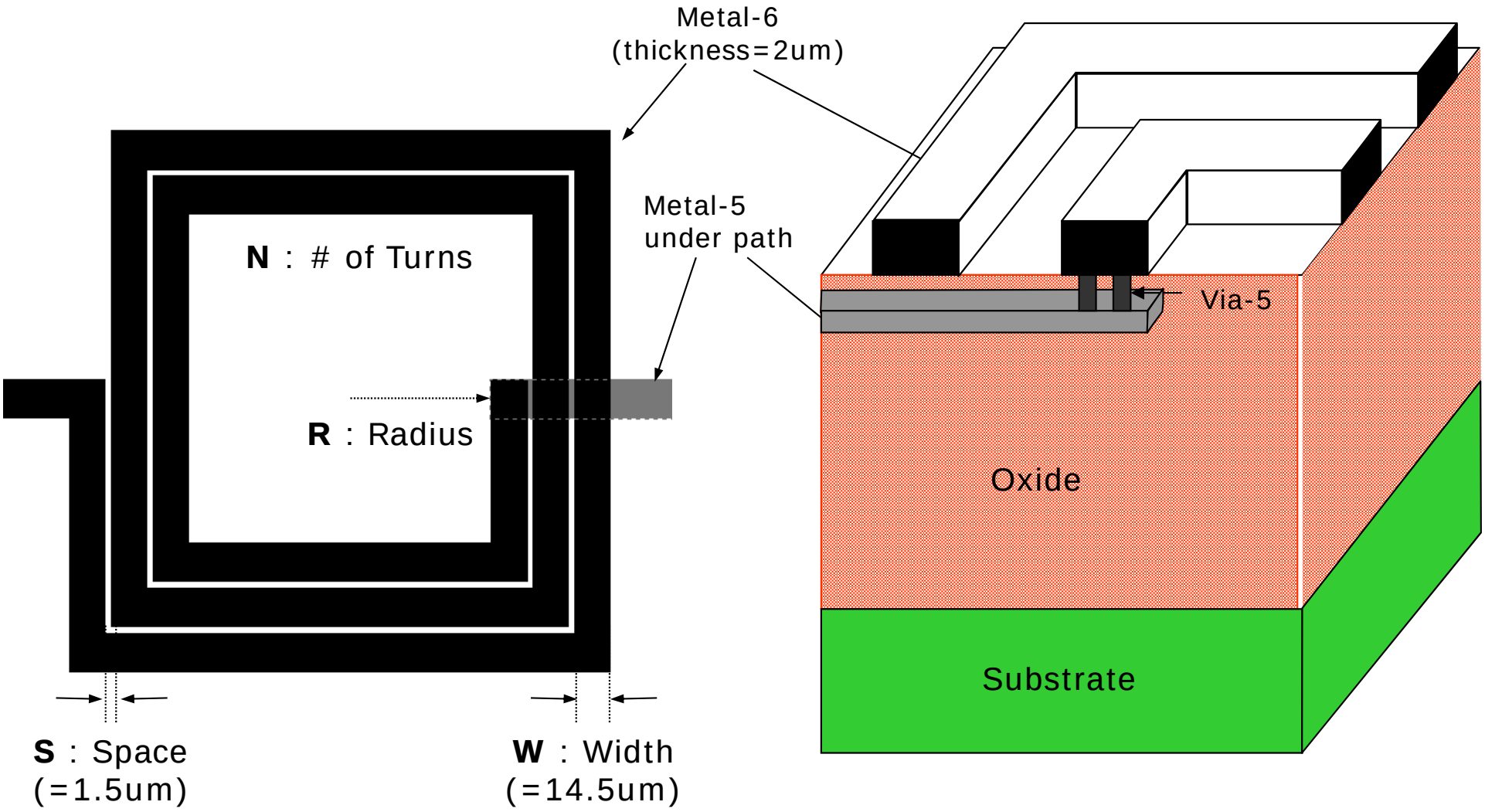


Equivalent Circuit



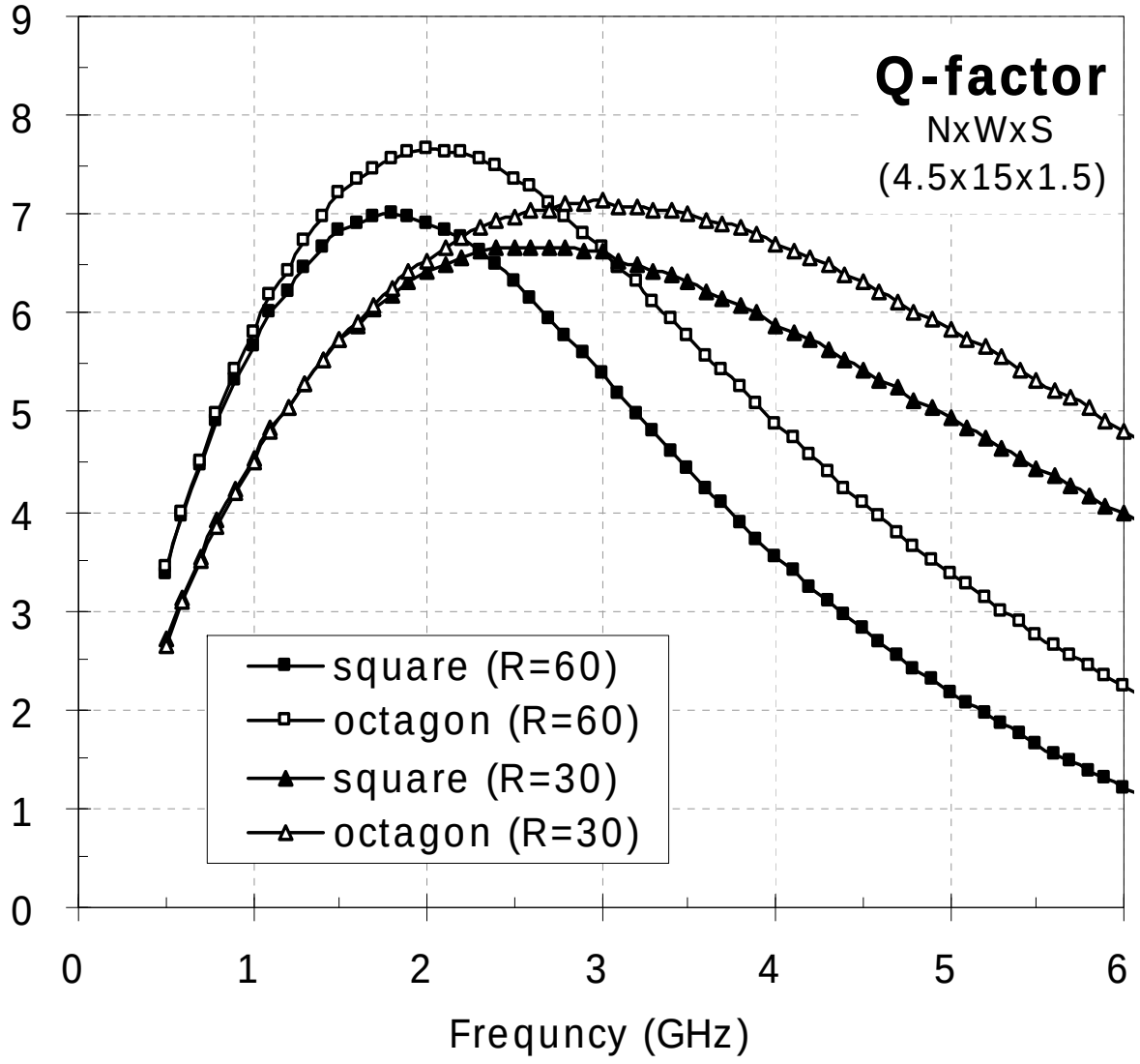
Parameter Calculation

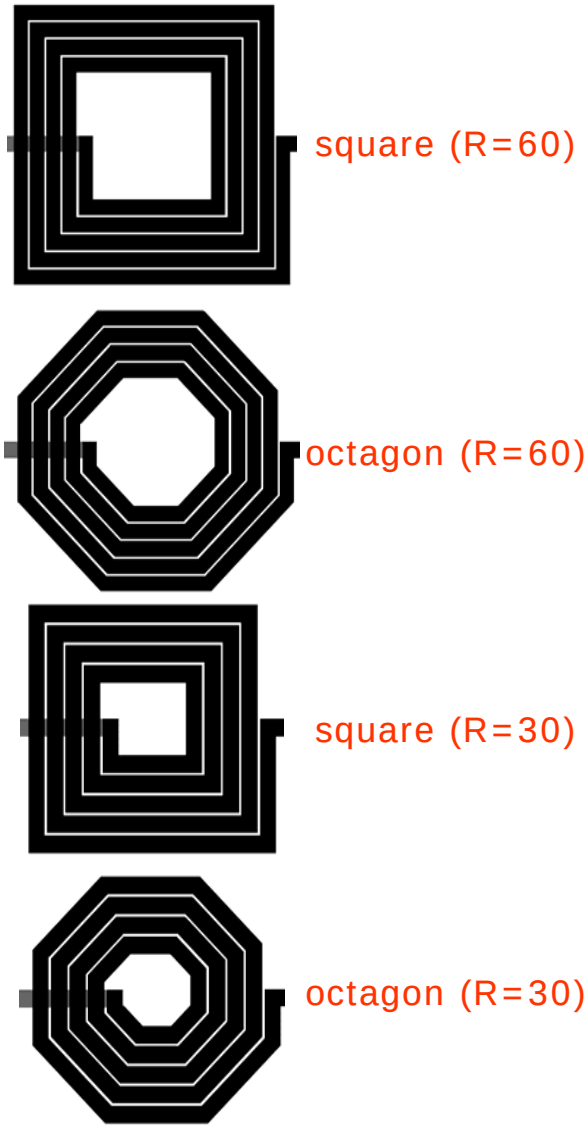
Layout & Structure



Layout Split 1

Shape & Radius

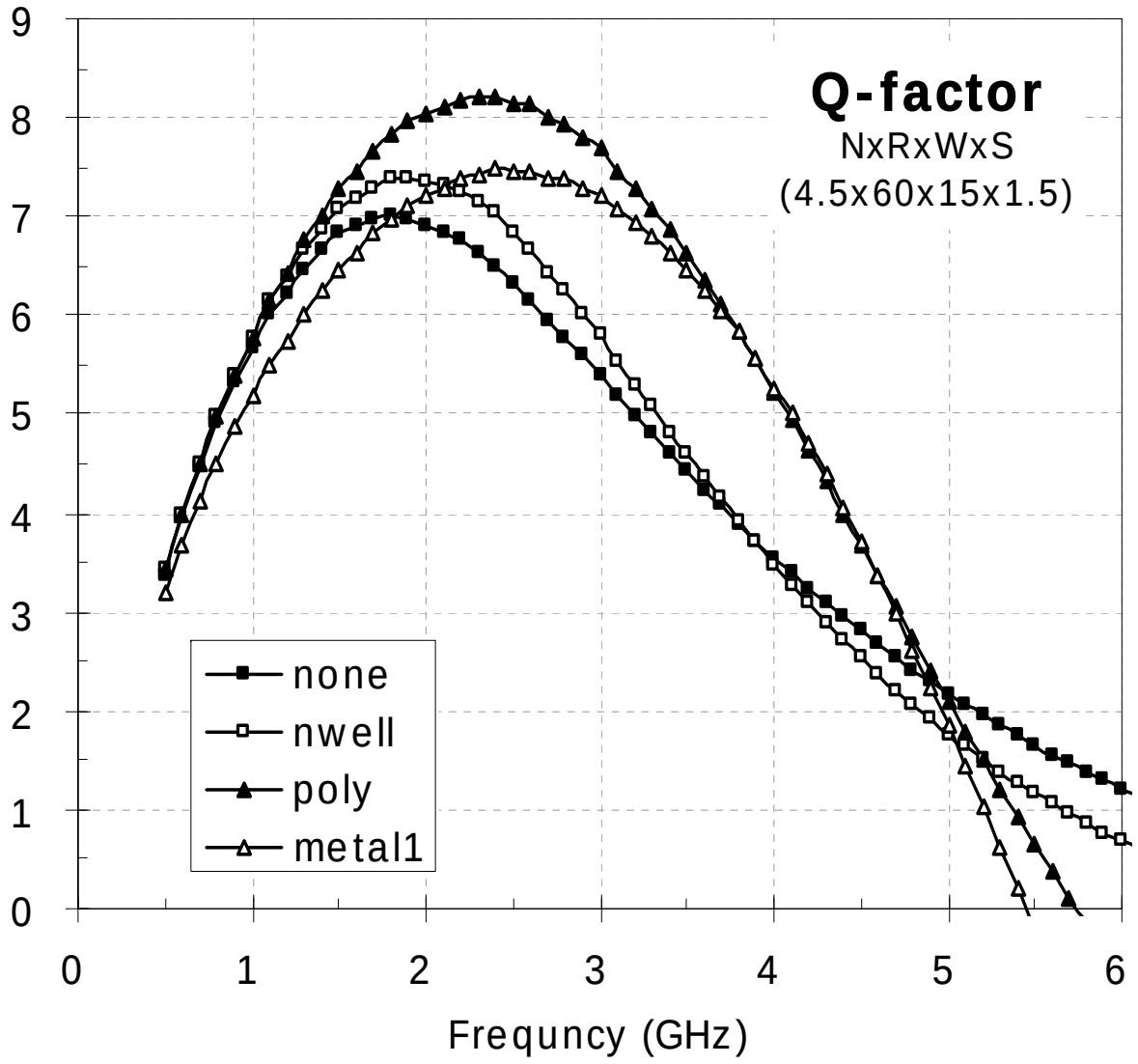


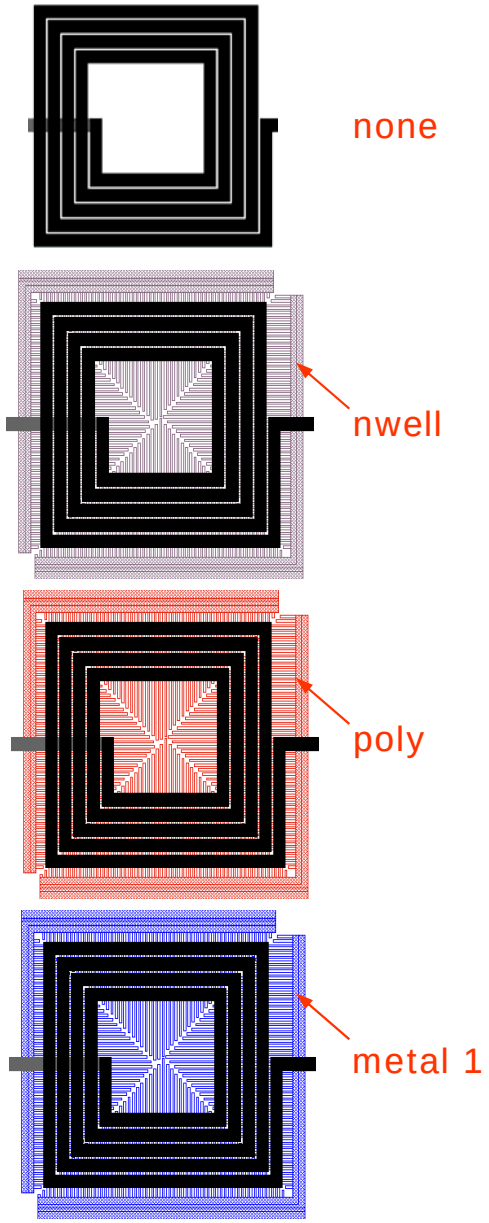


- **Shape : Octagon > Square**
- **Radius : 60 > 30**

Layout Split 2

PGS (Patterned Ground Shield) material

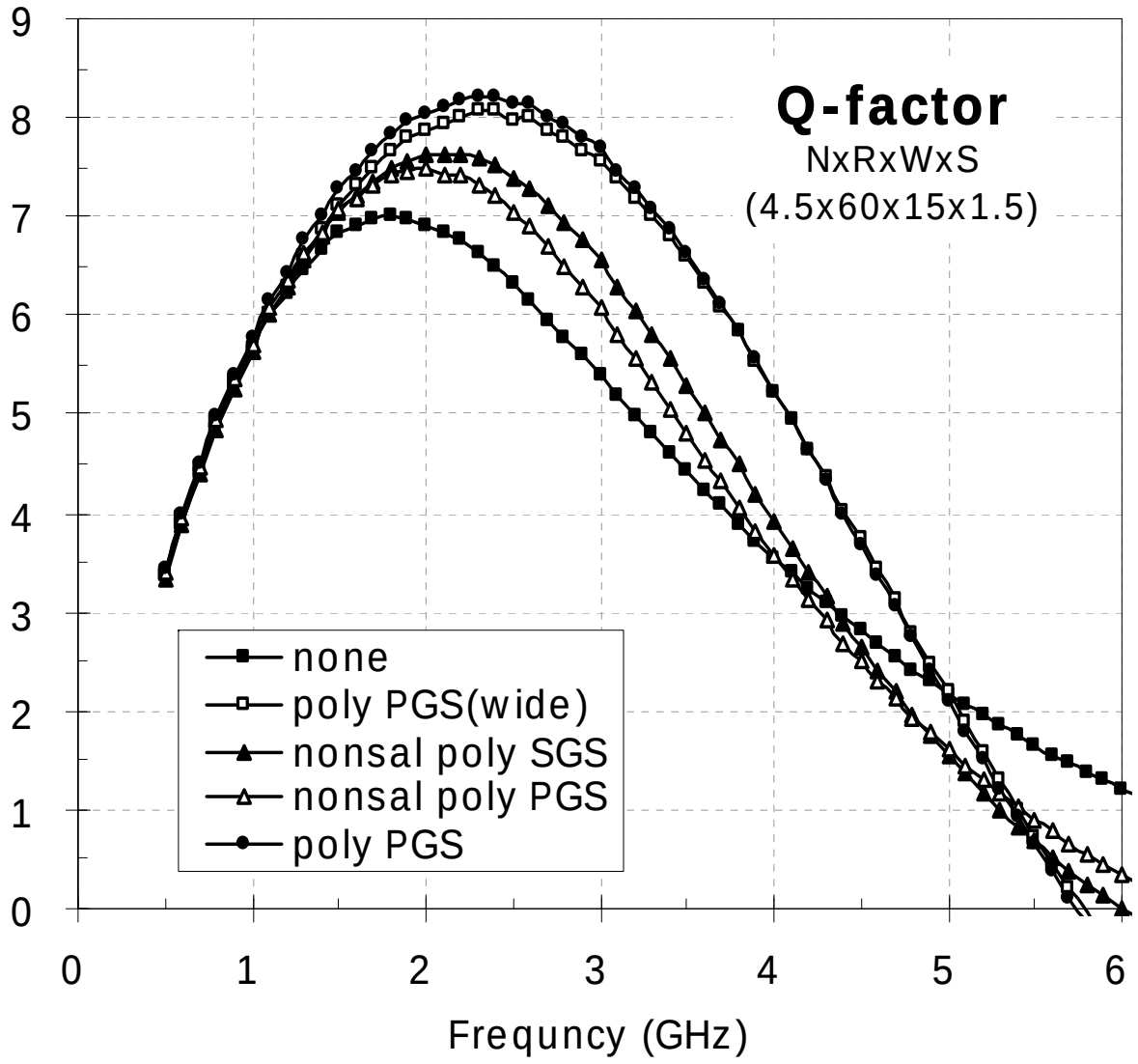


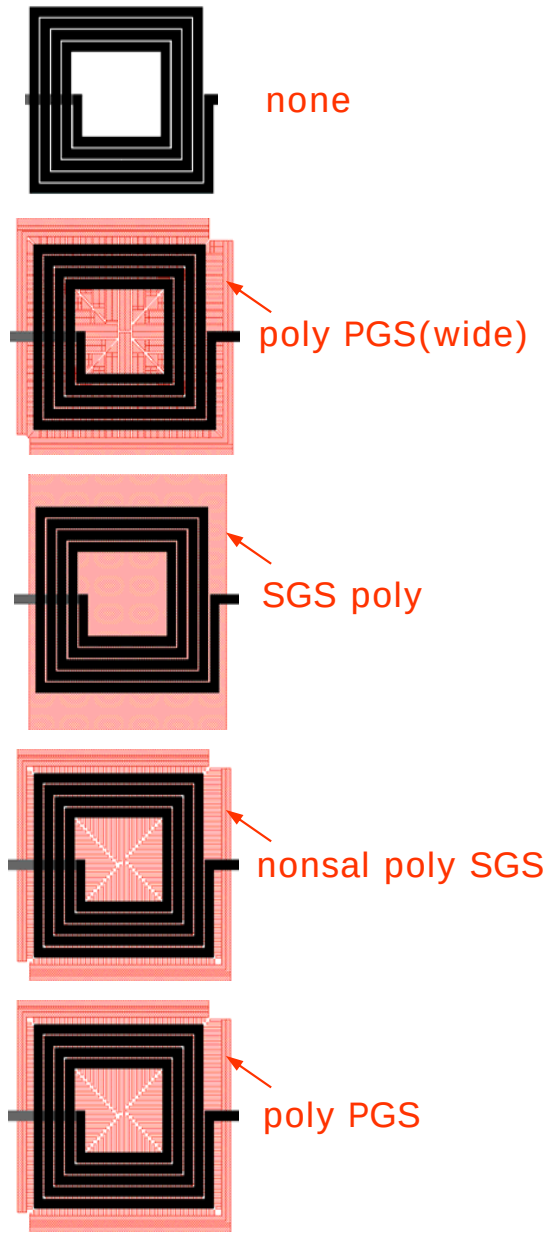


PGS : Poly > Nwell > none > Metal1

Layout Split 3

GS (Ground Shield) type





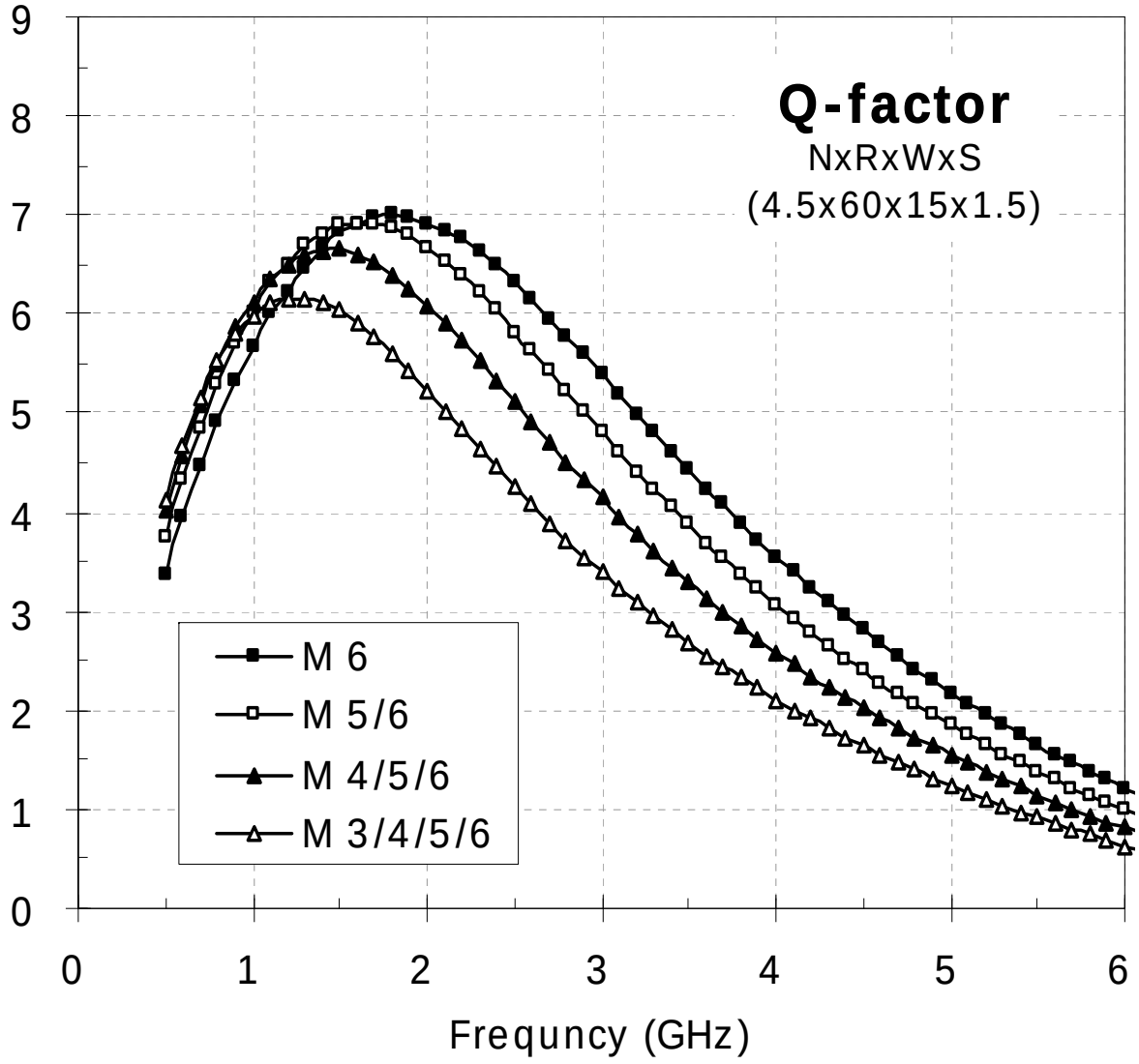
- **GS : Poly PGS > Poly(nonsal) SGS > Poly(nonsal) PGS > none**

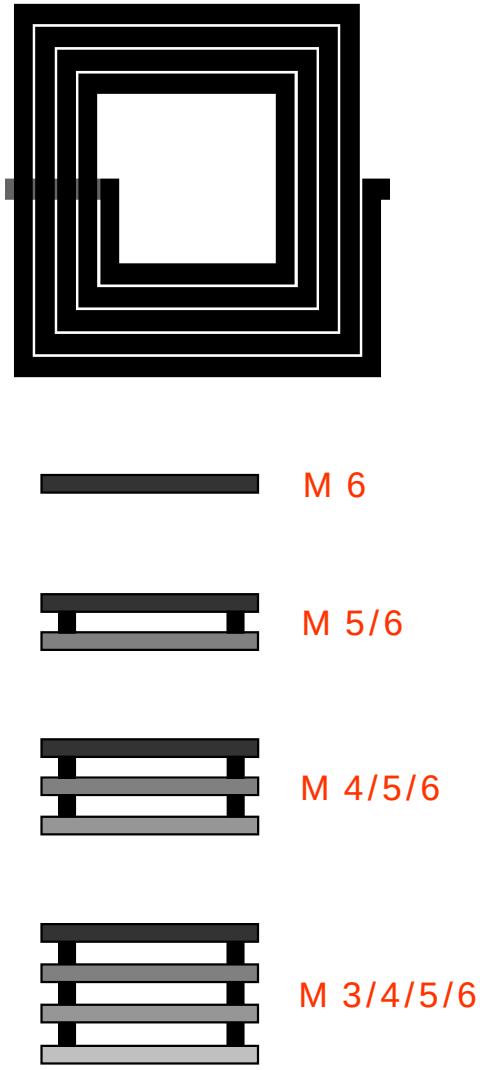
PGS = patterned ground shield

SGS = solid ground shield

Layout Split 4

Metal Stack

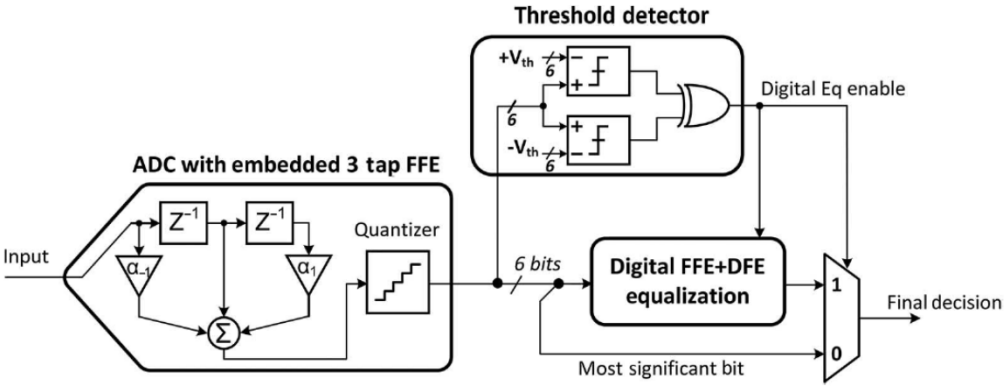


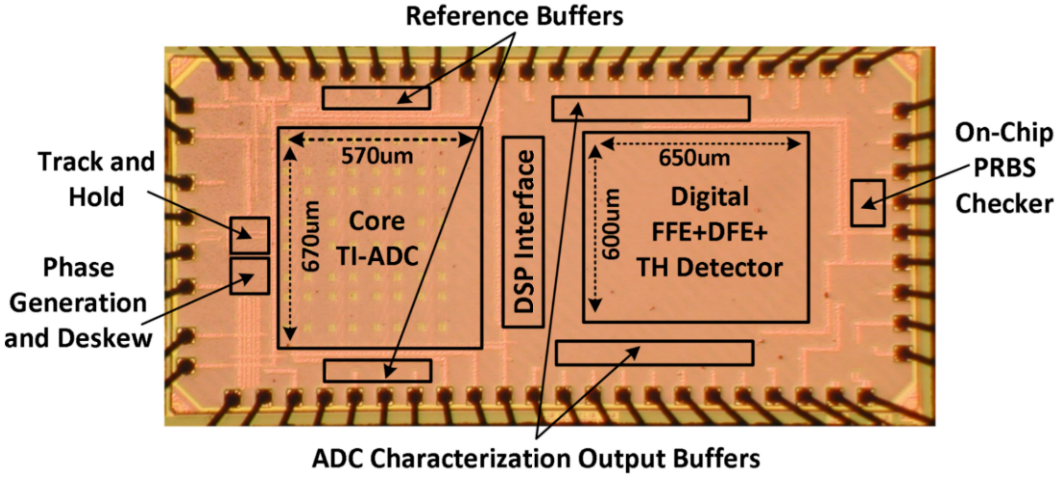


- **Stack : M6 > M5/6 > M4/5/6 > M3/4/5/6**

TAMU Mixed-Signal Research Chip

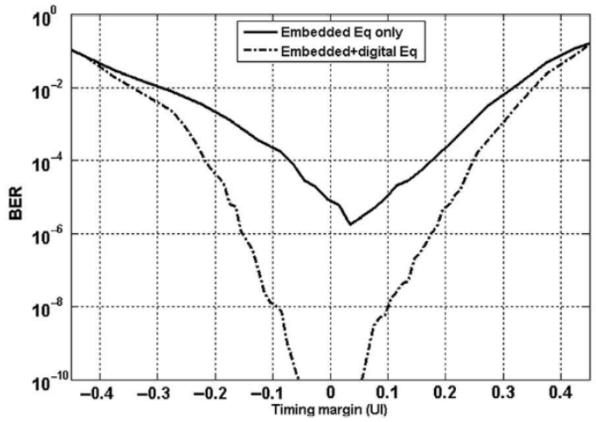
- A 10 Gb/s Hybrid ADC-Based Receiver w/ Embedded Analog and Per-Symbol Dynamically Enabled Digital Equalization





- 10GS/s asynchronous SAR ADC with embedded 3-tap FFE
- Digital equalizer with 4-tap FFE and 3-tap DFE
- Fabricated in GP 65nm CMOS

BER w/ 36.4dB Loss Channel



A. Shafik et al, "A 10Gb/s Hybrid ADC-Based Receiver with Embedded 3-Tap Analog FFE and Dynamically-Enabled Digital Equalization in 65nm CMOS," ISSCC 2015.

A. Shafik et al, "A 10 Gb/s Hybrid ADC-Based Receiver With Embedded Analog and Per-Symbol Dynamically Enabled Digital Equalization," JSSC 2016.

Next Time

- Current Mirrors