ECEN474/704: (Analog) VLSI Circuit Design
Spring 2018

Lecture 1: Introduction

Sam Palermo

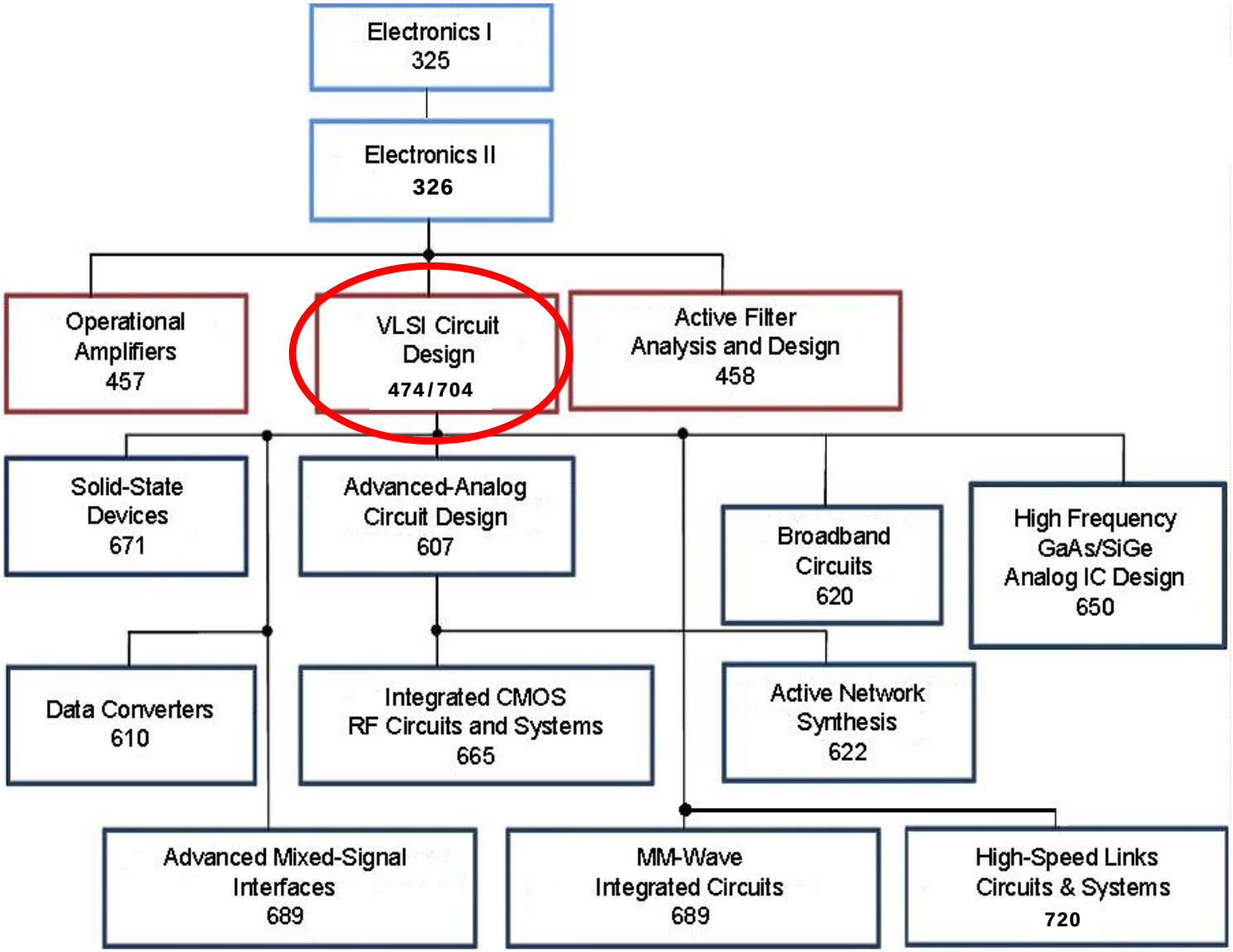
Analog & Mixed-Signal Center

Texas A&M University

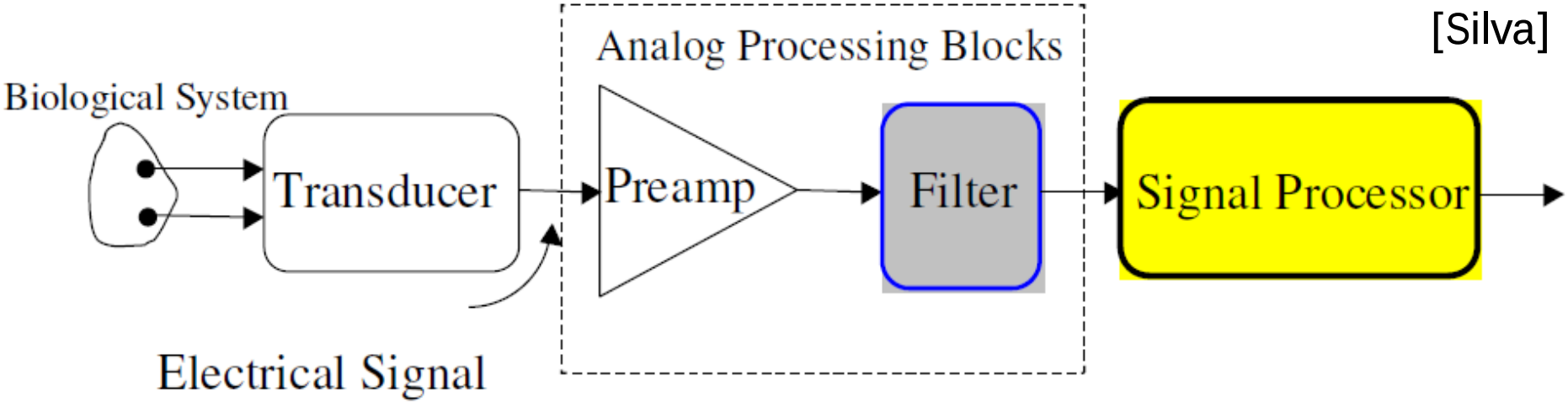
Announcements

- Turn in your 0.18um NDA form by Tuesday Jan 23
- No Lab this week
  - Lab 1 starts Jan 31
- Lab requires a Linux account
  - Go to CVLB 324 to see if you can login
  - Same Login ID and Password as the HOWDY portal
  - Contact Omar Valenzuela (o4valenzuela@tamu.edu) in WEB 076 if any issues
- Current Reading
  - Razavi Chapters 2 & 17

Analog Circuit Sequence



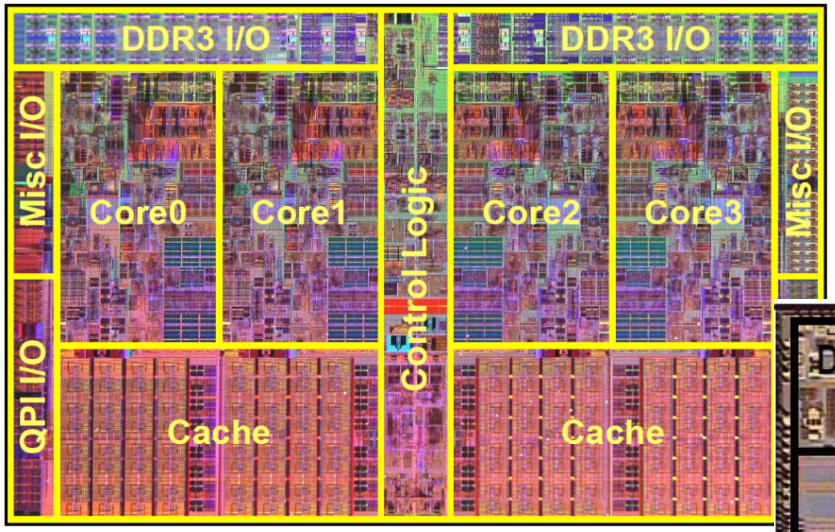
Why is Analog Important?



- Naturally occurring signals are analog
- Analog circuits are required to amplify and condition the signal for further processing
- Performance of analog circuits often determine whether the chip works or not
- Examples
  - Sensors and actuators (imagers, MEMS)
  - RF transceivers
  - Microprocessor circuits (PLL, high-speed I/O, thermal sensor)

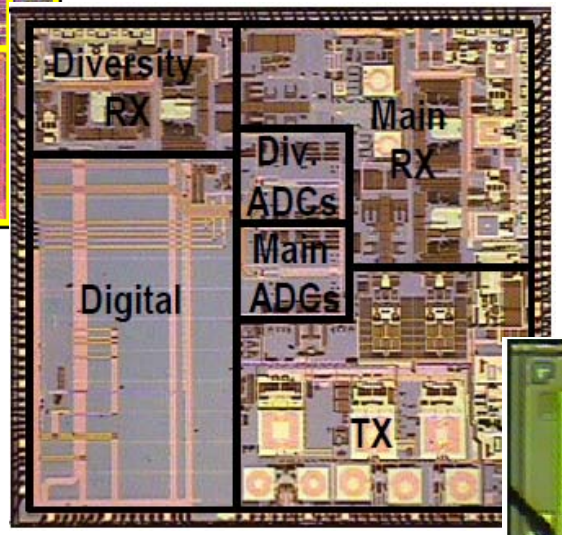
Integrated Circuits

[Bohr ISSCC 2009]



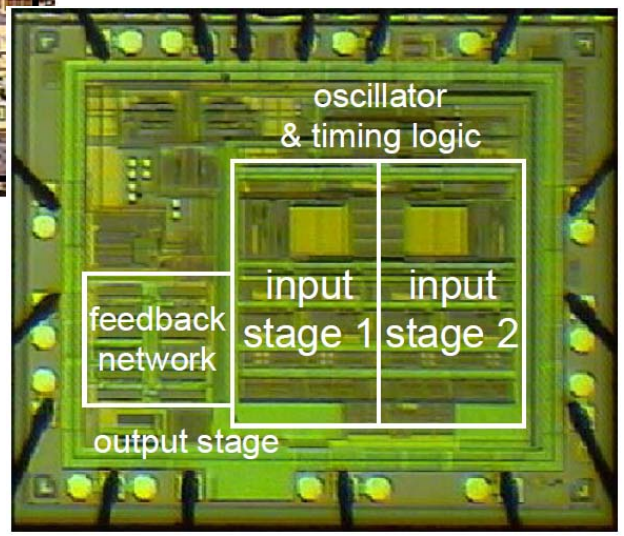
- 4-core Microprocessor (45nm CMOS)
  - Mostly Digital
  - Noteable analog blocks
    - PLL, I/O circuits, thermal sensor

[Sowlati ISSCC 2009]



- Cellular Transceiver (0.13μm CMOS)
  - Considerable analog & digital

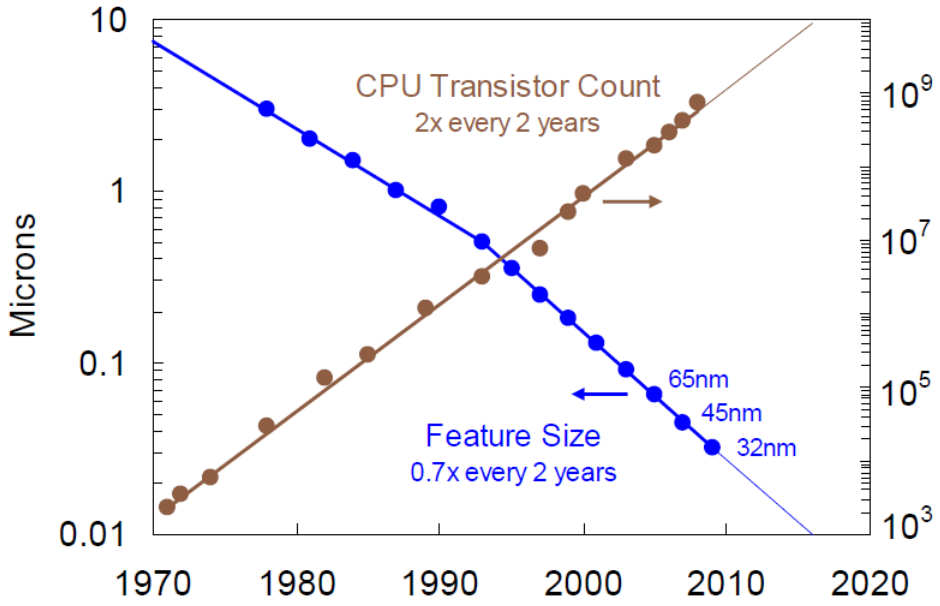
[Pertijs ISSCC 2009]

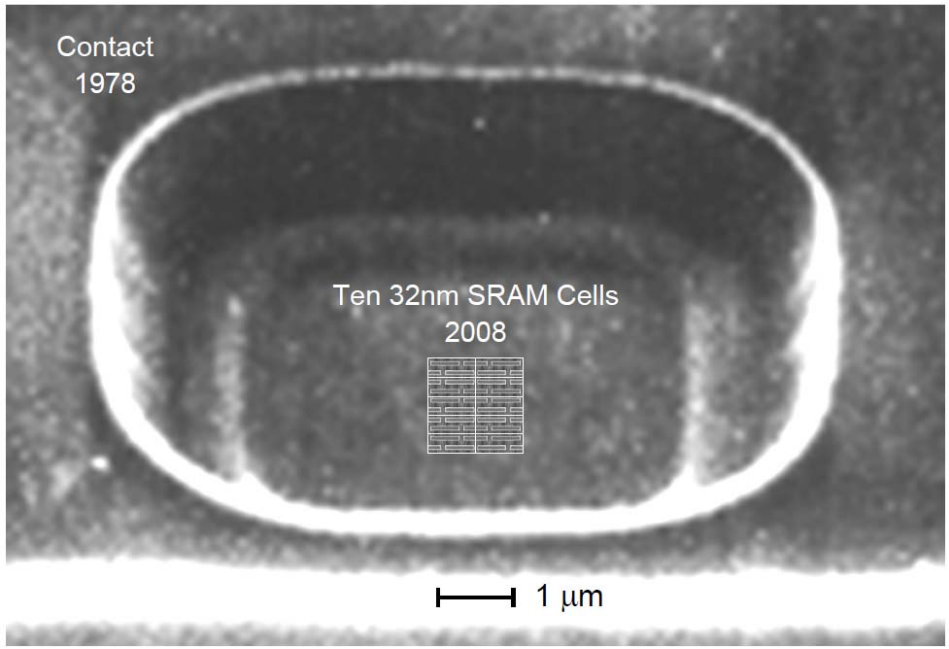


- Instrumentation Amplifier (0.5μm CMOS)
  - Mostly Analog
  - Some Digital Control Logic

The Power of CMOS Scaling

[Bohr ISSCC 2009]





- Scaling transistor dimensions allows for improved performance, reduced power, and reduced cost/transistor
- Assuming you can afford to build the fab
  - 32nm CMOS fab ~3-4 BILLION dollars

Course Topics

- CMOS technology
  - Active and passive devices
  - Layout techniques
- MOS circuit building blocks
  - Single-stage amplifiers, current mirrors, differential pairs
- Amplifiers and advanced circuit techiques

Course Goals

- Learn analog CMOS design approaches
  - Specification $\Rightarrow$ Circuit Topology $\Rightarrow$ Circuit Simulation $\Rightarrow$ Layout $\Rightarrow$ Fabrication
- Understand CMOS technology from a design perspective
  - Device modeling and layout techniques
- Use circuit building blocks to construct moderately complex analog circuits
  - Multi-stage amplifiers, filters, simple data converters, ...

Administrative

- Instructor:
  - Sam Palermo
  - 315E WERC Bldg., 845-4114, spalermo@tamu.edu
  - Office hours: T 2:30pm-4:00pm, W 8:30AM-10:00AM
    - Distance learning office hours will be held via Zoom (similar to WebEx) at the same time. Email me if you want to meet and I will set up the session.
- Lectures: TR 11:00am-12:25pm, WEB 049
  - Distance learning lecture recordings will be posted online on same day at ~4PM
- Class web page
  - http://www.ece.tamu.edu/~spalermo/ecen474.html
  - We will also use eCampus, but the above will be the main site

Class Material

- Textbook: *Design of Analog CMOS Integrated Circuits*, B. Razavi, McGraw-Hill, 2nd Edition, 2017.
- References
  - *Analog Integrated Circuit Design*, T. Chan Carusone, D. Johns and K. Martin, John Wiley & Sons, 2nd Edition, 2011.
  - *Analysis and Design of Analog Integrated Circuits*, P. Gray, P. Hurst, S. Lewis, and R. Meyer, John Wiley and Sons, 5th Edition, 2009.
  - *Microelectronic Circuits*, A. Sedra and K. Smith, Oxford University Press, 7th Edition, 2014.
  - Technical Papers
- Class notes
  - Posted on the web

Grading

- Exams (60%)
  - Three midterm exams in class (20% each)
  - For distance learning students, you should have your manager proctor the exam
- Homework (10%)
  - Collaboration is allowed, but independent simulations and write-ups
  - Need to setup CADENCE simulation environment
  - No late homework will be graded
- Laboratory (20%)
  - Lab will start on the third week (Jan. 31)
  - Need to complete NDA for 180nm process access
- Final Project (10%)
  - Groups of 1-3 students
  - Report and PowerPoint presentation required

Preliminary Schedule

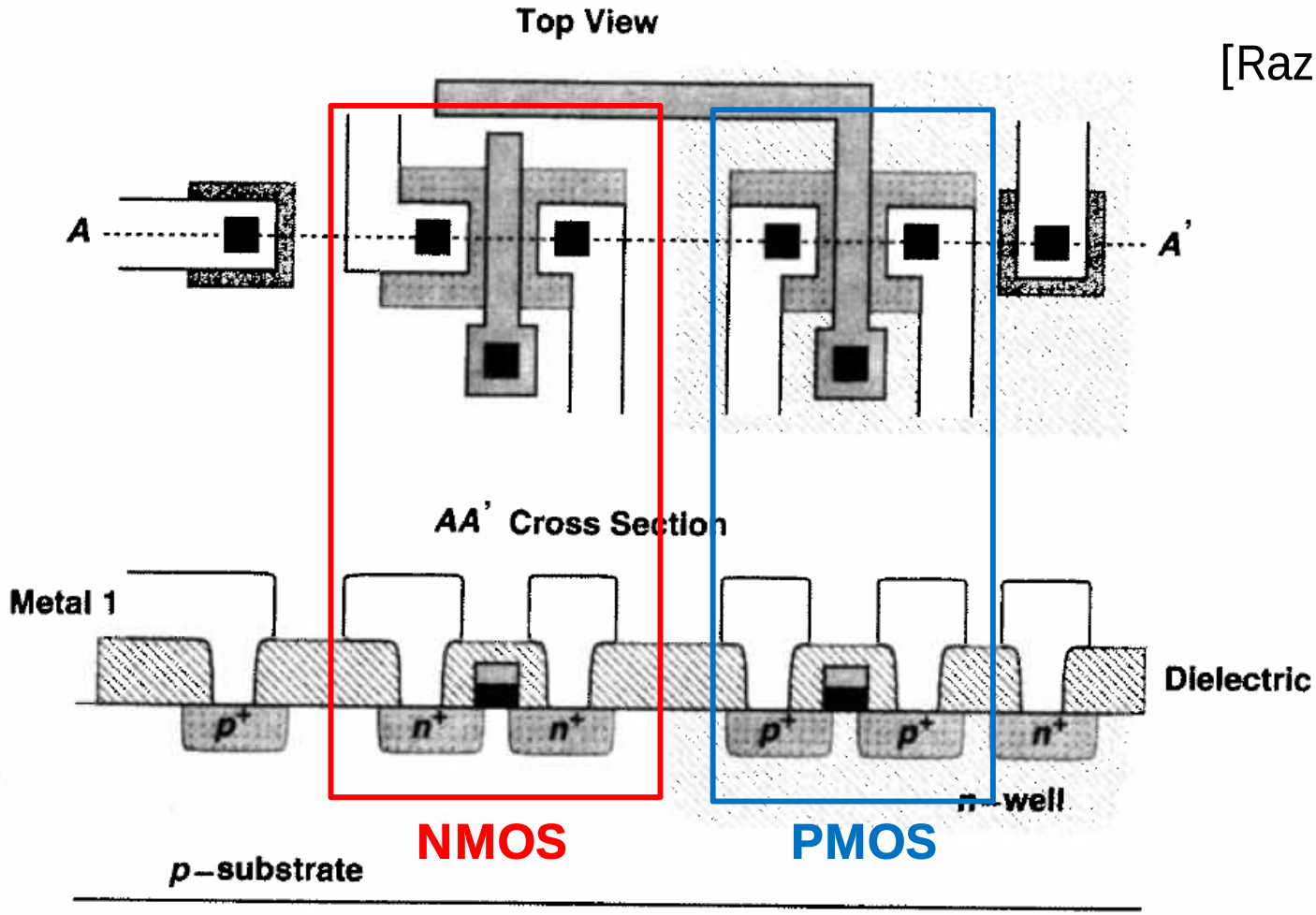
	Topic	Week
I.	Introduction and MOS models	Week 1-4
II.	CMOS Technologies and Layouts	
	Review Session	**Feb. 8**
	1st Exam	**Feb. 13**
III.	Current Mirrors and Differential Pairs	Week 5-9
IV.	Voltage References and Differential Pairs	
V.	OTA Design (Part 1)	
	Review Session	**Mar. 27**
	2nd Exam	**Mar. 29**
VI.	OTA Design (Part 2)	Week 10-14
VII.	Miller OpAmp Design	
VIII.	Advanced Topics	
	Review Session	**Apr. 24**
	3rd Exam	**Apr. 26**
	Project Report Due	**May 1**
	Project Presentation	**May 3 (3:00PM-5:00PM)**

- Dates may change with reasonable notice

CMOS Technology Overview

- MOS Transistors
- Interconnect
- Diodes
- Resistors
- Capacitors
- Inductors
- Bipolar Transistors

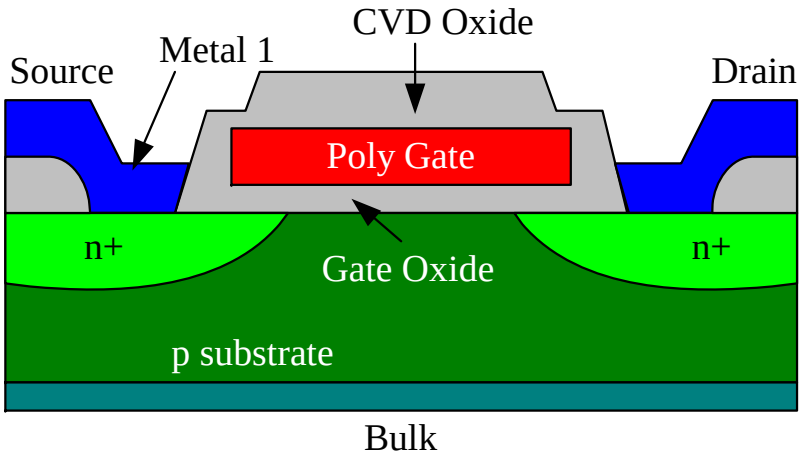
CMOS Technology



[Razavi]

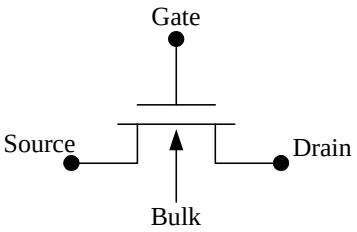
- Why p-substrate?
  - Easier to build n-wells vs p-wells
  - Allows for overall reduced doping levels

NMOS Transistor

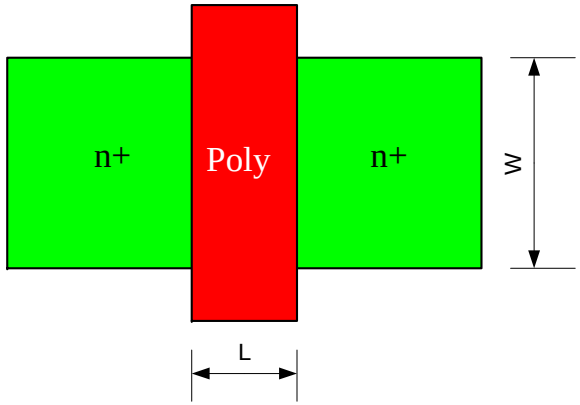


[Silva]

Cross Section

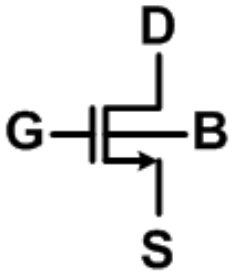


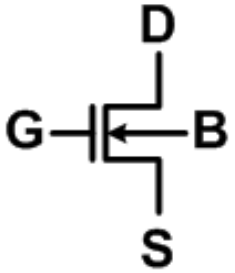
Circuit Symbol

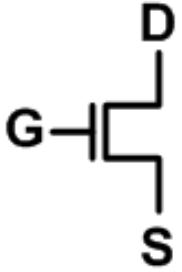


Top View

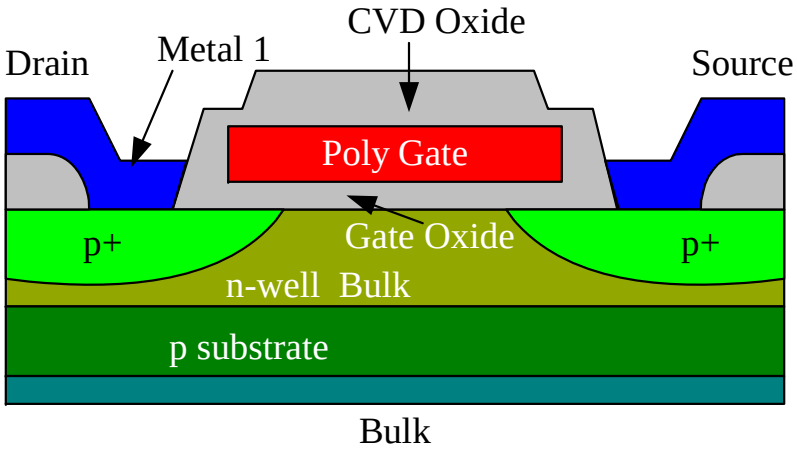
NMOS Symbols





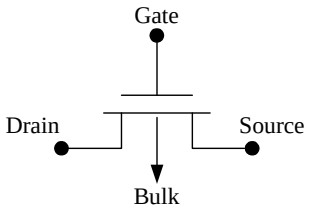


PMOS Transistor

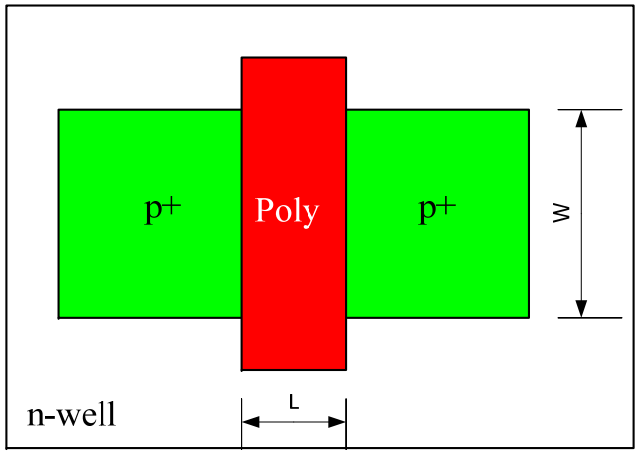


[Silva]

Cross Section

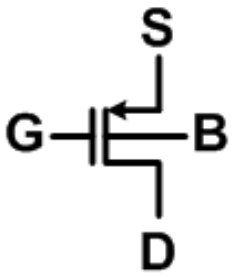


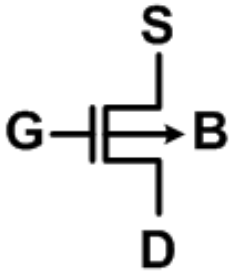
Circuit Symbol

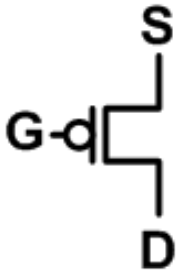


Top View

PMOS Symbols

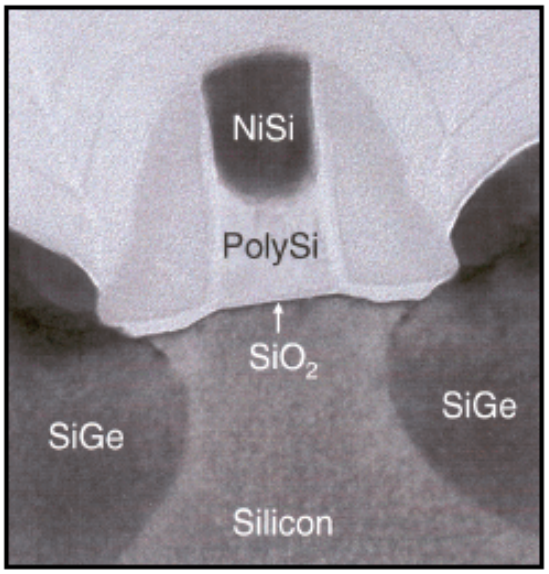






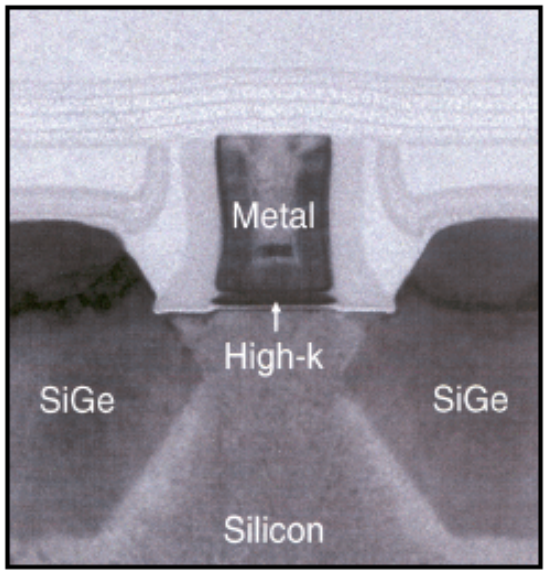
Today's Planar CMOS Transistors

65 nm Transistor



SiO_2 dielectric
Polysilicon gate electrode

45 nm HK+MG [Bohr ISSCC 2009]

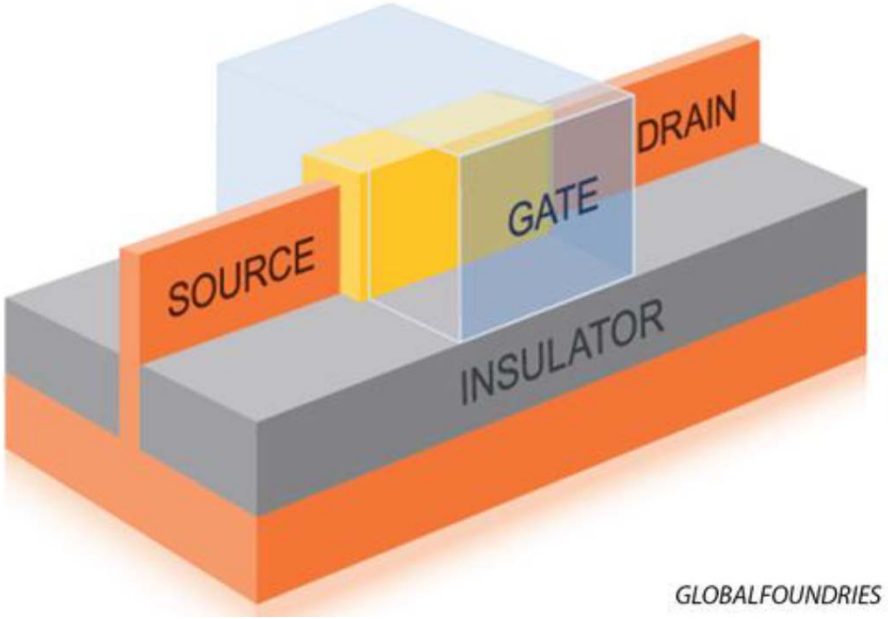


Hafnium-based dielectric
Metal gate electrode

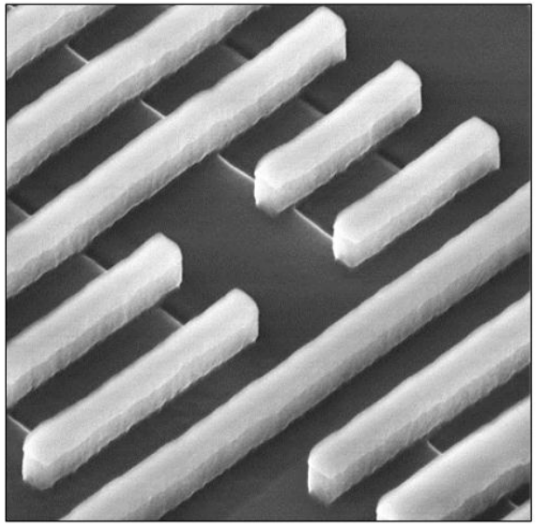
- Today's transistors have advanced device structures
- Modern transistors are moving from poly-gates back to metal-gates
  - Allows for High-K gate dielectric and reduced gate leakage current

FinFET Transistors

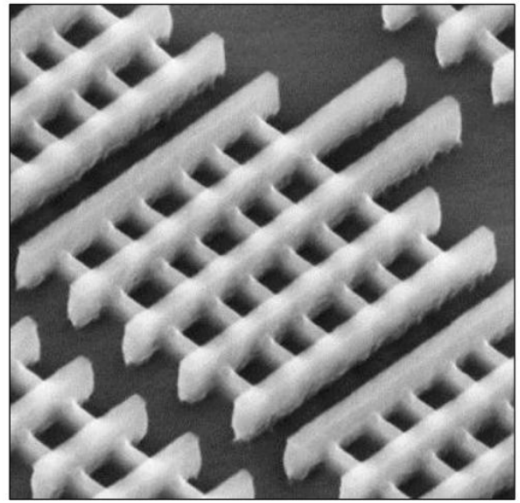
[Bohr 2011]



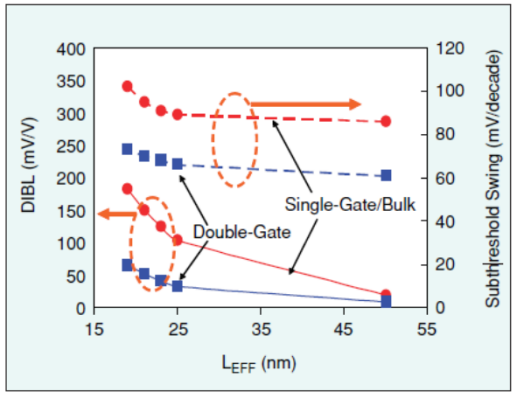
32nm Planar Transistors

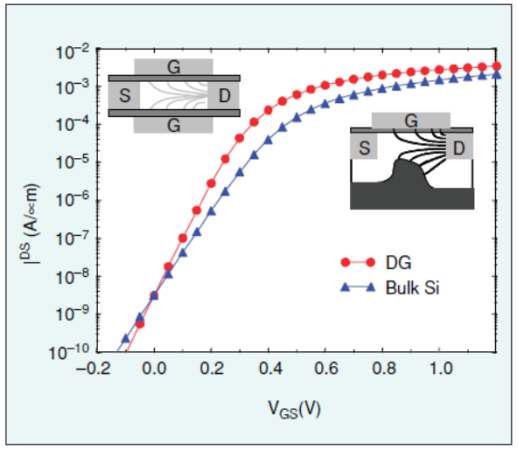


22nm FinFET Transistors



[Nowak IEEE 2004]





- Introducing a vertical 3rd-dimension allows for better gate control and superior device performance
- The most advanced CMOS processes are based on these FinFET devices

In the graphs above “Double-Gate” means the FinFET transistor

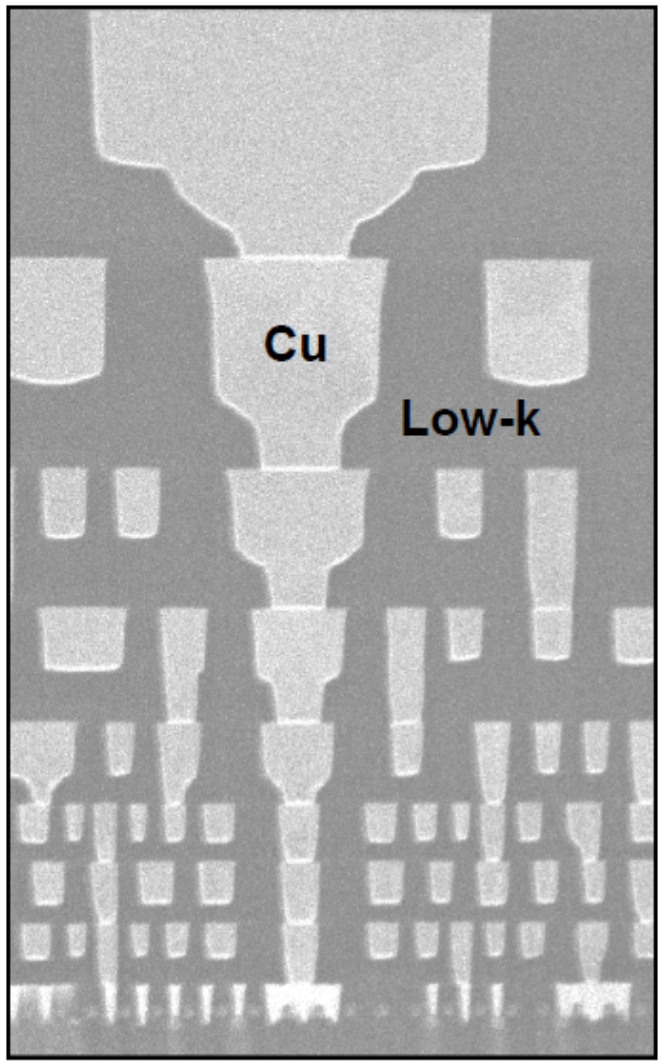
Interconnect (Wires)

Loose pitch + thick metal on upper layers

- High speed global wires
- Low resistance power grid

Tight pitch on lower layers

- Maximum density for local interconnects

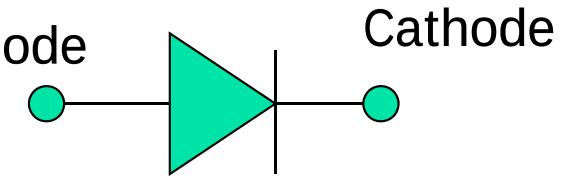


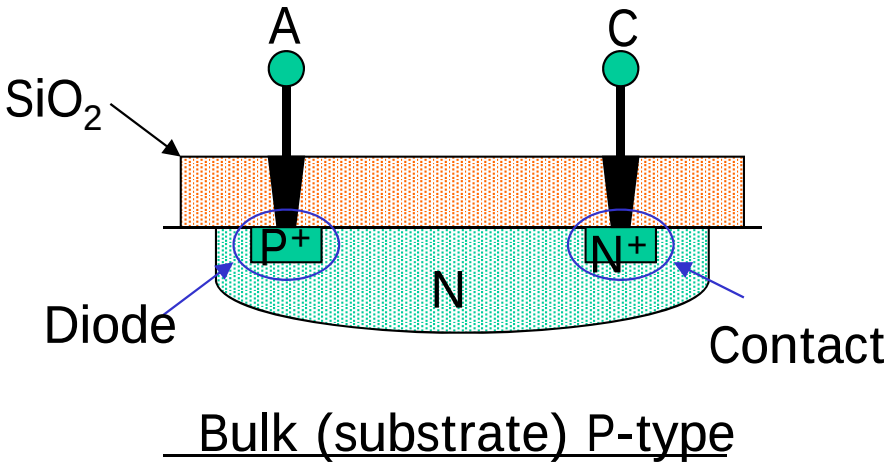
	Pitch (nm)
M8	810
M7	560
M6	360
M5	280
M4	240
M3	160
M2	160
M1	160

[Bohr ISSCC 2009]

Diodes

[Silva]





Typical values:

$P^+ = 10^{17}$-10^{19} acceptors /cm^3

$P = 10^{15}$-10^{17} acceptors /cm^3

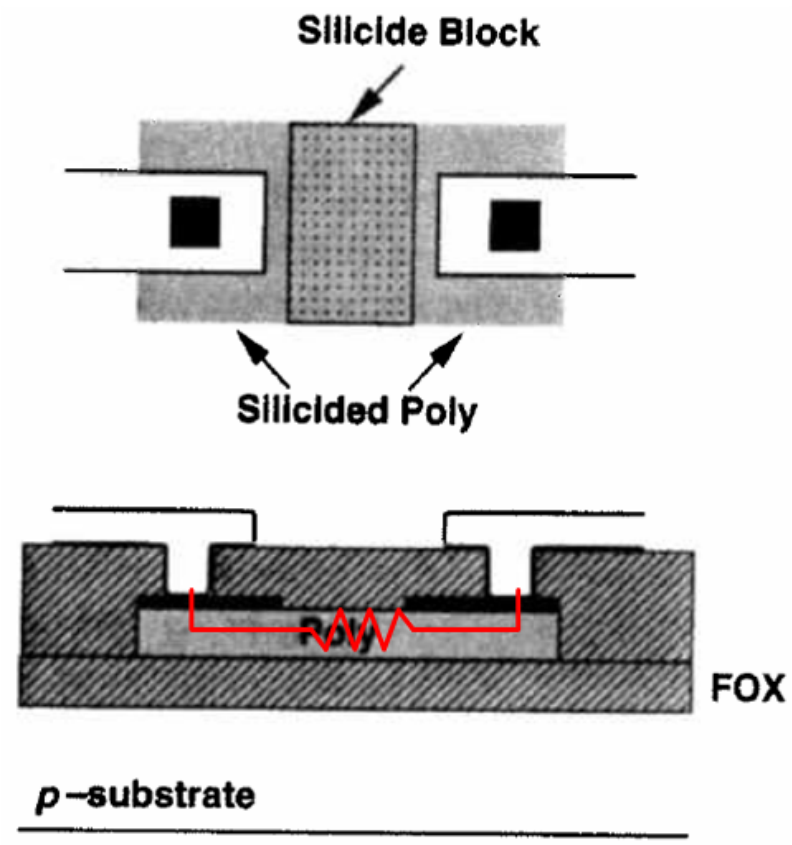
$N = 10^{16}$-10^{18} donors/cm^3

$N^+ = 10^{17}$-10^{19} donors/cm^3

Metal $\rightarrow$ 5×10^{22} electrons/cm^3

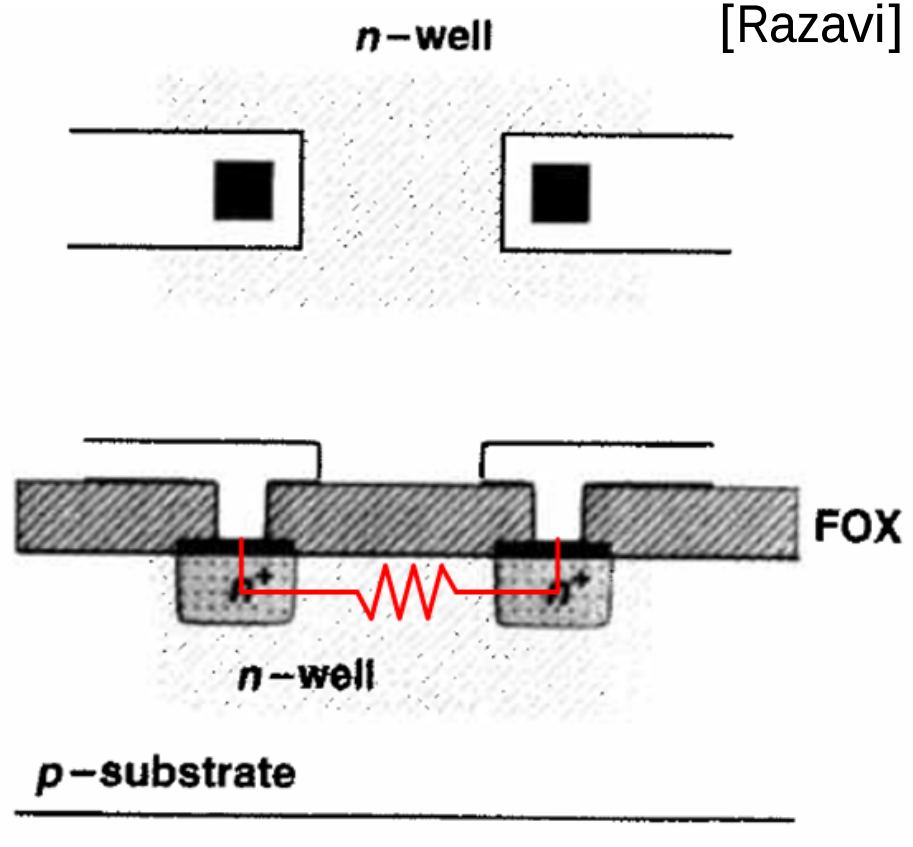
Resistors

Poly Resistor



Nwell Resistor

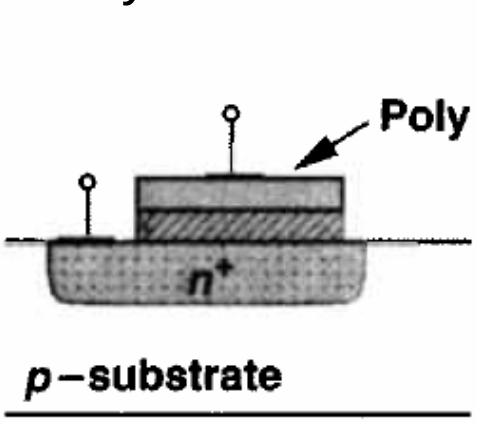
[Razavi]



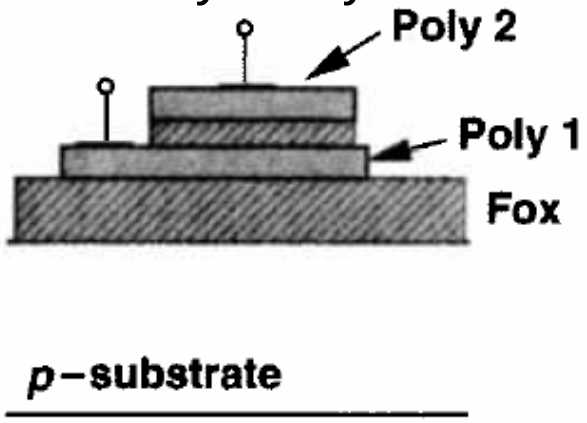
- Different resistor types have varying levels of accuracy and temperature and voltage sensitivities

Capacitors

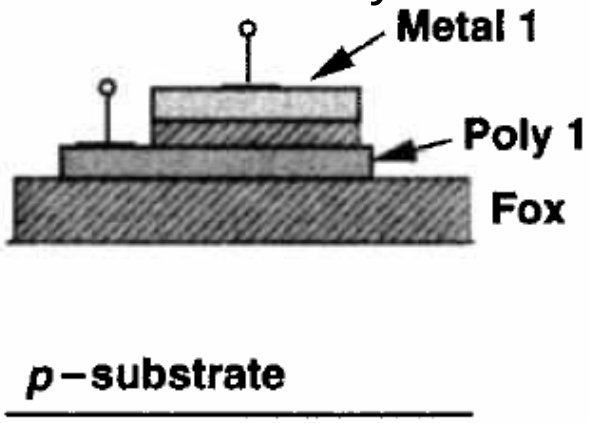
Poly - Diffusion



Poly - Poly

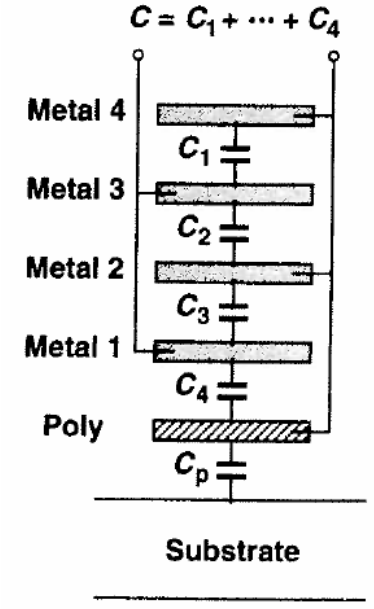


Metal1 - Poly

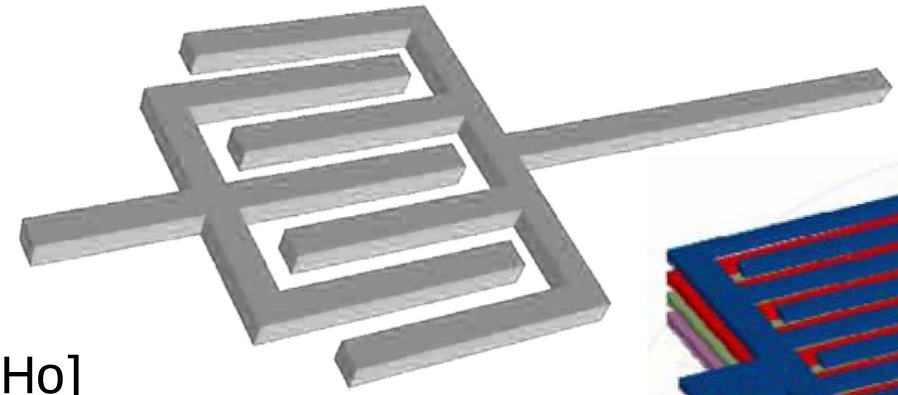


[Razavi]

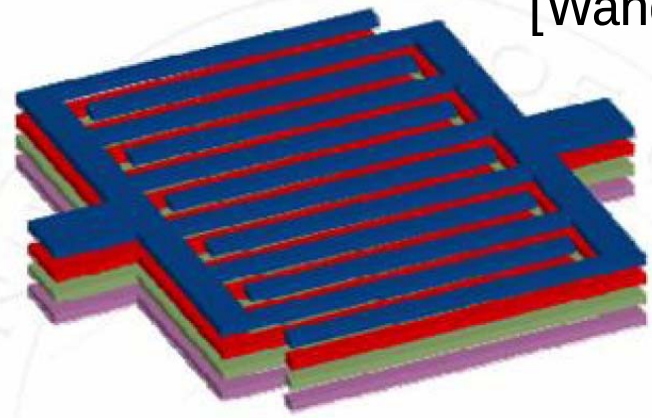
Vertical Metal “Sandwich”



Lateral Metal-Oxide-Metal (MOM)



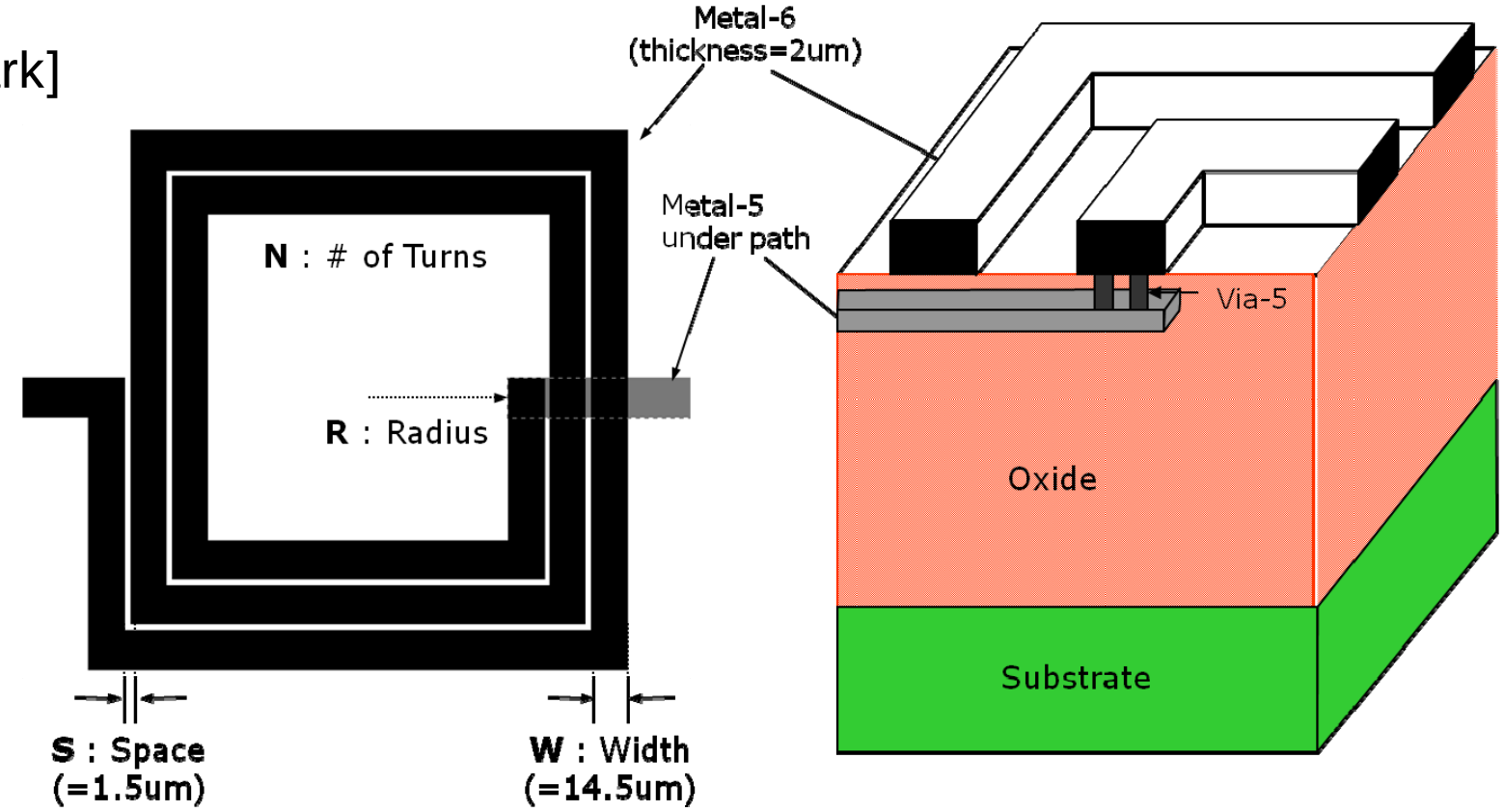
[Ho]



[Wang]

Inductors

[Silva/Park]

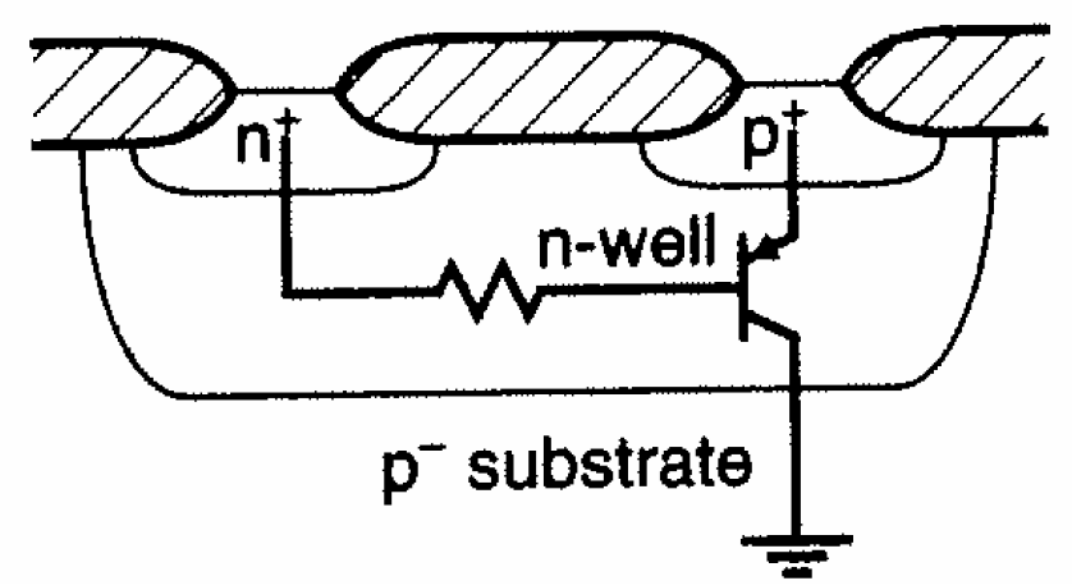


- Inductors are generally too big for widespread use in analog IC design
  - Can fit thousands of transistors in a typical inductor area (100μm x 100μm)
- Useful to extend amplifier bandwidth at zero power cost (but significant area cost)

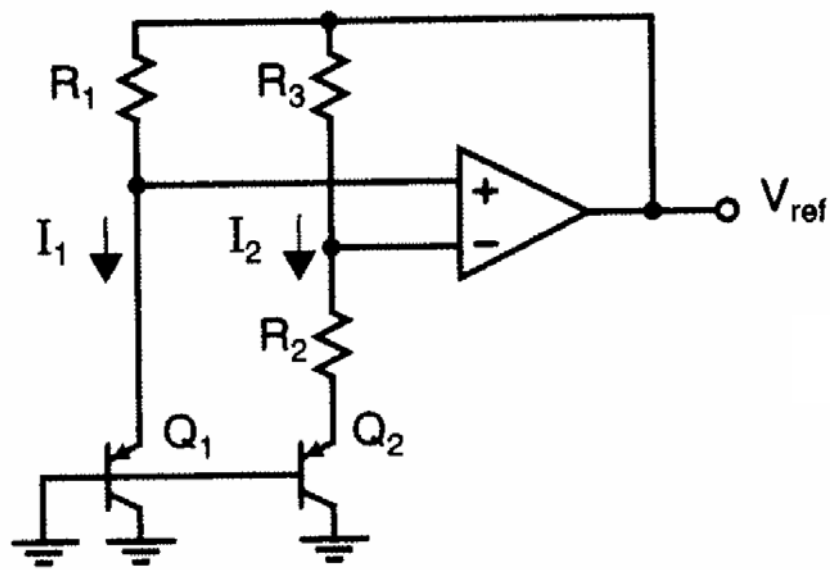
Bipolar Transistors – Vertical PNP

[Johns]

Vertical PNP



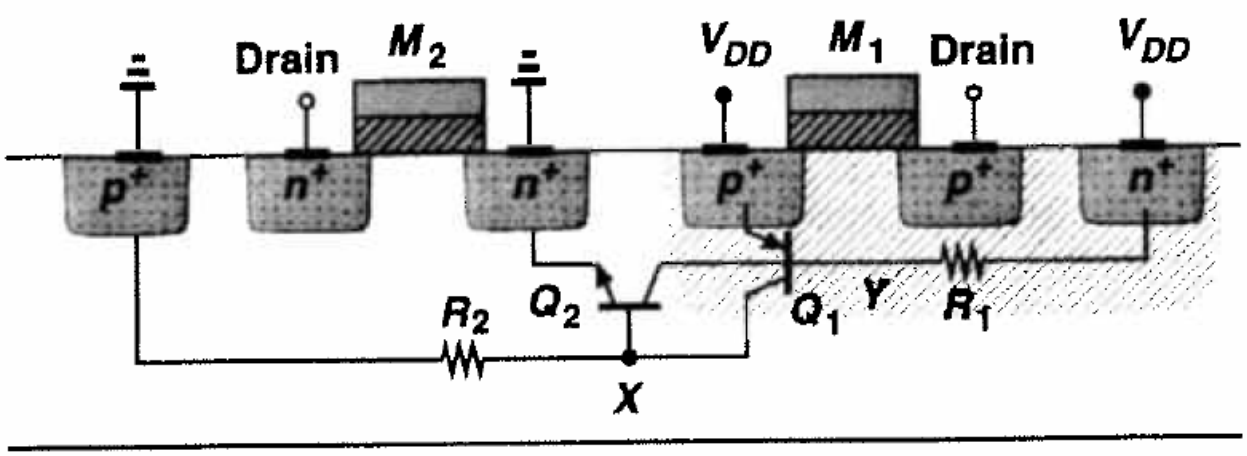
Bandgap Reference



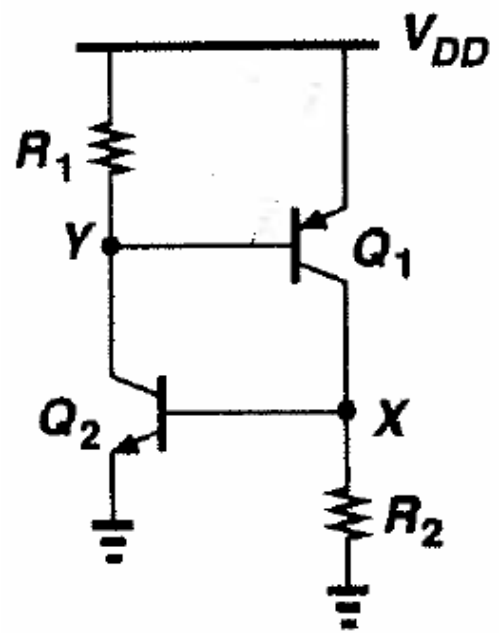
- Useful in a precise voltage reference circuit commonly implemented in ICs (Bandgap Reference)

Bipolar Transistors – Latchup

[Razavi]



Equivalent Circuit



- Potential for parasitic BJTs (Vertical PNP and Lateral NPN) to form a positive feedback loop circuit
- If circuit is triggered, due to current injected into substrate, then a large current can be drawn through the circuit and cause damage
- Important to minimize substrate and well resistance with many contacts/guard rings

Next Time

- MOS Transistor Modeling
  - DC I-V Equations
  - Small-Signal Model