ECEN 474

Homework #2 Notes

Due: 3-6-2018, 5:00PM

Homeworks will not be received after due.

Instructor: Sam Palermo

1. (50 points) Technology Characterization for Design

In this problem, we will extract some of the key MOSFET parameters used in circuit design. For all the following, extract the required data and plots for both the NMOS AND the PMOS device. For the PMOS device swap the polarity of the given bias conditions, i.e use V_{SD} for V_{DS} and V_{SG} for V_{GS} .

- a) Threshold Voltage Dependency on Width & Length.
 - Plot V_T vs Length for a range of $0.18\mu m \le L \le 1\mu m$. Use W=2 μm and $V_{DS}=V_{GS}=0.9V$. (one plot w/ one curve for both NMOS and PMOS versions)
 - Plot V_T vs Width for a range of $0.5\mu m \le W \le 6\mu m$. Plot for L=0.18 μm , L=0.36 μm , and L=0.72 μm . Use $V_{DS}=V_{GS}=0.9V$. (one plot w/ 3 curves for both NMOS and PMOS versions)

For parts (a)-(d), I used the following schematic in Cadence. It has 3 transistors which all have a default W=2 μ m, but transistor N0 has L=0.18 μ m, N1 has L=0.36 μ m, and N2 has L=0.72 μ m.



Unfortunately, Cadence Analog Design Environment (ADE) does not by default save the operating point information of the transistors and, to my knowledge, you cannot directly tell ADE to do this through any of the menus. In order to do this you must include a "Definition File", which I call "saveop.scs". This file has the following three lines to save the three transistors' operating point information:

save TN0:all save TN1:all save TN2:all

То	include	the file	in the	simulation,	in the	ADE windo	w:
				,			

C Virtue	so® Analo	og Desigr	n Environme	ent (2) - ECE	474_704 hw	2_1 schemati	c			-		×
Launch	S <u>e</u> ssion	Set <u>u</u> p	<u>A</u> nalyses	<u>V</u> ariables	<u>O</u> utputs	<u>S</u> imulation	<u>R</u> esults	<u>T</u> ools	Calibre	<u>H</u> elp	cāder	nce
11 📇 🧔) [c	27	🔊 🏃	• 🖄 🛛	1 🖻	_	_		_			
Design V 1 p5von	ariables Iame Y	0	Value		jalyses ype Ena	lble		Argum	ents		? @ X	AC DC Trans
				0	itputs Name/Si	gnal/Expr	Value	Plot	Save	Save (? 🗗 🗙 Options	
												M
>				Plot	: after simu	lation: Auto	_	Plottin	g mode:	Replace		
mouse L	:					M:						R:
6(14)							Status: F	Ready	T=27 C	C Simu	ulator: spe	ctre 📘
ect Setup ->	Simulat	ion Fi	les. Yo	u should	l get a v	vindow w	which lo	oks l	ike this	S		
spectre1: Simu	ation File	s Setup										
Paths/Files	Vec	tor File:	IS									
Files	/Paths			_		_						_
	:k here to	o add a	. path>									
Clin	ies es/grad/ł :k here to	nwyang biaddia	;/ECE474 file>	_2016s/sa	iveop.scs							×
Sumulus Fil	es :k here to) add a	file>									

 \times

OK Cancel Apply Help

Click on "Click here to add a file" in the Definition Files part and browse to the path of your "saveop.scs" file. Click "OK" and it should save the transistor operating point info during the simulations.

All the simulation data for the first problem should be extracted with DC simulations. To simulate the first part of part (a), you just need to look at one of the transistors because I ask you to sweep L with only one $W=6\mu m$. Here are the settings I use:

🔀 Choosing Analyses Virtuoso ® Analog Design Environment (2) 🛛 🗙								
Analysis	 tran xf pz pac psp qpxf hbnoise 	 dc sens sp pstb qpss qpsp 	 ac dcmatch envlp pnoise qpac hb 	 noise stb pss pxf qpnoise hbac 				
		DC Ana	alysis					
Save DC Operating Point								
Sweep Va	riable				_			
🔲 Temper	ature	Co	mponent Nan	ne /TNO				
📃 Design	Variable		Select	t Component				
Component Parameter Parameter Name 1 Model Parameter								
Sweep Ra	nge							
🖲 Start-S	itop .	tort 0 1	0	Stop 1.	_			
🔾 Center	-Span		.00	Stop Id				
Sweep Tyj	ре	~ ~						
Linear		 Step 	p Size	100				
		UNUT	uper of Stebs					
Add Specifi	c Points 📃							
Enabled 🖌				Options	.)			
	ОК	Cano	el Defaul	Its Apply F	elp			

Here I am sweeping the Component Transistor "/TN0" and Parameter "I" from $0.18\mu m$ to $1\mu m$ with 100 points. After running the simulation, in the ADE select Tools -> Results Browser and the following window should pop up.



Double click on "dc-dc" and you should be able to see the DC simulation outputs, including all the operating point information. Double-click on TN0/vth and it should plot it for you as shown above. (Note, plot background is black by default)

To simulate the second part of part (a), you need to look at all three transistors because I ask you to sweep W for the 3 Ls. In order to do this in one simulation, I create a "Design Variable" called "wtest" which is the common width of the transistors. For all 3 transistors in the schematic, I "Edit Object Properties" (select and press "q") and change the "Width" to "wtest", as shown below.

Browse	Reset Instance Labels Display	
Property	Value	Display
Library Name	cmhv7sf	off 🔽
Cell Name	nfetx	value 🧧
View Name	symbol	off 🔽
Instance Name	TNO	off 🔽
	Add Delete Modify	v)
User Property	Master Value Local Valu	e Display
permuteRule	(p D S)	off 🔽
CDF Parameter	Value	Display
Description	1.8V NFET	off
Width Single Finger	wtest M	off 🔽
Width All Fingers	(wtest) M	off 🔽
Length	180.0n M	off 🔽
Number of Fingers	1	off 🔽
Multiplicity	1	off 🔽
S/D CA space multiplier	1	off 🔽
Gate Connection	1 🔽	off 🔽
Interdigited Layout?		off 🔽
Fet Configuration	n_bb 🔽	off 🔽
Modify CA vs Gate space		off 🔽
Modify CA vs Diff. space		off 🔽
Source Drain Metal Width	0.24	off 🔽
CA on Left edge	⊻	off 🔽
CA on Right edge	⊻	off 🔽
Add Top Gate Contact		off 🔽
Add Bot Gate Contact		off 🔽
Num diff CA columns	● 1 ○ 2	off 🗖

In the ADE, you will need to set the default variable value by selecting Variables ->Edit

Name = wtest Value (Expr) = 6u

Note, this is the default value

Now your ADE window should look as follows, with the Design Variables info on the left.



Here are the settings I use for the DC simulation:

🔀 Choosing A	Analyses Vi	rtuoso® A	Analog Design	Environment (2)	×			
Analysis	 tran xf pz pac psp qpxf hbnoise 	 dc sens sp pstb qpss qpsp 	 ac dcmatch envlp pnoise qpac hb 	 noise stb pss pxf qpnoise hbac 				
		DC Ana	dysis					
Save DC Op Hysteresis S\	erating Poin weep	t ⊻	.,					
Sweep Variable Temperature Design Variable Component Parameter Model Parameter								
Sweep Ran Start-S	ge op _S Span	tart 0.5	u 8	itop 6u				
Sweep Type Linear	•	🔾 Step 🖲 Num	o Size nber of Steps	100				
Add Specific	Points 📃							
Enabled ⊻	ок	Canc	el Default	Options	.)			

Here I am sweeping the Design Variable "wtest" from $0.5\mu m$ to $6\mu m$ with 100 points. After running the simulation, refresh the results browser and you should be able to plot the three transistors' V_T on one plot as shown below.



- b) For a unit device finger of W=2µm and V_{DS}=0.9V, extract a data table with the following device parameters from a DC sweep of V_{GS} from 0 to 1.8V with a step size of 1mV. Extract three sets of data for L=0.18µm, L=0.36µm, and L=0.72µm.
 - V_{GS}, I_D, g_m, g_{ds}, V_T, C_{gg}, C_{gs}, C_{gd}, C_{dd}, C_{ss}, C_{jd}, C_{js}

To extract all this data, you simply need to run one DC simulation, sweeping V_{GS} from 0 to 1.8V. Here are the settings that I use:

🔀 Choosing	Analyses V	∕irtuoso®	Analog Desigr	Environment (2)	×
Analysis	 tran xf pz pac psp qpxf hbnoise 	 dc sens sp pstb qpss qpss 	ac dcmatch envlp pnoise qpac hb	 noise stb pss pxf qpnoise hbac 	
		DC An	alvsis		
Save DC O Hysteresis (perating Poir Sweep	nt 🗹	aiy 313		
Sweep Va Temper Design Compo Model	riable ature Variable nent Parame Parameter	Ci ter Pa	omponent Nam Select trameter Nami	ne /V1 t Component e dc	
Sweep Ra Start-S Center Sweep Tyl Linear	nge Stop g - Span pe	Start 0 • Ste • Nu	P Size mber of Steps	Stop 1.8	
Add Specifi	c Points 📃				
Enabled 🖌	ОК	Can	cel Defaul	Option Its Apply	s Help

Here I am sweeping the Component Voltage Source "/V1" and Parameter "dc" from 0 to 1.8V with a step of 1mV. After running the simulation, I would suggest to NOT USE THE CALCULATOR TO PLOT THE REMAINING PLOTS, as the cadence calculator is somewhat inconvenient to use. Instead, I would save the data to a text file and plot the remaining plots using MATLAB.

In order to extract the data, type the following four lines in the main cadence CIW command window:

	🚺 Virtuoso® 6.1.5 - Log: /homes/grad/hwyang/CDS.log	-		×
	Eile Tools Options IBM_PDK Help		cāde	nce
	t > envSetVal("ui" "ciwCmdInputLines" 'int 9) t envSetVal("ui" "ciwCmdInputLines" 'int 8) t			
	<pre>selectResult('dc) ocnPrint(?output "~/nom_w6_0p18_vgs.dat" ?numberNotation 'scientific g</pre>	etData("	ENO:d"),	get
	ocnPrint(?output "~/nom_w6_0p36_vgs.dat" ?numberNotation 'scientific g	etData("	EN1:d"),	get≣
	ocnPrint(?output "~/nom_w6_0p72_vgs.dat" ?numberNotation 'scientific g	etData("	EN2:d"),	get
ĺ	mouse L: M:			R:

selectResult('dc)

ocnPrint(?output "~/nom_w6_0p18_vgs.dat" ?numberNotation 'scientific getData("TN0:d"), getData("TN0:gm"), getData("TN0:gds"), getData("TN0:vth"), getData("TN0:cgg"), getData("TN0:cgs"), getData("TN0:cgd"), getData("TN0:cdd"), getData("TN0:css"), getData("TN0:cjd"), getData("TN0:cjs"))

ocnPrint(?output "~/nom_w6_0p36_vgs.dat" ?numberNotation 'scientific getData("TN1:d"), getData("TN1:gm"), getData("TN1:gds"), getData("TN1:vth"), getData("TN1:cgg"), getData("TN1:cgs"), getData("TN1:cgd"), getData("TN1:cdd"), getData("TN1:css"), getData("TN1:cjd"), getData("TN1:cjs"))

ocnPrint(?output "~/nom_w6_0p72_vgs.dat" ?numberNotation 'scientific getData("TN2:d"), getData("TN2:gm"), getData("TN2:gds"), getData("TN2:vth"), getData("TN2:cgg"), getData("TN2:cgs"), getData("TN2:cgd"), getData("TN2:cd"), getData("TN2:css"), getData("TN2:cjd"), getData("TN2:cjs"))

Hit return and this should write the data to 3 text files in your home directory (the ?output variable is the file name). The data is written in column format in the order as given above with an additional first variable being the sweep parameter " V_{GS} ". Note in order to load the data into MATLAB for plotting, you will need to delete the header in the top line of the three data files. Also, potentially typing the above lines multiple times can be tedious. So I generally create a text file with the above lines and "copy-and-paste" the lines into the main cadence window using the mouse middle button.

In MATLAB, you can use the following command to import the data from the *.dat file.

- c) Essential Design Plots. Using the table data from part (b), plot the following
 - $g_m/I_D vs V_{ov} = V_{GS} V_T$
 - $g_m/g_{ds} vs g_m/I_D$
 - $f_T vs g_m/I_D$
 - $I_D/W vs g_m/I_D$

For the 4 plots for both the NMOS and PMOS versions, each one should have 3 curves for the 3 channel lengths.

- d) Other Useful Design Plots. Using the table data from part (b), plot the following
 - $g_{ds}/W vs g_m/I_D$
 - $C_{gg}/W vs g_m/I_D$
 - $C_{dtotal}/W \text{ vs } g_m/I_D$, where $C_{dtotal}=C_{dd}+C_{jd}$
 - $C_{stotal}/W vs g_m/I_D$, where $C_{stotal}=C_{ss}+C_{js}$

For the 4 plots for both the NMOS and PMOS versions, each one should have 3 curves for the 3 channel lengths.

Grading is 2.5points/plot for the 20 total plots.

2. (50 points) Table-Based (g_m/I_D) Design of Common-Source Amplifier

Using the table-based design procedure outlined in Lecture 7, design the common-source amplifier below to satisfy the following specifications.

- 0.18µm technology
- $|A_v| \ge 5V/V$
- $f_u \ge 200 MHz$
- $C_L = 5pF$
- Vdd = 1.8V

Design procedure counts for 30 points.

Turn in the following to validate the design performance:

- Schematic with DC operating points and the bias current labeled (5 points)
- Print-out with small-signal device parameters. Highlight the critical small-signal parameters, such as g_m , g_{ds} , etc. (5 points)
- AC frequency response with the DC gain and unity-gain frequency labeled. (10 points)

