ECEN 474/704

Homework #2

Due: 3-6-2018, 5:00PM

Homeworks will not be received after due.

Instructor: Sam Palermo

1. **(50 points)** Technology Characterization for Design

In this problem, we will extract some of the key MOSFET parameters used in circuit design. For all the following, extract the required data and plots for both the NMOS AND the PMOS device. For the PMOS device swap the polarity of the given bias conditions, i.e use V_{SD} for V_{DS} and V_{SG} for $V_{GS.}$

  a) Threshold Voltage Dependency on Width & Length.
- Plot V_T vs Length for a range of $0.18\mu m \leq L \leq 1\mu m$. Use W=2$\mu$m and $V_{DS}=V_{GS}$=0.9V. (one plot w/ one curve for both NMOS and PMOS versions)
- Plot V_T vs Width for a range of $0.5\mu m \leq W \leq 6\mu m$. Plot for L=0.18$\mu$m, L=0.36$\mu$m, and L=0.72$\mu$m. Use $V_{DS}=V_{GS}$=0.9V. (one plot w/ 3 curves for both NMOS and PMOS versions)

  b) For a unit device finger of W=2μm and V_{DS}=0.9V, extract a data table with the following device parameters from a DC sweep of V_{GS} from 0 to 1.8V with a step size of 1mV. Extract three sets of data for L=0.18μm, L=0.36μm, and L=0.72μm.
- V_{GS}, I_D, g_m, g_{ds}, V_T, C_{gg}, C_{gs}, C_{gd}, C_{dd}, C_{ss}, C_{jd}, C_{js}

I suggest using the schematic below to obtain the three sets of NMOS data with one simulation. Note, the 0V DC source between the transistors' source nodes and ground (bulks) is to allow the simulator to report a non-zero value for C_{js}. If the source and bulk are shorted, C_{js} is reported as zero.
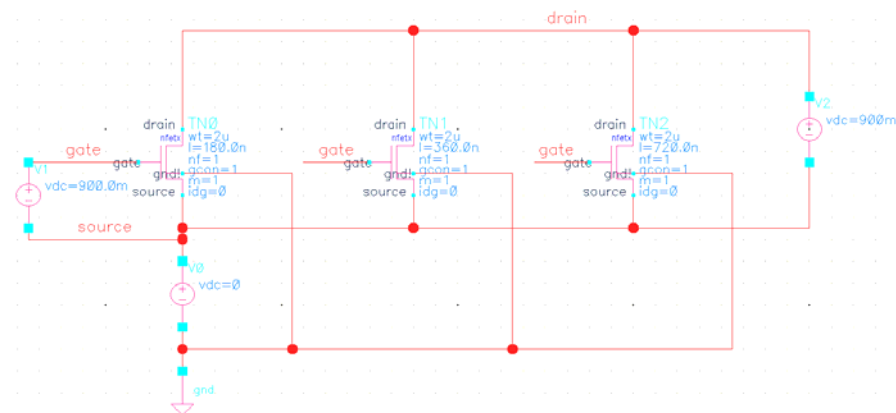
  c) Essential Design Plots. Using the table data from part (b), plot the following
- g_m/I_D vs $V_{ov}=V_{GS}-V_T$
- g_m/g_{ds} vs g_m/I_D
- f_T vs g_m/I_D
- I_D/W vs g_m/I_D

For the 4 plots for both the NMOS and PMOS versions, each one should have 3 curves for the 3 channel lengths.

d) Other Useful Design Plots. Using the table data from part (b), plot the following
  - g_{ds}/W vs g_m/I_D
  - C_{gg}/W vs g_m/I_D
  - C_{dtotal}/W vs g_m/I_D, where $C_{dtotal}=C_{dd}+C_{jd}$
  - C_{stotal}/W vs g_m/I_D, where $C_{stotal}=C_{ss}+C_{js}$

  For the 4 plots for both the NMOS and PMOS versions, each one should have 3 curves for the 3 channel lengths.

Grading is 2.5points/plot for the 20 total plots.

2. **(50 points)** Table-Based (g_m/I_D) Design of Common-Source Amplifier
Using the table-based design procedure outlined in Lecture 7, design the common-source amplifier below to satisfy the following specifications.
  - 0.18µm technology
  - $|A_v| \geq 5V/V$
  - $f_u \geq 200MHz$
  - $C_L = 5pF$
  - Vdd = 1.8V

Design procedure counts for 30 points.

Turn in the following to validate the design performance:
  - Schematic with DC operating points and the bias current labeled (5 points)
  - Print-out with small-signal device parameters. Highlight the critical small-signal parameters, such as g_m, g_{ds}, etc.   (5 points)
  - AC frequency response with the DC gain and unity-gain frequency labeled. (10 points)