Texas A&M University
Department of Electrical and Computer Engineering

ECEN 474/704 – (Analog) VLSI Circuit Design

Spring 2016

Exam #1

Instructor: Sam Palermo

- Please write your name in the space provided below
- Please verify that there are **5** pages in your exam
- You may use <u>one</u> double-sided page of notes and equations for the exam
- Good Luck!

Problem	Score	Max Score
1		40
2		40
3		20
Total		**100**

Name: SAM PALERMO

UIN:

Problem 1 (40 points)

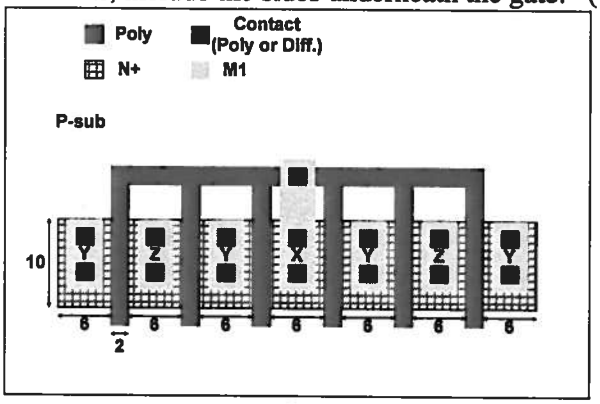
For the layout below, assume that all the commonly labeled diffusion areas are connected with the appropriate metal layers. Assume that V_X=1.2V, V_Y=0V, V_Z=0.4V, V_{T0}=0.7V, γ=0, and that all Spice parameters are given (i.e. C_j, C_{jsw}, C_{jc}, C_{ox}, C_{ov}). The dimensions are given in µm, with all the poly gates having a length of 2µm and L_D=0.1µm.

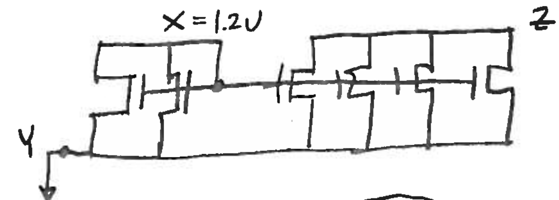
a) Draw the equivalent circuit. Combine all parallel transistors and given the total width and length of the equivalent transistors. (15 points)

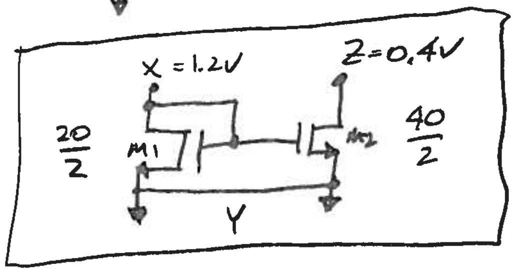
b) What region(s) are the transistors operating in? (5 points)

c) **For node X only**, give an expression and calculate the total gate cap. (10 points)

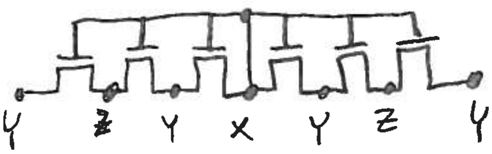
d) **For node Z only**, give an expression and calculate the total junction cap. Note for the perimeter terms, include the sides underneath the gate. (10 points)







a. All unit transistors 10/2



b. M1 ⇒ $V_{GS} = V_{DS} = 1.2V > V_T$

$V_{DS} > V_{GS} - V_T$ ⇒ **Saturation**

M2 ⇒ $V_{GS} = 1.2V > V_T$

$V_{DS} = 0.4V$ $V_{GS} - V_T = 1.2V - 0.7V = 0.5$

$V_{DS} < V_{GS} - V_T$ ⇒ **Triode**

c. For C_{gx} ⇒ M1 = Sat ⇒ $C_{gs} + \cancel{C_{gd}}$ (shorted out) $= \frac{2}{3}(20\mu)(1.8\mu)C_{ox} + 20\mu C_{ov} = 24\mu^2 C_{ox} + 20\mu C_{ov}$

M2 = Triode = $C_{gs} + C_{gd} = 2\left[\frac{1}{2}(40\mu)(1.8\mu)C_{ox} + 40\mu C_{ov}\right] = 72\mu^2 C_{ox} + 80\mu C_{ov}$

Total $C_{gX} = 96\mu^2 C_{ox} + 100\mu C_{ov}$

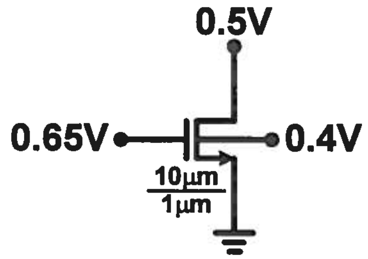
d. C_{jZ} ⇒ M2 = Triode ⇒ $C_{jZ} = A_Z C_j + P_Z C_{jsw} + C_{jc}\frac{W_2 L_{eff}}{2}$

$C_{jZ} = 2(6\mu)(10\mu)C_j + (2)(2)(6\mu + 10\mu)C_{jsw} + \frac{(40\mu)(1.8\mu)}{2}C_{jc}$

$C_{jZ} = 120\mu^2 C_j + 64\mu C_{jsw} + 36\mu^2 C_{jc}$

Problem 2 (40 points)

For the transistor below, assume V_{T0}=0.7V, γ=0.45$V^{1/2}$, and $2\Phi_F$=0.9V.



$$I_{DS} = I_o \exp\left(\frac{(V_{GS}-V_{Tn})q}{\zeta kT}\right)\left(1-\exp\left(-\frac{V_{DS}q}{kT}\right)\right) \quad \text{(Subthreshold)}$$

$$I_{DS} = B\frac{W}{L-2L_D}(V_{GS}-V_{Tn})^{\alpha}(1+\lambda V_{DS})\left(2-\frac{V_{DS}}{V_{DSAT}}\right)\left(\frac{V_{DS}}{V_{DSAT}}\right) \quad \text{(Triode)}$$

$$I_{DS} = B\frac{W}{L-2L_D}(V_{GS}-V_{Tn})^{\alpha}(1+\lambda V_{DS}) \quad \text{(Saturation)}$$

$$V_{Tn} = V_{T0} + \gamma\left(\sqrt{|2\Phi_F|+V_{SB}} - \sqrt{|2\Phi_F|}\right)$$

$$V_{DSAT} = V_{GS} - V_{Tn}$$

a. Calculate V_T and state the transistor's operation region. (10 points)

$$V_T = 0.7V + 0.45V^{1/2}\left(\sqrt{0.9V-0.4V} - \sqrt{0.9V}\right) = 0.591V$$

$$V_{GS} - V_T = 0.65V - 0.591V = 58.7mV$$

$$V_{DS} = 0.5V$$

$$V_{DS} > V_{GS} - V_T \Rightarrow \text{Saturation}$$

V_T = 0.591V

Operation Region = Saturation

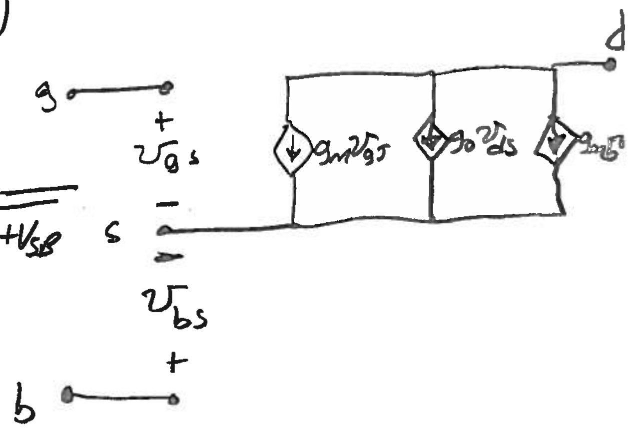
b. Using the appropriate I_{DS} equation above, **derive and sketch the small-signal model** of the transistor. **Include expressions for the g_m, g_o, and g_{mb}.** (20 points)

$$g_m = \frac{\partial I_{DS}}{\partial V_{GS}}\Big|_Q = B\frac{W}{L_{eff}}\alpha(V_{GS}-V_T)^{\alpha-1}(1+\lambda V_{DS})$$

$$g_o = \frac{\partial I_{DS}}{\partial V_{DS}}\Big|_Q = B\frac{W}{L_{eff}}(V_{GS}-V_T)^{\alpha}(\lambda)$$

$$g_{mb} = B\frac{W}{L_{eff}}\alpha(V_{GS}-V_T)^{\alpha-1}(-1)(-1)(1+\lambda V_{DS})\frac{\gamma}{2\sqrt{|2\Phi_F|+V_{SB}}}$$

$$= \frac{\gamma g_m}{2\sqrt{|2\Phi_F|+V_{SB}}}$$



c. Assume that B=65µA/V^{α}, λ=0.1V^{-1}, and L_D=0.1µm. Calculate the transistor's intrinsic gain (g_m/g_o) for both α=2 and α=1. (10 points)

$$\frac{g_m}{g_o} = \frac{B\frac{W}{L_{eff}}\alpha(V_{GS}-V_T)^{\alpha-1}(1+\lambda V_{DS})}{B\frac{W}{L_{eff}}(V_{GS}-V_T)^{\alpha}(\lambda)}$$

$$= \left(\frac{\alpha}{V_{GS}-V_T}\right)\left(\frac{1+\lambda V_{DS}}{\lambda}\right) \overset{\alpha=2}{\Longrightarrow} \left(\frac{2}{58.7mV}\right)\left(\frac{1+(0.1V^{-1})(0.5V)}{0.1V^{-1}}\right) = 358 V/V$$

α=2 Intrinsic Gain (g_m/g_o) = 358 V/V

α=1 Intrinsic Gain (g_m/g_o) = 179 V/V

Problem 3 (20 points)

Sketch a layout that matches **three** capacitors of unit size 2.2, 4.5, and 6.8. Assume that the unit capacitors are sized 5μm x 5μm. **Make sure to give the non-unit capacitor(s) dimensions.** In the sketch clearly label the critical dimensions and use at least 2 layout matching techniques. **Also, write specifically the 2 layout matching techniques that you are using.** Note, if you use a common-centroid layout technique, it doesn't have to have perfect center-of-mass matching, but it should be close.

Need to match $\frac{\text{Perimeter}}{\text{Area}}$ for all caps

"C1" for 2.2 cap ⟹ 1 unit cap + 1 non-unit cap w/ $A_{nu} = 1.2 A_u$ $(K_1 = 1.2)$

"C_2" for 4.5 cap ⟹ 3 unit caps + 1 non-unit cap w/ $A_{nu} = 1.5 A_u$ $(K_2 = 1.5)$

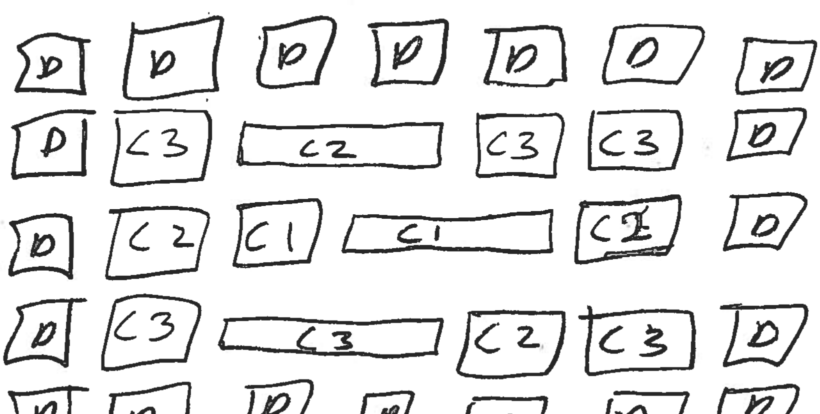
"C_3" for 6.8 cap ⟹ 5 unit caps + 1 non-unit cap w/ $A_{nu} = 1.8 A_u$ $(K_3 = 1.8)$

$y_{nu1} = x_u\left(K_1 - \sqrt{K_1^2 - K_1}\right)$

C1: $= 5\mu\left(1.2 - \sqrt{1.2^2 - 1.2}\right) = 3.55\mu$ $\quad x_{nu1} = \frac{K_1 x_u^2}{y_{n1}} = \frac{1.2(5\mu)^2}{3.55\mu} = 8.45\mu$

C2: $y_{nu2} = 5\mu\left(1.5 - \sqrt{1.5^2 - 1.5}\right) = 3.17\mu$ $\quad x_{nu2} = \frac{1.5(5\mu)^2}{3.17\mu} = 11.83\mu$

C3: $y_{nu3} = 5\mu\left(1.8 - \sqrt{1.8^2 - 1.8}\right) = 3\mu$ $\quad x_{nu3} = \frac{1.8(5\mu)^2}{3\mu} = 15\mu$



Layout Technique #1 = Dummies around entire perimeter

Layout Technique #2 = Common-Centroid (Approximately)

Scratch Paper