Texas A&M University
Department of Electrical and Computer Engineering

ECEN 474 – (Analog) VLSI Circuit Design

Fall 2012

Exam #1

Instructor: Sam Palermo

- Please write your name in the space provided below
- Please verify that there are **4** pages in your exam
- You may use <u>one</u> double-sided page of notes and equations for the exam
- Good Luck!

Problem	Score	Max Score
1		40
2		40
3		20
Total		**100**

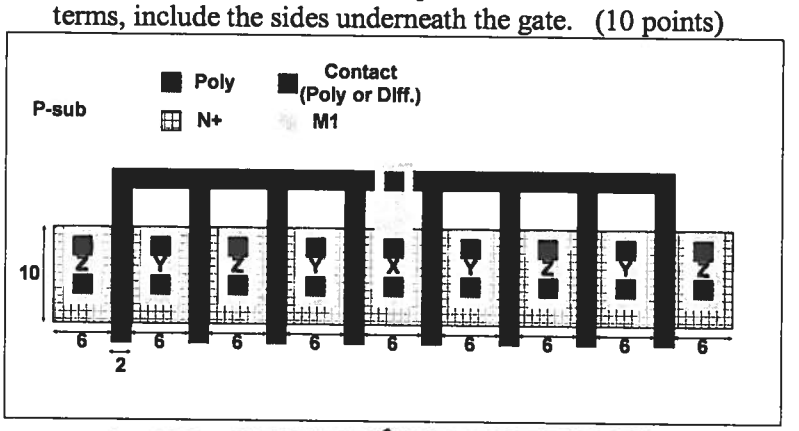
Name: SAM PALERMO

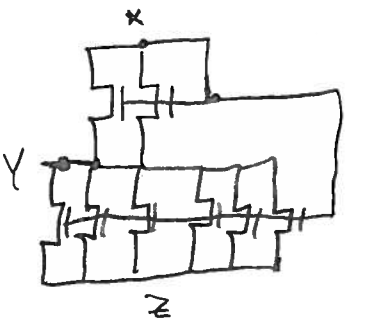
UIN: _____

Problem 1 (40 points)

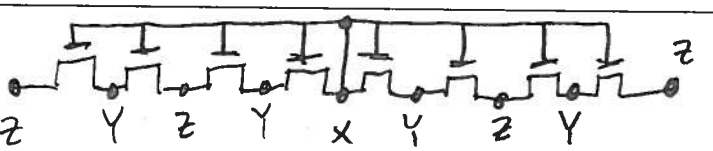
For the layout below, assume that all the commonly labeled diffusion areas are connected with the appropriate metal layers. Assume that V_X=1.5V, V_Y=1V, V_Z=0.5V, V_{T0}=0.7V, γ=0, and that all Spice parameters are given (i.e. C_j, C_{jsw}, C_{jc}, C_{ox}, C_{ov}). The dimensions are given in μm, with all the poly gates having a length of 2μm and L_D=0.1μm.

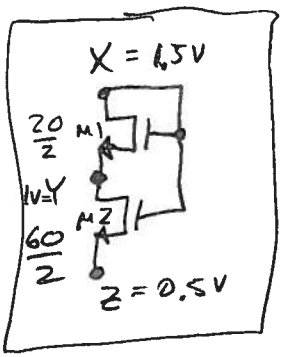
a) Draw the equivalent circuit. Combine all parallel transistors and given the total width and length of the equivalent transistors. (15 points)
b) What region(s) are the transistors operating in? (5 points)
c) **For node X only**, give an expression and calculate the total gate cap. (10 points)
d) **For node X only**, give an expression and calculate the total junction cap. Note for the perimeter terms, include the sides underneath the gate. (10 points)





a. All unit transistors 10/2





b. M1 $\Rightarrow V_{GS} = 1.5V - 1.0V = 0.5V$

$V_{DS} = 1.5V - 1.0V = 0.5V$

$V_{GS} < V_T = 0.7V \Rightarrow$ Cutoff or Subthreshold

M2 $\Rightarrow V_{GS} = 1.5V - 0.5V = 1.0V$

$V_{DS} = 1V - 0.5V = 0.5V$

$V_{GS} > V_T$ & $V_{DS} > V_{GS} - V_T = 0.3V$

Saturation

c. For $C_{gx} \Rightarrow$ M1 = Cutoff $\Rightarrow C_{gc} + C_{gsov}$ (Note C_{gd} is shorted out!)

$= (20\mu)(1.8\mu)\frac{C_{ox}C_{jc}}{C_{ox}+C_{jc}} + 20\mu C_{ov} = 36\mu^2\frac{C_{ox}C_{jc}}{C_{ox}+C_{jc}} + 20\mu C_{ov}$

M2 = Sat. $\Rightarrow C_{gs} + C_{gd} = \frac{2}{3}(60\mu)(1.8\mu)C_{ox} + 60\mu C_{ov} + 60\mu C_{ov}$

$= 72\mu^2 C_{ox} + 120\mu C_{ov}$

Total C_G

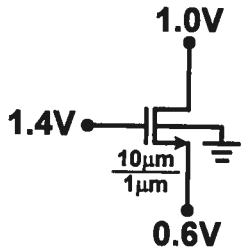
$36\mu^2\frac{C_{ox}C_{jc}}{C_{ox}+C_{jc}} + 72\mu^2 C_{ox} + 140\mu C_{ov}$

d. $C_{jx} \Rightarrow$ M1 = Cutoff

$C_{jx} = A_x C_j + P_x C_{jsw} = 6\mu(10\mu)C_j + (6\mu+10\mu)2C_{jsw}$

Problem 2 (40 points)

For the transistor below, assume V_{T0}=0.7V, γ=0.45V$^{1/2}$, and $2\Phi_F$=0.9V.



$$I_{DS} = I_o \exp\left(\frac{(V_{GS}-V_{Tn})q}{\zeta kT}\right)\left(1-\exp\left(-\frac{V_{DS}q}{kT}\right)\right) \quad \text{(Subthreshold)}$$

$$I_{DS} = \mu_n C_{OX}\frac{W}{L-2L_D}(V_{GS}-V_{Tn}-0.5V_{DS})V_{DS} \quad \text{(Triode)}$$

$$I_{DS} = \frac{1}{2}\mu_n C_{OX}\frac{W}{L-2L_D}(V_{GS}-V_{Tn})^2(1+\lambda V_{DS}) \quad \text{(Saturation)}$$

$$V_{Tn} = V_{T0}+\gamma\left(\sqrt{|2\Phi_F|+V_{SB}}-\sqrt{|2\Phi_F|}\right)$$

$V_{SB} = 0.6V$

a. Calculate V_T and state the transistor's operation region. (10 points)

$V_T = 0.7V + 0.45V^{1/2}\left(\sqrt{0.9V+0.6V}-\sqrt{0.9V}\right) = 0.824V$

$V_{GS} = 1.4V - 0.6V = 0.8V$

$V_{GS} < V_T \Rightarrow$ Subthreshold

$V_T = 0.824V$

Operation Region = Subthreshold

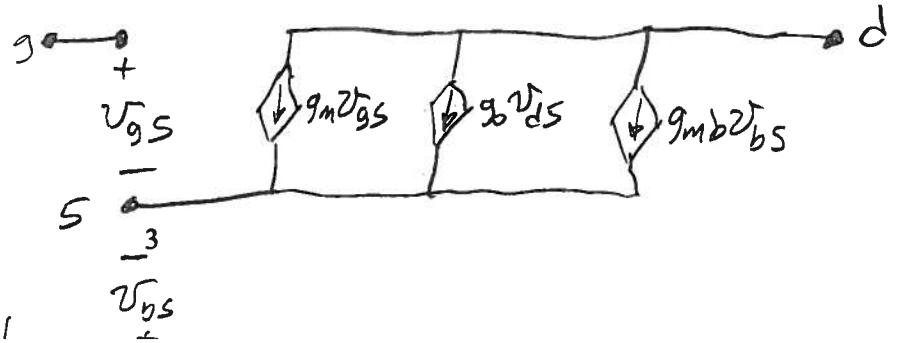
b. Using the appropriate I_{DS} equation above, **derive and sketch the small-signal model** of the transistor. **Include expressions for the g_m, g_o, and g_{mb}.** (30 points)

$$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_Q = \frac{I_o q}{\zeta kT}\exp\left(\frac{(V_{GS}-V_T)q}{\zeta kT}\right)\left(1-\exp\left(-\frac{V_{DS}q}{kT}\right)\right)$$

$$g_o = \left.\frac{\partial I_{DS}}{\partial V_{DS}}\right|_Q = \frac{I_o q}{kT}\exp\left(\frac{(V_{GS}-V_T)q}{\zeta kT}\right)\left(\exp\left(-\frac{V_{DS}q}{kT}\right)\right)$$

$$g_{mb} = \left.\frac{\partial I_{DS}}{\partial V_{BS}}\right|_Q = \frac{I_o q}{\zeta kT}(-1)\exp\left(\frac{(V_{GS}-V_T)q}{\zeta kT}\right)\left(1-\exp\left(-\frac{V_{DS}q}{kT}\right)\right)(-1)\left(\frac{\gamma}{2\sqrt{|2\Phi_F|+V_{SB}}}\right)$$

$$= \frac{\gamma g_m}{2\sqrt{|2\Phi_F|+V_{SB}}}$$



Problem 3 (20 points)
Sketch a layout that matches two capacitors of unit size 7.5 and 3.3. Assume that the unit capacitors are sized 10μm x 10μm. **Make sure to give the non-unit capacitor(s) dimensions.** In the sketch clearly label the critical dimensions and use at least 2 layout matching techniques. **Also, write specifically the 2 layout matching techniques that you are using.** Note, if you use a common-centroid layout technique, it doesn't have to have perfect center-of-mass matching, but it should be close.

Need to match $\frac{\text{Perimeter}}{\text{Area}}$ for all caps

"C1" For 7.5 cap ⇒ 6 unit caps + 1 non-unit cap
$W/A_{nu} = 1.5A_u$ ($K_1 = 1.5$)

"C2" For 3.3 cap ⇒ 2 unit caps + 1 non-unit cap
$W/A_{nu} = 1.3A_u$ ($K_2 = 1.3$)

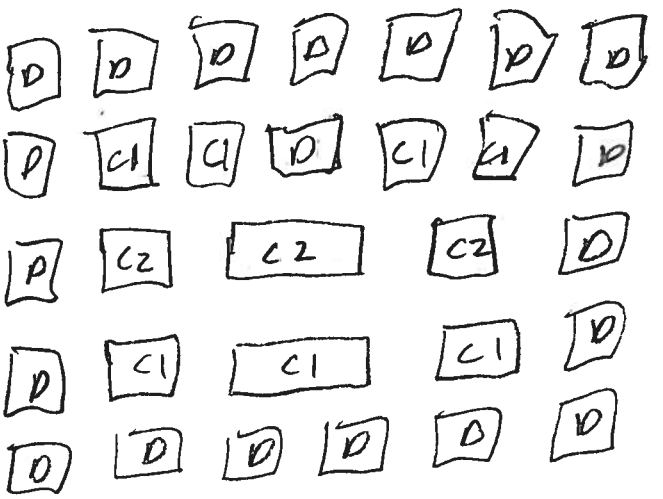
$$Y_{nu1} = X_u\left(K_1 - \sqrt{K_1^2 - K_1}\right)$$

C1: $= 10\mu\left(1.5 - \sqrt{1.5^2 - 1.5}\right) = 6.34\mu$

$$X_{nu1} = \frac{K_1 X_u^2}{Y_{nu1}} = \frac{1.5(10\mu)^2}{6.34\mu} = 23.7\mu$$

C2: $Y_{nu2} = 10\mu\left(1.3 - \sqrt{1.3^2 - 1.3}\right) = 6.76\mu$

$$X_{nu2} = \frac{1.3(10\mu)^2}{6.76\mu} = 19.2\mu$$



C_1 Non-Unit
$6.34 \times 23.7\mu$

C_2 Non-Unit
$6.76 \times 19.2\mu$

Layout Technique #1 = Dummies around entire perimeter
Layout Technique #2 = Common-Centroid (Approximately)