Texas A&M University
Department of Electrical and Computer Engineering

ECEN 474/704 – (Analog) VLSI Circuit Design

Spring 2018

Exam #1

Instructor: Sam Palermo

- Please write your name in the space provided below
- Please verify that there are **6** pages in your exam
- You may use one double-sided page of notes and equations for the exam
- Good Luck!

Problem	Score	Max Score
1		40
2		40
3		20
Total		**100**

Name:____

UIN:____

Problem 1 (40 points)

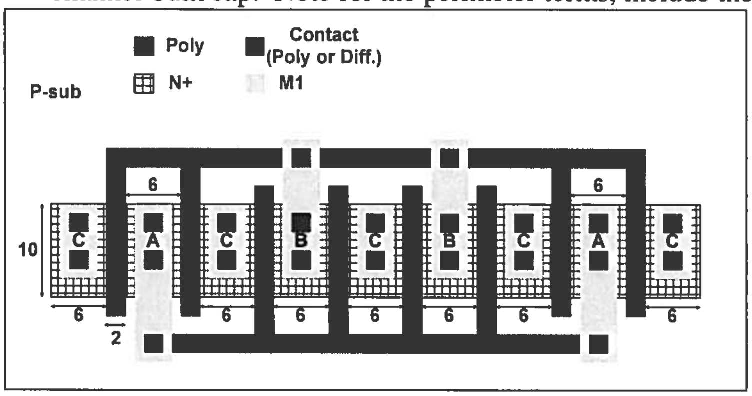
For the layout below, assume that all the commonly labeled diffusion areas are connected with the appropriate metal layers. Assume that V_A=2V, V_B=1.5V, V_C=1.0V, V_{T0}=0.7V, γ=0, and that all Spice parameters are given (i.e. C_j, C_{jsw}, C_{jc}, C_{ox}, C_{ov}). The dimensions are given in μm, with the poly gates having an L_D=0.1μm.

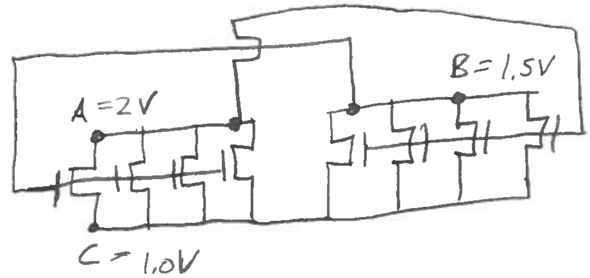
a) Draw the equivalent circuit. Combine all parallel transistors and given the total width and length of the equivalent transistors.

b) What region(s) are the transistors operating in?

c) **For node B only**, give an expression and calculate the total gate cap (only consider where B is the gate).

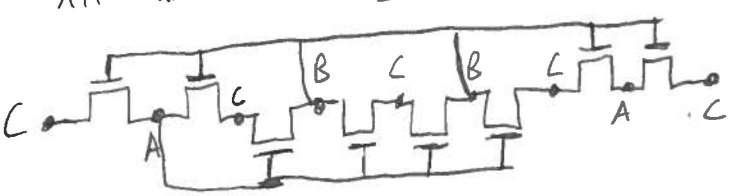
d) **For node A only**, give an expression and calculate the total junction cap, including the relevant channel-bulk cap. Note for the perimeter terms, include the sides underneath the gate.

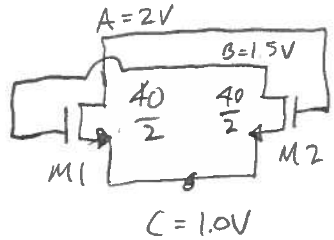




All transistors = 10/2

a.





b. $M_1 \Rightarrow V_{GS} = 1.5V - 1.0V = 0.5V < V_T \Rightarrow$ Cutoff or Subthreshold

$M_2 \Rightarrow V_{GS} = 2.0V - 1.0V = 1.0V > V_T$

$V_{DS} = 0.5V,\ V_{GS} - V_T = 0.3V \Rightarrow$ Saturation

c. $C_{gB} \Rightarrow M_1 =$ Cutoff

$= C_{gc} + C_{gsov} + C_{gdov}$

$= (40\mu)(1.8\mu)\dfrac{C_{ox}C_{jc}}{C_{ox}+C_{jc}} + 40\mu C_{ov} + 40\mu C_{ov}$

$$C_{gB} = 72\mu^2 \frac{C_{ox}C_{jc}}{C_{ox}+C_{jc}} + 80\mu C_{ov}$$

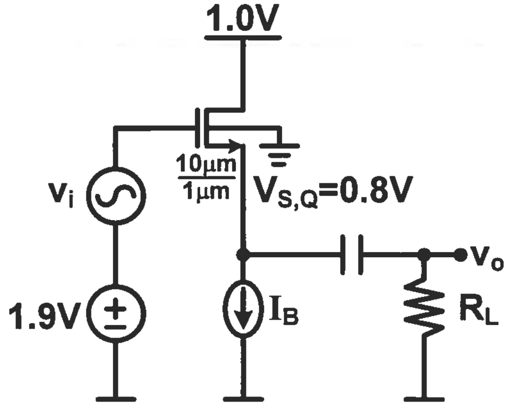
d. $C_{jA} \Rightarrow M1 =$ Cutoff

$C_{jA} = A_A C_j + P_A C_{jsw}$

$= (10\mu)(6\mu)(2)C_j + (10\mu + 6\mu)(2)(2)C_{jsw}$

$$C_{jA} = 120\mu^2 C_j + 64\mu C_{jsw}$$

Problem 2 (40 points)
For the circuit shown below, assume the transistor has V_{T0}=0.7V, γ=0.45$V^{1/2}$, and $2\Phi_F$=0.9V and its DC drain current is determined by the following equations.



$$I_{DS} = I_o \exp\left(\frac{(V_{GS}-V_{Tn})q}{\zeta kT}\right)\left(1-\exp\left(-\frac{V_{DS}q}{kT}\right)\right) \quad \text{(Subthreshold)}$$

$$I_{DS} = \mu_n C_{OX}\frac{W}{L-2L_D}(V_{GS}-V_{Tn}-0.5V_{DS})V_{DS} \quad \text{(Triode)}$$

$$I_{DS} = \frac{1}{2}\mu_n C_{OX}\frac{W}{L-2L_D}(V_{GS}-V_{Tn})^2(1+\lambda V_{DS}) \quad \text{(Saturation)}$$

$$V_{Tn} = V_{T0} + \gamma\left(\sqrt{|2\Phi_F|+V_{SB}} - \sqrt{|2\Phi_F|}\right)$$

a. Calculate V_T and state the transistor's operation region.

$V_T = 0.7V + 0.45V^{1/2}(\sqrt{0.9V + 0.8V} - \sqrt{0.9V}) = 0.860V$

$V_{DS} = 0.2V$, $V_{GS} - V_T = 1.1V - 0.86V = 0.24V$

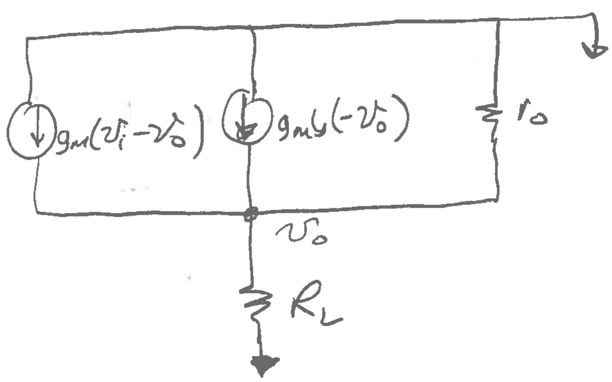
$V_{DS} < V_{GS} - V_T \Rightarrow$ Triode

V_T = 0.860 V

Operation Region = Triode

b. Using the appropriate I_{DS} equation above, **draw the low-frequency small-signal model of the circuit** (neglecting transistor capacitors), **include expressions for the g_m, g_o, and g_{mb}**, and **give an expression for the small-signal voltage gain of the circuit**, $A_v=v_o/v_i$, as a function of the relevant transistor conductances and the load resistor. Note, you can assume that the output AC–coupling capacitor acts as an ideal short.

SSM



$g_m = \left.\frac{\partial I_{DS}}{\partial V_{GS}}\right|_Q = \mu_n C_{ox}\frac{W}{L_{eff}}V_{DS}$

$g_o = \left.\frac{\partial I_{DS}}{\partial V_{DS}}\right|_Q = \mu_n C_{ox}\frac{W}{L_{eff}}(V_{GS} - V_T - V_{DS})$

$g_{mb} = \frac{\partial I_{DS}}{\partial V_{BS}} = \mu_n C_{ox}\frac{W}{L_{eff}}V_{DS}(-1)(-1)\frac{\gamma}{2\sqrt{|2\Phi_F| + V_{SB}}}$

$= \frac{\gamma g_m}{2\sqrt{|2\Phi_F| + V_{SB}}} = \eta g_m$

$v_o = [g_m(v_i - v_o) + g_{mb}(-v_o)](R_L \| r_o)$

$v_o[1 + (g_m + g_{mb})(R_L \| r_o)] = v_i g_m (R_L \| r_o)$

$$\frac{v_o}{v_i} = \frac{g_m (R_L \| r_o)}{1 + (g_m + g_{mb})(R_L \| r_o)}$$

c. In addition to the parameters given previously, assume that I_o=1nA, kT/q=25.9mV, ζ=1, μC_{ox}=130μA/V^2, L_D=0.1μm, and λ=0.1V^{-1}. Calculate the necessary load resistor value for $|A_V|$=0.7V/V.

$$A_V = \frac{g_m(R_L||r_o)}{1+(g_m+g_{mb})(R_L||r_o)} = \frac{g_m}{G_L+g_o+(1+\eta)g_m}$$

$$G_L = \frac{g_m}{A_V} - g_o - (1+\eta)g_m$$

$$g_m = (130\mu)\left(\frac{10}{0.8}\right)(0.2) = 325\ \mu A/V$$

$$g_o = (130\mu)\left(\frac{10}{0.8}\right)(1.1-0.86-0.2) = 65\ \mu A/V$$

$$\eta = \frac{0.45}{2\sqrt{0.9+0.8}} = 0.173$$

$$G_L = \frac{325\mu}{0.7} - 65\mu - 1.173(325\mu) = 18.1\ \mu A/V$$

$$R_L = \frac{1}{G_L} = 55.4k\Omega$$

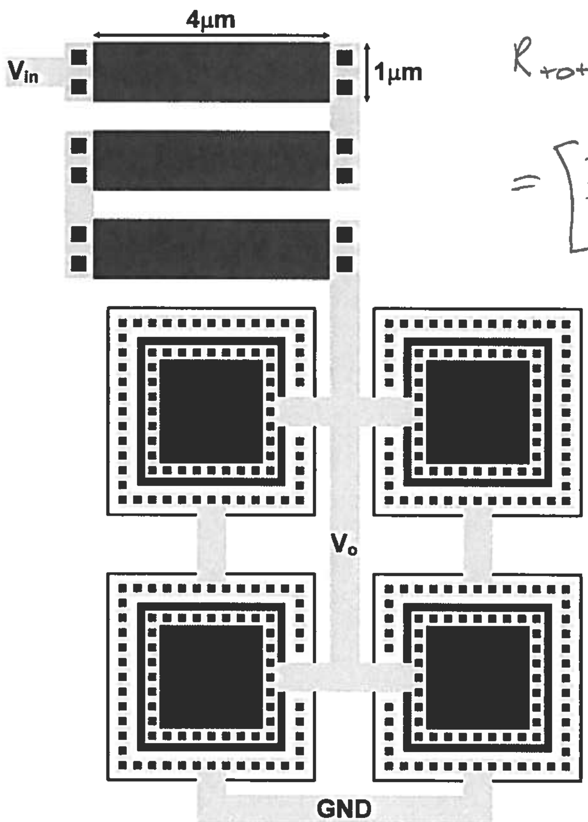
R_L for $|A_V|$=0.7V/V = 55.4kΩ

Problem 3 (20 points)

The layout of a simple RC-filter is shown below. For the 3-finger resistor, assume that $R_\square$=200Ω/□ and each contact has a resistance of 10Ω. The capacitor consists of 4 unit capacitors that each have top-plate dimensions of 10μm x 10μm. These unit capacitors have a capacitive density of 1fF/μm^2.

a. Sketch the equivalent circuit and give the values of the resistor and the capacitor. The resistor contacts should be considered in its resistance calculation, but the capacitor contacts' resistance can be ignored. Also neglect the impedance of all the metal interconnect between the elements.

b. Sketch the Bode plot (Magnitude only) and label any pole and/or zero frequencies.



Each unit capacitor has top-plate dimensions of 10μm x 10μm

n = # parallel contacts

F = # fingers

$$R_{total} = \left(\frac{2R_C}{n} + R_\square \frac{L}{W}\right)F$$

$$= \left[\frac{2(10)}{2} + 200\left(\frac{4}{1}\right)\right]3 = 2.43k\Omega$$

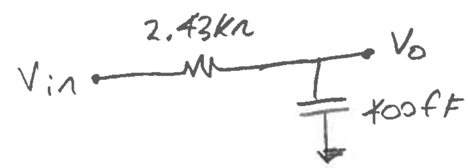
U = # unit caps

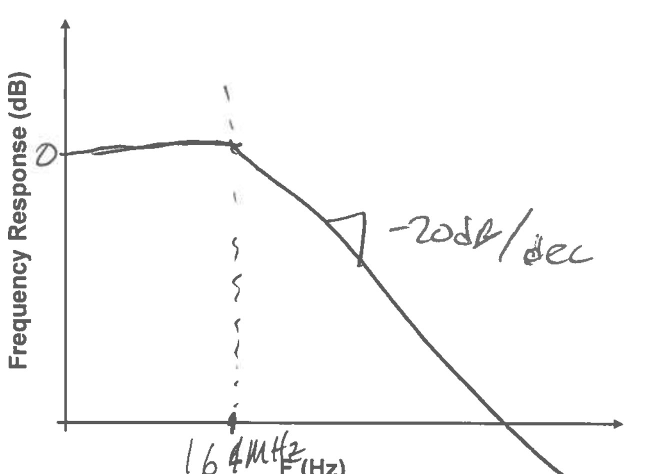
$$C_{total} = A_{top} C_{density} U$$

$$= (10\mu)(10\mu)\left(1\frac{fF}{\mu^2}\right)(4)$$

$$= 400fF$$

Schematic





$$\frac{V_o}{V_i} = \frac{1}{1+sRC}$$

$$= \frac{1}{1+s(9.72\times10^{-10})}$$

DC gain = 1 = 0dB

1 pole at −1.03 Grad/s = −164MH

Scratch Paper