ECEN 474/704 Lab 5: Frequency Response of Inverting Amplifiers

Objective

Design, simulate and layout various inverting amplifiers.

Introduction

Inverting amplifiers are fundamental building blocks of electronic circuits. These amplifiers are used in a variety of circuit applications such as the gain stage of operational amplifiers and the NOT gate in digital logic. Due to the utility of inverting amplifiers, learning the process of analyzing and designing these basic building blocks is important to successful circuit design.

Studying inverting amplifiers also gives us insight into basic circuit concepts such as small-signal frequency response and feedback. In this lab, the small-signal model of a generic inverting amplifier is analyzed while a generic design procedure is developed. Next, the lab manual presents advantages and disadvantages of several circuit structures. Finally, the students will design various inverting amplifiers by choosing a circuit structure and developing a design procedure.

The basic inverting amplifier is shown in Figure 7-1. The input signal V_{in} will contain an AC signal component as well as a DC component used to set the operating point:

$$V_{IN} = V_{BIAS} + v_{in}$$

Transistor M_1 is called the driver since the input signal controls the amplifier from this point. An ideal load will have infinite impedance. In the basic inverting amplifier circuit of Figure 7-1, the load is represented by an ideal current source.

The DC operating point of the circuit is determined by I_{BIAS} and V_{BIAS}. These currents and voltages determine the transistor's small-signal parameters and establish the quiescent output voltage.

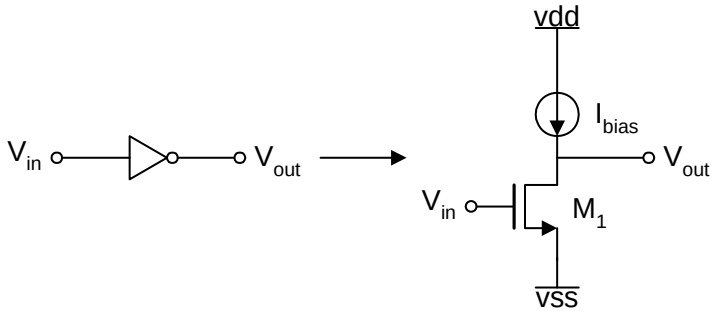

Figure 7-1: Basic Inverting Amplifier

The small-signal model for an inverting amplifier is given in Figure 7-2. The circuit consists of two connected nodes which will result in two poles and one zero. The resistance R_A represents the voltage source's resistance R_S and any resistance used to establish the DC biasing. The resistance R_B includes the load resistance and the small-signal output resistance of the driving transistor. The capacitance C_A includes source capacitance and the small-signal input capacitance of the transistor. Similarly, C_B represents the load capacitance and the small-signal input capacitance of the transistor. Finally, C_C consists of any external stray capacitance and internal capacitance between the drain and gate of the driving transistor.

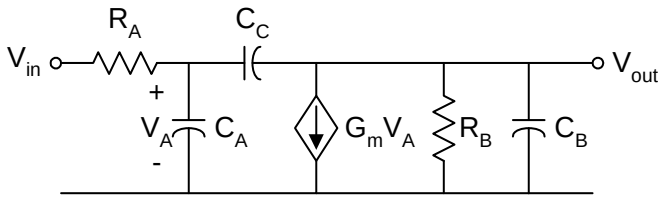

Figure 7-2: Generic Inverting Amplifier Small-Signal Model

Using node voltage equations or mesh currents, the input-output transfer function for the inverting amplifier can be obtained. The transfer function for the generic amplifier from Figure 7-2 is given by:

$$H(s) = \frac{\frac{C_C}{R_A}\left(s - \frac{G_m}{C_C}\right)}{\left((C_A + C_C)(C_B + C_C) - C_C^2\right)s^2 + \left(\frac{C_A + C_C}{R_B} + \frac{C_B + C_C}{R_A} + G_m C_C\right)s + \frac{1}{R_A R_B}} \tag{1}$$

This formula is too complicated to gain any useful insight as to how various resistors and capacitors affect the frequency response of the inverting amplifier. Various assumptions can be made to simplify (1). If we make the assumptions $C_B >> C_A$ and $C_C >> C_A$, then the transfer function can be simplified to:

$$H(s) = \frac{\frac{1}{R_A C_B}\left(s - \frac{G_m}{C_C}\right)}{s^2 + \left(\frac{1}{R_B C_B} + \frac{1}{R_A\left(\frac{C_B C_C}{C_B + C_C}\right)} + \frac{G_m}{C_B}\right)s + \frac{1}{R_A R_B C_B C_C}} \tag{2}$$

This simplification is useful because C_C is generally a large capacitor used to set the gain-bandwidth product, and the total load capacitance C_B is generally larger than any parasitic input capacitances.

Next, we can simplify (2) in two different meaningful ways. The first way assumes that R_A is small while the second assumes R_A is large. Using the first assumption that R_A is small, we have $R_A << R_B$ and $R_A << 1/G_m$. With this simplifying assumption, the transfer function in (2) becomes:

$$H(s) = \frac{\frac{1}{R_A C_B}\left(s - \frac{G_m}{C_C}\right)}{s^2 + \left(\frac{1}{R_A\left(\frac{C_B C_C}{C_B + C_C}\right)}\right)s + \frac{1}{R_A R_B C_B C_C}} \tag{3}$$

Also, if we assume the poles are far apart ($p_1 << p_2$), then we can use the following simplification when factoring:

$$D(s) = (s + p_1)(s + p_2) = s^2 + (p_1 + p_2)s + p_1 p_2 \approx s^2 + (p_2)s + p_1 p_2$$

The above simplification assumes a dominant pole exists. The dominant pole is the pole which is significantly closer to the origin than all the other poles. The non-dominant poles occur at a much greater frequency than the dominant pole. Using this simplification, the denominator in (3) can be factored as follows:

$$H(s) = \frac{\frac{1}{R_A C_B}\left(s - \frac{G_m}{C_C}\right)}{\left(s + \frac{1}{(C_B + C_C)R_B}\right)\left(s + \frac{1}{R_A\left(\frac{C_B C_C}{C_B + C_C}\right)}\right)} \tag{4}$$

Now that the transfer function is in factored form, we can find the DC gain, poles, and zero for the case when C_A is small and R_A is small:

$$A_{v0} = -G_m R_B$$

$$p_1 = \frac{-1}{(C_B + C_C)R_B}$$

$$p_2 = \frac{-1}{R_A\left(\frac{C_B C_C}{C_B + C_C}\right)}$$

$$z = \frac{G_m}{C_C}$$

Assuming R_A is large ($R_A \approx R_B$ and $R_A >> 1/G_m$), the transfer function given by (2) can be factored as:

$$H(s) = \frac{\frac{1}{R_A C_B}\left(s - \frac{G_m}{C_C}\right)}{\left(s + \frac{G_m}{C_B}\right)\left(s + \frac{1}{G_m R_A R_B C_C}\right)} \tag{5}$$

With this transfer function in factored form, we can find the DC gain, poles and zero for the case when C_A is small and R_A is large:

$$A_{v0} = -G_m R_B$$

$$p_1 = \frac{-1}{G_m R_A R_B C_C} = \frac{-1}{|A_{v0}| R_A C_C}$$

$$p_2 = \frac{-G_m}{C_B}$$

$$z = \frac{G_m}{C_C}$$

Notice that the dominant pole had been shifted towards the origin. This is an example of the Miller Effect.

Next the frequency response of the two transfer functions derived above will be examined. For the case when R_A is small, the poles are greatly separated. Usually this system can be represented adequately by a first-order transfer function. The pole-zero diagram is shown in Figure 7-3. Since this system is approximately first-order, any stability problems will be less likely, however, the right-half plane zero will reduce the phase margin. If stability becomes a problem, increase C_B relative to C_C.

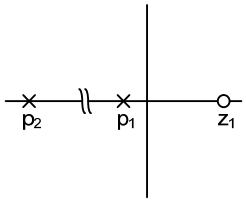

Figure 7-3: Pole-Zero Diagram for Small R_A

For the case when R_A is large, the system consists of a dominant pole, a non-dominant pole, and a right-half plane zero. Due to these factors reducing phase margin, careful circuit design is required to guarantee stability. The zero reduces the phase margin and should be placed as far to the right as possible, while the non-dominant pole should be placed as far to the left as possible. Figure 7-4 illustrates the pole-zero diagram for this system.

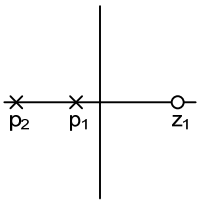

Figure 7-4: Pole-Zero Diagram for Large R_A

Two other simplifications are shown below. The first simplification assumes $C_A >> C_C$, and $R_A \geq R_B$. This situation may occur when the inverter is used to amplify a signal from a capacitive transducer:

$$A_{v0} = -G_m R_B$$

$$p_1 = \frac{-1}{R_A C_A}$$

$$p_2 = \frac{-1}{R_B(C_B + C_C)}$$

$$z = \frac{G_m}{C_C}$$

The second set of equations assumes $C_B >> C_C$, $C_B >> C_S$ and $R_B \geq R_A$. These equations are useful if a wideband inverter is driving a capacitive load:

$$A_{v0} = -G_m R_B$$

$$p_1 = \frac{-1}{R_B C_B}$$

$$p_2 = \frac{-1}{R_A(C_A + C_C)}$$

$$z = \frac{G_m}{C_C}$$

Design Description

This section of the lab will discuss in detail four inverting amplifier configurations. The first inverter uses a current mirror as an active load. The second is a basic inverter commonly used in CMOS digital logic. The last two amplifiers employ diode-connected transistors as loads. Each of these amplifiers have characteristics which makes their use advantageous in certain applications.

Inverter with Current Mirror Load:

The inverter of Figure 7-5 employs an NMOS driver and a PMOS current mirror as the load. The current mirror provides a large small-signal output resistance and constant biasing current. The biasing current establishes the operating point for the transistor M_1, which in turn determines its small-signal transconductance. This circuit can provide a high output resistance and a large small-signal gain.

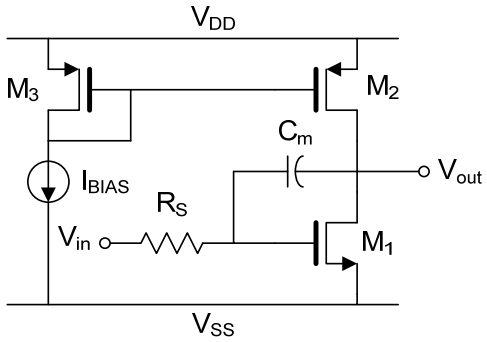

Figure 7-5: Inverting Amplifier with Current Mirror Load

A disadvantage of this circuit is the need for a biasing current which requires additional circuitry. However, since this circuit is biased by another circuit, this amplifier can be programmed or tuned to operate at a specific operating point even during the presence of process variations.

Design Procedure:

This design procedure is only an example. To achieve the desired inverter performance another procedure may need to be used.

1. Determine the Miller compensation capacitor C_m from the gain-bandwidth product (GBW) specification. Remember GBW = $A_{v0}p_1$, $A_{v0} = -G_mR_{out}$ and $p_1 = -1/(R_{out}C_m)$.

2. To guarantee stability be sure the phase margin is greater than 60º, make sure the non-dominant pole p_2 is at least three times greater than the GBW. Use this information along with the load capacitance to determine g_{m1}.

3. Determine I_{BIAS} to provide the desired DC gain.

4. Using g_{m1} and I_{BIAS}, determine the size for transistor M_1.

5. Use a 1:1 current mirror sized such that the transconductance is equal to that of the driver transistor.

Digital CMOS Inverter:

Figure 7-6 illustrates the digital CMOS inverter. This circuit is commonly used in digital logic circuits. Since both transistors are driven by the input source, the voltage gain will be higher with this circuit than the amplifier with a current mirror load.

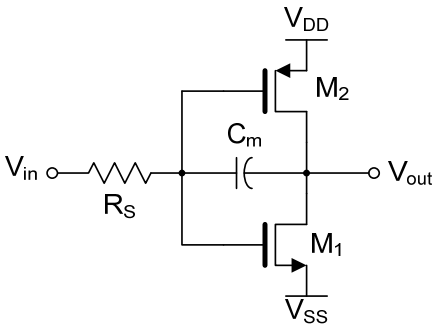

Figure 7-6: Digital CMOS Inverting Amplifier

An advantage of this circuit is that it does not need external biasing circuitry. The operating point of this circuit is determined by the ratio of the transistor sizes. Using large transistors will cause G_m to be high. This allows higher frequency operation when driving large capacitive loads.

Figure 7-7 illustrates the effect of changing the ratio of the transistors. Typically, the transition region will be half the supply voltage. In this case, the products of the transconductance and transistor sizes for the NMOS and PMOS must be equal. If process variations cause KP_P or KP_N to change, then the transition region will shift.

Figure 7-7 also shows the gain and linearity of the amplifier. The slope of the curve at any point is the gain. The vertical section of the graph is a region of high gain. Since the slope of the curve changes with signal amplitude, the amplifier exhibits high distortion. To obtain low distortion operation, the input voltage must remain small.

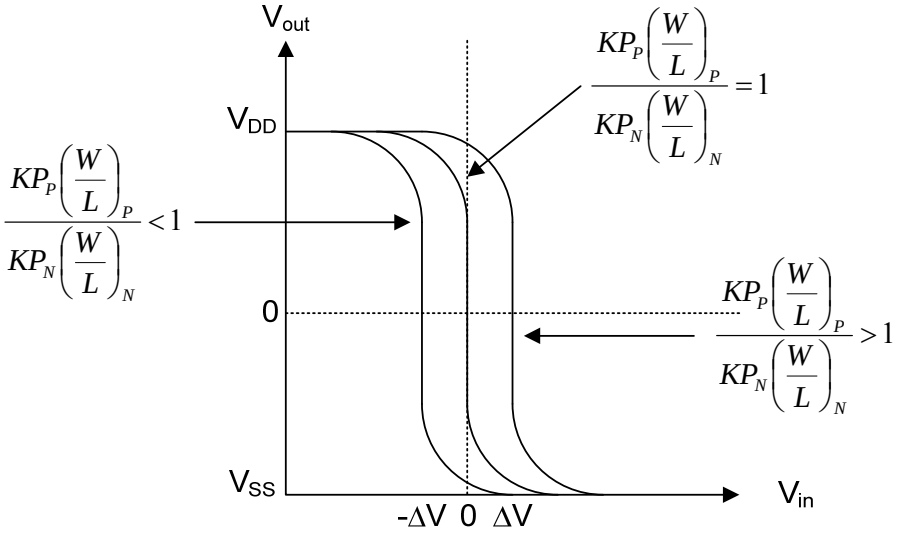

Figure 7-7: Transition Regions for Various Transistor Size Ratios

Design Procedure:

This design procedure is only an example. To achieve the desired performance another procedure may need to be used.

1. First, notice the DC gain is determined by the power supply voltage for symmetrical operation:

$$A_{v0} = G_m R_B = \frac{g_{m1}}{\lambda I_{BIAS}} = \frac{2}{\lambda(V_{GS} - V_T)} = \frac{2}{\lambda(V_{DD} - V_T)}$$

2. Determine the Miller compensation capacitor C_m from the gain-bandwidth product (GBW) specification or dominant pole specification. Remember GBW = $A_{v0}p_1$.

3. To guarantee stability, be sure the phase margin is greater than 60º. This requires the non-dominant pole p_2 to be at least three times higher in frequency than the gain-bandwidth product ($p_2 > 3$ GBW). Use this information to determine g_{m1}.

4. For symmetrical operation, the transistors must satisfy the ratio:

$$\frac{KP_N \left(\frac{W}{L}\right)_N}{KP_P \left(\frac{W}{L}\right)_P} = 1$$

5. Using the value for g_{m1} and the above equation, determine the size for transistors M_1 and M_2. Remember, the current through both transistors is the same.

$$KP_{N,P} \left(\frac{W}{L}\right)_{N,P} = \frac{g_{m1,2}}{(V_{DD} - V_T)}$$

PMOS Only Inverter with Self-Biased Load:

Figure 7-8 shows a PMOS inverter that does not require a CMOS process. Due to the diode-connected load, the inverter has a low output resistance which in turn gives it a low gain. This inverter however is very linear.

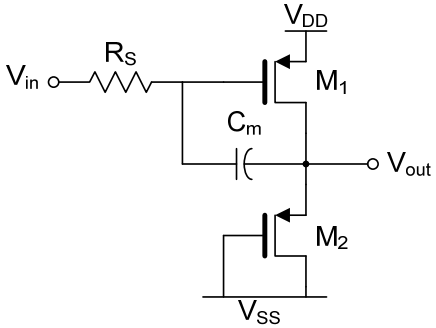

Figure 7-8: PMOS Only Inverter with Self-Biased Load

The derivation of the large-signal transfer function is easy. Assume both transistors have the same size and perfectly matched. Since the drain current is the same for both transistors:

$$I = I_{D1} = I_{D2} = \frac{1}{2} KP_P \left(\frac{W}{L}\right)_1 (V_{SG1} - |V_T|)^2$$

M_2 is diode connected, so V_{out} is given by:

$$V_{out} = V_{SS} + V_{SG2} = V_{SS} + |V_T| + \sqrt{\frac{2I}{KP_P \left(\frac{W}{L}\right)_2}} = V_{SS} + |V_T| + \sqrt{\frac{KP_P \left(\frac{W}{L}\right)_1 (V_{SG1} - |V_T|)^2}{KP_P \left(\frac{W}{L}\right)_2}}$$

$$V_{out} = V_{SS} + |V_T| + V_{SG1} - |V_T| = V_{SS} + V_{DD} - V_{in} = -V_{in}$$

Design Procedure:

This design procedure is only an example. To achieve the desired inverter performance another procedure may need to be used.

1. First, notice the DC gain is determined by the sizes of the transistors. For a unity-gain buffer, the gain is one.

$$A_{v0} = G_m R_B = \frac{g_{m1}}{g_{m2}}$$

2. Determine the Miller compensation capacitor C_m from the dominant pole location of the GBW specification

3. To guarantee stability, be sure the phase margin is greater than 60º. This requires the non-dominant pole p_2 to be at least three times higher in frequency than the GBW. Use this information to determine g_{m1} and g_{m2}.

4. Using the value for the transistor transconductance, determine the size for the transistors M_1 and M_2. Remember, the current through both transistors is the same.

CMOS Inverter with Self-Biased Load:

The inverter of Figure 7-9 is similar to the previous inverter except it requires a CMOS process. Matching of transistors is also difficult. Use a design procedure similar to the previous inverter.

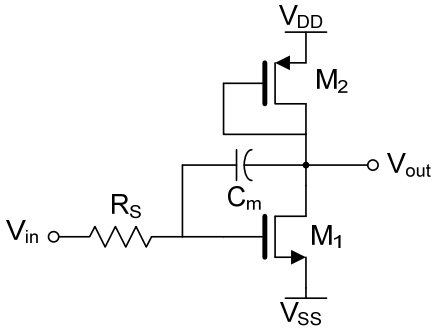

Figure 7-9: CMOS Inverter with Self-Biased Load

Summary of AC Characteristics

Table 7-1 lists the capacitors and resistors from Figure 7-2 and gives the parameter value for each of the four configurations. This table does not include all possible parasitic capacitance associated with the transistors. The table also does not include stray capacitances associated with circuit layout, which might be a significant component of the frequency response.

Table 7-1: Relationship between the Generic Amplifier Model and the Inverter Circuits

	Current-Mirror Load	Digital CMOS	Self-Biased PMOS	Self Biased CMOS
R_A	R_S	R_S	R_S	R_S
R_B	$r_{o1}\|\|r_{o2}\|\|R_L$	$r_{o1}\|\|r_{o2}\|\|R_L$	$r_{o1}\|\|1/g_{m2}\|\|R_L$	$r_{o1}\|\|1/g_{m2}\|\|R_L$
C_A	C_{gs1}	$C_{gs1}+ C_{gs2}$	C_{gs1}	C_{gs1}
C_B	$(C_{bd1}\|\|C_{bs1})+$ $(C_{bd2}\|\|C_{bs2})+$ C_L	$(C_{bd1}\|\|C_{bs1})+$ $(C_{bd2}\|\|C_{bs2})+$ C_L	$(C_{bd1}\|\|C_{bs1})+$ $(C_{bd2}\|\|C_{bs2})+$ $C_L+ C_{gs2}$	$(C_{bd1}\|\|C_{bs1})+$ $(C_{bd2}\|\|C_{bs2})+$ $C_L+ C_{gs2}$
C_C	$C_{gd1}+C_m$	$C_{gd1}+C_{gd2}+C_m$	$C_{gd1}+C_m$	$C_{gd1}+C_m$
G_m	g_{m1}	$g_{m1}+g_{m2}$	g_{m1}	g_{m1}

Prelab

The prelab exercises are due at the beginning of the lab period. No late work is accepted.

1. Create a table ranking the various amplifiers as good, medium or poor in the following categories: gain, input impedance, output impedance and linearity. Include the expressions for each design specification (except for linearity).

2. Derive the transfer function for the generic amplifier by applying Miller's theorem. Compare this transfer function to the one derived in the lab manual. Comment on the utility of Miller's theorem. (Hint: Simplify all input capacitances as C_{in} and output capacitances as C_{out}. C_{in} and C_{out} will contain the terms $C_C(1+A_0)$ and $C_C(1+1/A_0)$, respectively).

3. Design the following inverting amplifiers with the following specifications:

   a) Current mirror load inverter
   GBW = 1 MHz, PM = 60º, A_{v0} = 30 dB, $V_{DD} = -V_{SS}$ = 0.9 V, R_S = 100 kΩ, C_L = 30 pF

   b) Digital CMOS inverter
   GBW = 1 MHz, PM = 60º, A_{v0} = 30 dB, $V_{DD} = -V_{SS}$ = 0.9 V, R_S = 100 kΩ, C_L = 30 pF

   c) Self-biased PMOS only inverter
   GBW = 1 MHz, PM = 60º, A_{v0} = 0 dB, $V_{DD} = -V_{SS}$ = 0.9 V, R_S = 100 kΩ, C_L = 30 pF

   d) Self-biased CMOS inverter
   GBW = 1 MHz, PM = 60º, A_{v0} = 0 dB, $V_{DD} = -V_{SS}$ = 0.9 V, R_S = 100 kΩ, C_L = 30 pF

Lab Report

1. Simulate the designs from the prelab. Simulate and perform design iterations until your circuit operates within the given specifications. These simulation results will be included in the final lab report.

    a) Run a DC sweep of each of the inverter circuits from -0.9 V to 0.9 V and use markers to mark the zero crossing voltage for the X-axis and Y-axis (points where X = 0 and Y = 0, also remember the "m" hotkey is used for marker), and comment on the linear region. Determine input offset and add a bias source to the circuit to insure $V_{out} = V_{in} = 0$.

    b) Create frequency response plots and set markers for GBW, PM, p_1 and A_{v0}.

2. Layout your final designs and include the LVS reports (again NetID and time stamp required for credit).

3. Repeat simulations from part 1 on the layout. Be sure parasitic capacitances from the layout are included.