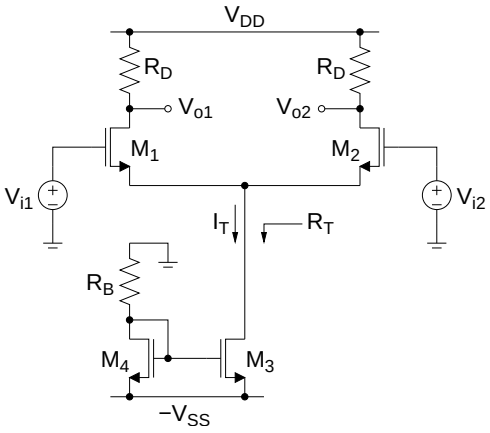
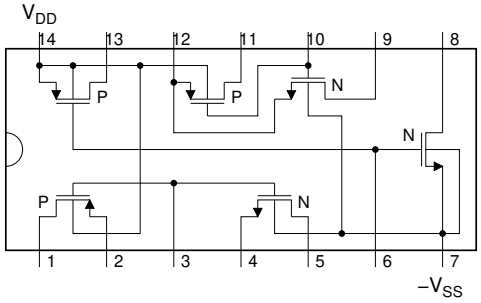
ECEN 326 Lab 5
Design of a MOS Differential Amplifier

Circuit Topology

The following figure shows a typical MOS differential amplifier, as well as MOS device parameters.



CD4007N	CD4007P
$k_n' = 70\ \mu A/V^2$	$k_p' = 15\ \mu A/V^2$
$V_{tn} = 1.4\ V$	$V_{tp} = -1.65\ V$
$W = 170\ \mu m$	$W = 360\ \mu m$
$L = 10\ \mu m$	$L = 10\ \mu m$
$\lambda_n = 0.016\ V^{-1}$	$\lambda_p = 0.01\ V^{-1}$



The tail current source (I_T) can be calculated from

$$V_{SS} = I_{D4}R_B + V_{GS4}$$
$$I_{D4} = \frac{k_n'}{2}\frac{W}{L}(V_{GS4} - V_{tn})^2$$
$$I_T = I_{D3} = I_{D4}$$

DC drain currents of M_1 and M_2 are

$$I_{D1} = I_{D2} = \frac{I_T}{2}$$

Assuming $r_{o1}, r_{o2} \gg R_D$, small-signal differential-mode gain can be obtained as

$$A_{dm} = \frac{v_{od}}{v_{id}} \approx -\frac{R_D}{\frac{1}{g_{m1}}} = -g_{m1}R_D$$

where $g_{m1} = \sqrt{2k_n'\frac{W}{L}I_{D1}}$. Common-mode gain can be found as

$$A_{cm} = \frac{v_{oc}}{v_{ic}} \approx -\frac{R_D}{\frac{1}{g_{m1}} + 2R_T}$$

where $R_T = r_{o3} = \frac{1}{\lambda_n I_{D3}}$. Common-mode rejection ratio (CMRR) can be calculated from

$$\text{CMRR} = 20\log\left|\frac{A_{dm}}{A_{cm}}\right|$$

Calculations and Simulations

Design a MOS differential amplifier with the following specifications:

$V_{ic} = 0\ V$ $\quad I_{supply} \leq 0.5\ mA$ $\quad$ THD $\leq 5\%$ for $V_{od} = 5\ V$ 0-to-peak @ 1 kHz
$V_{DD} = V_{SS} = 5\ V$ $\quad |A_{dm}| \geq 10$

1. Show all your calculations, design procedure, and final component values.
2. Simulate your circuit using CD4007N transistors. Submit all necessary simulation plots showing that the specifications are satisfied. Also provide the circuit schematic with DC bias points annotated.
3. Using a circuit simulator, perform Fourier analysis and show that the total harmonic distortion (THD) is less than 5% when the differential output voltage (V_{od}) is 5 V zero-to-peak at 1 kHz. Provide the simulation results.

Measurements

1. Construct the amplifier you designed.
2. Connect V_{i1} and V_{i2} to ground and record all DC quiescent voltages and currents. If any DC bias value (especially I_D) is **significantly** different than the one obtained from simulations, modify your circuit to get the desired DC bias before you move onto the next step.
3. Measure I_{supply} and the output offset voltage $V_{o1} - V_{o2}$.
4. Apply differential input signals at 1 kHz to the amplifier, measure A_{dm}.
5. Adjust the input signal level so that the differential output voltage is 5 V zero-to-peak. Measure the THD at the differential output.
6. Apply common input signals to the amplifier, measure A_{cm} and calculate CMRR.

Report

1. Include calculations, schematics, simulation plots, and measurement plots.
2. Prepare a table showing calculated, simulated and measured results.
3. Compare the results and comment on the differences.

Demonstration

1. Construct the amplifier you designed on your breadboard and bring it to your lab session.
2. Your name and UIN must be written on the side of your breadboard.
3. Submit your report to your TA at the beginning of your lab session.
4. Apply differential input signals at 1 kHz to the amplifier, measure A_{dm}.
5. Adjust the input signal level so that the differential output voltage is 5 V zero-to-peak. Measure the THD at the differential output.
6. Apply common input signals to the amplifier, measure A_{cm} and calculate CMRR.