ECEN 326 LAB 10
Design of a BJT Shunt-Series Feedback Amplifier

1 Circuit Topology

Circuit schematic of the feedback amplifier to be designed in this lab is shown in Fig. 1.

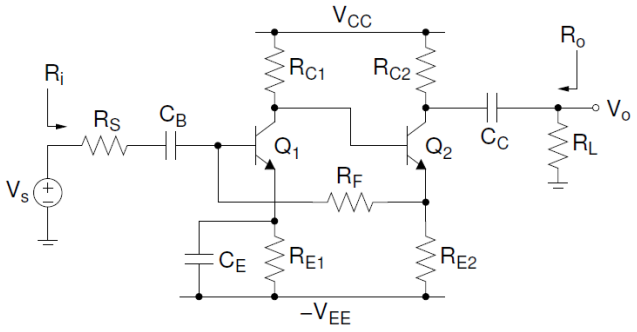


Figure 1: Feedback amplifier.

1.1 DC Biasing

First, the emitter DC bias voltage of Q_1 (V_{E1}) needs to be determined. Since only I_{B1} flows through the resistor R_F, the DC voltage drop on R_F can be assumed to be negligible. Thus, V_{E2} and V_{C1} can be expressed as

$$V_{E2} \approx V_{E1} + 0.7 \tag{1}$$

$$V_{C1} \approx V_{E1} + 1.4 \tag{2}$$

To maximize the voltage swing at the output, load-line analysis is needed for the second stage. The DC equation including I_{C2} and V_{CE2} can be written as

$$V_{CC} \approx R_{C2} I_{C2} + V_{CE2} + V_{E2} \tag{3}$$

Figure 2 shows the AC load line to obtain the maximum output swing.

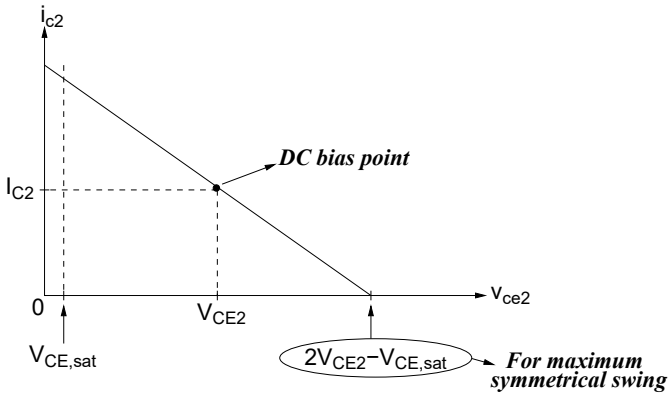


Figure 2: AC load line.

From the AC equivalent of Fig. 1, slope of the AC load line can be determined as

$$\frac{\Delta i_{c2}}{\Delta v_{ce2}} = -\frac{1}{(R_{C2} \parallel R_L) + R_{E2}} \tag{4}$$

Using the slope and the DC bias point $(i_{c2}, v_{ce2}) = (I_{C2}, V_{CE2})$, the load line equation can be obtained as

$$\frac{i_{c2} - I_{C2}}{v_{ce2} - V_{CE2}} = -\frac{1}{(R_{C2} \parallel R_L) + R_{E2}} \tag{5}$$

Evaluating Eq. (5) at the point $(i_{c2}, v_{ce2}) = (0, 2V_{CE2} - V_{CE,sat})$,

$$I_{C2}((R_{C2} \parallel R_L) + R_{E2}) = V_{CE2} - V_{CE,sat} \tag{6}$$

Solving Eqs. (3) and (6), the optimum I_{C2} to obtain the maximum symmetrical swing can be found as

$$I_{C2} = \frac{V_{CC} - 2V_{E2} - V_{CE,sat}}{R_{C2} + (R_{C2} \parallel R_L)} \tag{7}$$

After determining I_{C2}, 0-to-peak voltage swing at the output can be calculated as

$$V_{sw} = I_{C2}(R_{C2} \parallel R_L) = \frac{V_{CC} - 2V_{E2} - V_{CE,sat}}{1 + \dfrac{R_{C2}}{R_{C2} \parallel R_L}} = \frac{V_{CC} - 2V_{E2} - V_{CE,sat}}{2 + \dfrac{R_{C2}}{R_L}} \tag{8}$$

Since V_{E1} and V_{C1} are already determined, I_{C1} can be chosen based on other specifications. The remaining components can be calculated as

$$R_{E1} = \frac{V_{E1}}{I_{C1}} \tag{9}$$

$$R_{C1} = \frac{V_{CC} - V_{C1}}{I_{C1}} \tag{10}$$

$$R_{E2} = \frac{V_{E2}}{I_{C2}} \tag{11}$$

1.2 Feedback Analysis and Mid-band Frequency Response

AC equivalent of the amplifier in the mid-band frequency range is shown in Fig. 3.

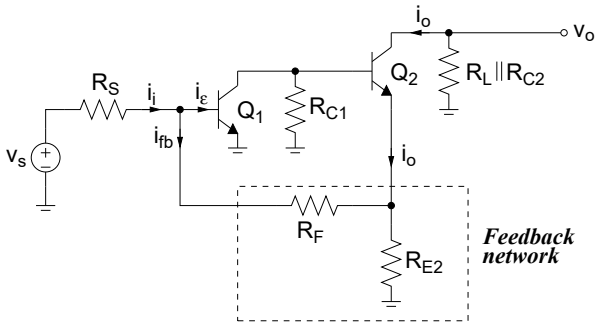


Figure 3: AC equivalent circuit.

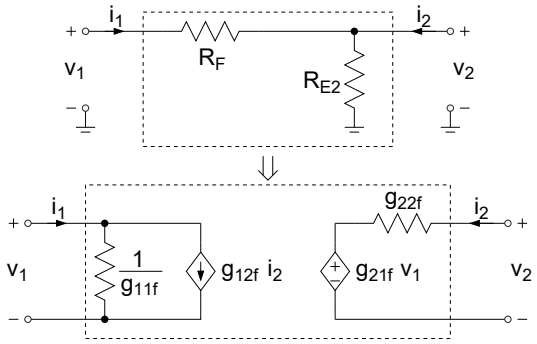
The input port of the feedback network in Fig. 3 is not directly connected to the output node (v_o). Therefore, the sampled output signal is not a voltage. Defining the output current as

$$i_o = -\frac{v_o}{R_L \parallel R_{C2}} \tag{12}$$

it can be concluded that i_o is sampled by the feedback network. At the amplifier's input, subtraction of the feedback signal is performed in the current domain,

$$i_i - i_{fb} = i_\varepsilon \tag{13}$$

Therefore, the type of feedback is shunt-series. The next step is to obtain the g parameters of the feedback network as shown in Fig. 4.



$$g_{11f} = \left.\frac{i_1}{v_1}\right|_{i_2=0} = \frac{1}{R_F + R_{E2}}$$

$$g_{22f} = \left.\frac{v_2}{i_2}\right|_{v_1=0} = R_{E2} \parallel R_F$$

$$g_{12f} = \left.\frac{i_1}{i_2}\right|_{v_1=0} = -\frac{R_{E2}}{R_{E2} + R_F}$$

Figure 4: Calculation of the g-parameters of the feedback network.

Replacing the feedback network with its two-port equivalent and converting the input source into current, the amplifier circuit can be arranged as in Fig. 5.

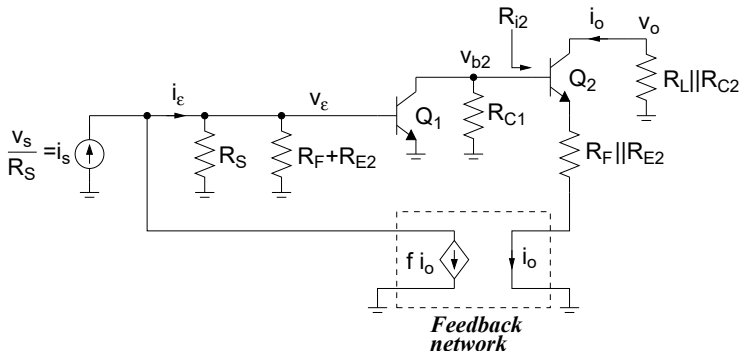


Figure 5: Amplifier with the ideal feedback network.

From Fig. 5, assuming r_{o1} and r_{o2} are large, the parameters a and f can be obtained as follows

$$v_\varepsilon = i_\varepsilon(R_S \parallel (R_F + R_{E2}) \parallel r_{\pi 1}) \tag{14}$$

$$\frac{v_{b2}}{v_\varepsilon} = -\frac{R_{C1} \parallel R_{i2}}{r_{e1}} \tag{15}$$

$$R_{i2} = (\beta + 1)(r_{e2} + (R_F \parallel R_{E2})) \tag{16}$$

$$\frac{v_o}{v_{b2}} = -\frac{R_L \parallel R_{C2}}{r_{e2} + (R_F \parallel R_{E2})} \tag{17}$$

$$v_o = -i_o(R_L \parallel R_{C2}) \tag{18}$$

$$a = \frac{i_o}{i_\varepsilon} = -\frac{(R_S \parallel (R_F + R_{E2}) \parallel r_{\pi 1})(R_{C1} \parallel R_{i2})}{r_{e1}(r_{e2} + (R_F \parallel R_{E2}))} \tag{19}$$

$$f = g_{12f} = -\frac{R_{E2}}{R_{E2} + R_F} \tag{20}$$

The current-mode close-loop amplifier parameters are

$$A_i = \frac{i_o}{i_s} = \frac{a}{1 + af} \tag{21}$$

$$Z_i = \frac{z_i}{1 + af} \tag{22}$$

$$Z_o = (1 + af)z_o \tag{23}$$

where

$$z_i = R_S \parallel (R_F + R_{E2}) \parallel r_{\pi 1} \tag{24}$$

$$z_o = R_T + r_{o2} + g_{m2} \frac{r_{\pi 2}}{r_{\pi 2} + (r_{o1} \parallel R_{C1})} r_{o2} R_T \tag{25}$$

$$R_T = R_F \parallel R_{E2} \parallel [r_{\pi 2} + (r_{o1} \parallel R_{C1})] \tag{26}$$

Figure 6 shows the current-mode equivalent model of the amplifier.

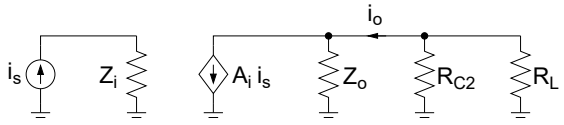


Figure 6: Current-mode equivalent model of the amplifier.

As the final step, the current-mode model needs to be converted to a voltage-mode amplifier. Figure 7 shows the equivalent amplifier where R_S is separated from Z_i and the controlled source depends on i_{in}.

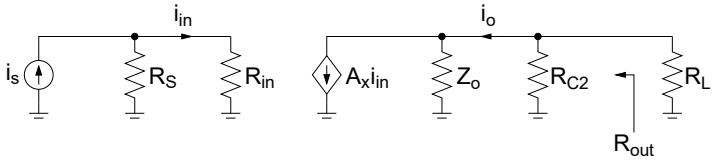


Figure 7: Current-mode amplifier with R_S separated.

R_{in} and A_x in Fig. 7 can be found as follows

$$Z_i = R_S \parallel R_{in} = \frac{1}{\dfrac{1}{R_S} + \dfrac{1}{R_{in}}} \;\Rightarrow\; R_{in} = \frac{1}{\dfrac{1}{Z_i} - \dfrac{1}{R_S}} \tag{27}$$

$$i_{in} = \frac{R_S}{R_S + R_{in}} i_s \;\Rightarrow\; A_x = A_i \left(1 + \frac{R_{in}}{R_S}\right) \tag{28}$$

Voltage-mode equivalent model of the amplifier can be obtained after final conversion as shown in Fig. 8.

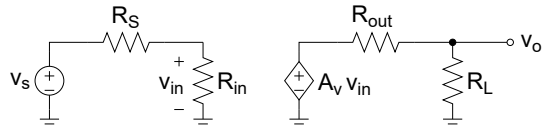


Figure 8: Voltage-mode equivalent model of the amplifier.

R_{out} and A_v in Fig. 8 can be found as follows

$$R_{out} = Z_o \parallel R_{C2} \approx R_{C2} \tag{29}$$

$$A_v = -A_x \frac{R_{out}}{R_{in}} = -A_i \left(1 + \frac{R_{in}}{R_S}\right) \frac{R_{out}}{R_{in}} \tag{30}$$

Finally, the voltage gain v_o/v_s can be calculated as

$$\frac{v_o}{v_s} = \frac{R_{in}}{R_S + R_{in}} A_v \frac{R_L}{R_{out} + R_L} \tag{31}$$

2 Calculations and Simulations

Using Q2N3904 transistors, design the feedback amplifier with the following specifications:

$V_{CC} = V_{EE} = 5\ V$ $\quad R_S = 50\Omega$ $\quad R_L = 10\ k\Omega$ $\quad V_{RE1} \geq 0.4\ V$
$af \geq 5$ $\quad I_{supply} \leq 10mA$ $\quad |v_o/v_s| \geq 80$ $\quad$ 0-to-peak unclipped output swing $\geq$ 3.5 V

1. Show all your calculations, design procedure, and final component values.
2. Using a circuit simulator, find a, f, I_{supply}, R_{in}, R_{out} and v_o/v_s to verify your results. Submit all necessary simulation plots showing that the specifications are satisfied. Also provide the circuit schematic with DC bias points annotated.
3. Using a circuit simulator, perform Fourier analysis to determine the THD of 3.5 V (0-to-peak) output waveform at 1 kHz. Submit transient and Fourier plots, and the distortion data.

3 Measurements

1. Construct the amplifier you designed.
2. Measure I_C, V_C, V_B and V_E for both transistors. If any DC bias value is significantly different than the one obtained from simulations, modify your circuit to get the desired DC bias before you move onto the next step.
3. Measure I_{supply}.
4. At midband frequencies, measure v_o/v_s, R_{in} and R_{out}.
5. Measure the maximum un-clipped output signal amplitude.
6. Measure the THD when the output is 3.5 V (0-to-peak) sinewave at 1 kHz.

Report

1. Include calculations, schematics, simulation plots, and measurement plots.
2. Prepare a table showing calculated, simulated and measured results.
3. Compare the results and comment on the differences.

Demonstration

1. Construct the amplifier you designed on your breadboard and bring it to your lab session.
2. Your name and UIN must be written on the side of your breadboard.
3. Submit your report to your TA at the beginning of your lab session.
4. Measure I_{supply}.
5. At midband frequencies, measure v_o/v_s, R_i and R_o.
6. Measure the THD when the output is 3.5 V (0-to-peak) sinewave at 1 kHz.