ECEN326: Electronic Circuits
Spring 2022

Lab 1 Graphical Design Approach

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Common Emitter Amp w/ Emitter Resistor

\[ A_v = -\frac{\alpha(R_C\|R_L)}{r_e + R_E\|R_G} = -\frac{g_m(R_C\|R_L)}{1 + g_m(R_E\|R_G)} \]

\[ R_{in} = kR_B\|(1 - k)R_B\left[(\beta + 1)(r_e + R_E\|R_G)\right] \]
Typical Design Specifications

- Loaded voltage gain, $A_v$
- Max output swing, $v_{omax}$
  - This must be satisfied at a given linearity (total harmonic distortion)
- Input resistance, $R_{in}$
- Power Supply, $V_{CC}$
- Min Emitter Voltage for $\beta$ robustness, $V_E$
How to set DC Biasing Conditions?

• In order to meet all design specifications, the DC biasing conditions ($I_C$, $R_C$) must be set appropriately.

• Can transform design specifications into functions of $I_C$ & $R_C$ and graph them to find acceptable solution space.
Rin, V_{CC}, & Neg. v_{omax} Specifications

- **R_{in} Spec**

\[
R_{in} = k R_B \|(1 - k) R_B \| [(\beta + 1)(r_e + R_E \| R_G)] \approx \beta (R_E \| R_G)
\]

\[
R_E \| R_G \approx \frac{R_{in}}{\beta}
\]

- Input resistance is primarily set by \( R_E \| R_G \)
Rin, VCC, & Neg. v_{omax} Specifications

- Need a minimum V_{CE} to keep transistor in active mode with maximum negative swing

  Set \( V_{CE\min} = 300mV \)

  * Note if the specs are relaxed enough, it is often good to set \( V_{CE\min} = 500mV \) for margin.

- V_{CC} Spec (w/ max negative swing)

\[
V_{CC} = V_E + V_{CE\min} + v_{omax} + I_C R_C \\
V_{CE\min} = V_{CC} - I_C R_C - v_{omax} - V_E \geq 300mV
\]
R_in, V_{CC}, & Neg. v_{omax} Specifications

- Can solve for I_C

\[ I_C \leq \frac{V_{CC} - v_{omax} - 0.3V - V_E}{R_C} \]

- Minimum negative AC Swing constraint sets an upper bound on I_C
Pos. $v_{o\text{max}}$ Specification

- Need to insure with a positive swing that the output signal doesn’t clip the power supply

\[ V_{CC} - I_C R_C + v_{o\text{max}} \leq V_{CC} \]

\[ I_C \geq \frac{v_{o\text{max}}}{R_C} \]

- Positive AC Swing constraint sets a lower bound on $I_C$

- Additional linearity constraint (harmonic distortion) generally sets a tighter bound
Gain Specification

\[
|A_v| = \left| \frac{v_o}{v_i} \right| \leq \frac{g_m \left( R_C \parallel R_L \right)}{1 + \frac{g_m \left( R_E \parallel R_G \right)}{\alpha}} = \frac{I_C}{V_{th}} \left( R_C \parallel R_L \right) \leq \frac{1}{1 + \frac{\left( \frac{I_C}{V_{th}} \right) \left( R_E \parallel R_G \right)}{\alpha}}
\]

\[
I_C \geq \frac{|A_v| V_{th}}{R_C || R_L - \frac{|A_v| \left( R_E || R_G \right)}{\alpha}} = \frac{|A_v| V_{th}}{R_C || R_L - \frac{|A_v| R_{in}}{\alpha \beta}}
\]

- Gain constraint sets a lower bound on $I_C$
Harmonic Distortion Specification

- Need a minimum amount of bias current to insure that the AC swing doesn’t distort

\[ i_c = a \cdot v_{be} = a_1 v_{be} + a_2 v_{be}^2 + a_3 v_{be}^3 + \ldots \]

where \( a_1 = g_m, \quad a_2 = \frac{1}{2} \frac{I_{CQ}}{V_{th}^2}, \quad \ldots \)

Here \( v_{be} = v_b - v_e \approx v_b - f \cdot i_c \)

where \( f = R_E \)

*This analysis is for a general CE Amp, in our specific circuit \( R_C \parallel R_C \parallel R_L \) and \( R_E \parallel R_E \parallel R_G \)
Harmonic Distortion Specification

We want to express $i_c$ as a function of $v_b$ because that is our input:

$$i_c = b_1 v_b + b_2 v_b^2 + b_3 v_b^3 + ...$$

Can show that:

$$b_1 = \frac{g_m}{1 + g_m R_E}, \quad b_2 = \frac{I_{CO}}{2 v_{th}^2 (1 + g_m R_E)^3}, \quad ...$$

- For single-ended amplifiers with low-distortion, HD2 will dominate the distortion terms.

The second-order harmonic distortion is:

$$HD2 = \frac{1}{2} \frac{b_2}{b_1^2} i_{c\text{max}} = \frac{1}{4} \left( \frac{1}{1 + g_m R_E} \right) \left( \frac{i_{c\text{max}}}{I_{CO}} \right)$$

*This analysis is for a general CE Amp, in our specific circuit $R_C \Rightarrow R_C || R_L$ and $R_E \Rightarrow R_E || R_G$*
Harmonic Distortion Specification

To satisfy a given HD2 specification

\[ i_{c_{\text{max}}} \leq 4HD2(1 + g_m R_E) I_{CQ} \]

\[ I_C \geq \frac{v_{o_{\text{max}}}}{R_C} \approx \frac{v_{o_{\text{max}}}}{4HD2(I_C/V_{th}) R_E} \]

\[ I_C \geq \frac{1}{2} \sqrt{\frac{V_{th} v_{o_{\text{max}}}}{R_C R_E HD2}} \]

Using \[ R_E \approx \frac{R_{\text{in}}}{\beta} \]

\[ I_C \geq \frac{1}{2} \sqrt{\frac{V_{th} v_{o_{\text{max}}} \beta}{(R_C || R_L) R_{\text{in}} HD2}} \]

- HD2 will dominate, but is not the only distortion term, so you need to use a slightly larger current or put some margin in the HD2 value relative to the THD spec

*This analysis is for a general CE Amp, in our specific circuit \( R_C \Rightarrow R_C || R_L \) and \( R_E \Rightarrow R_E || R_G \)
Key CE Amp Design Equation Summary

Neg. Swing, Rin, $V_{CC}$:

$$I_C \leq \frac{V_{CC} - v_{o \text{max}} - 0.3V - V_E}{R_C}$$

Pos. Swing:

$$I_C \geq \frac{v_{o \text{max}}}{R_C}$$

Gain:

$$I_C \geq \frac{|A_v| V_{th}}{R_C |R_L - \frac{A_v |R_{in}}{\alpha \beta}|}$$

Harmonic Distortion:

$$I_C \geq \frac{1}{2} \sqrt{\frac{V_{th} v_{o \text{max}} \beta}{(R_C |R_L| R_{in})}}$$
Design Example - Specifications

- $|A_v| \geq |-20|$
- $R_{in} \geq 10\,\text{k}\Omega$
- $R_L = 20\,\text{k}\Omega$
- $V_{omax} = 1V_{pk}$ w/ THD $\leq 5\%$ (-26.0dB)
- $V_{CC} = 5V$
- $V_E \geq 0.5V$
- $I_{supply} \leq 1.5mA$
- Nominal operation at 5kHz
Design Equation Plots

• Chosen design point is $I_C = 1\text{mA}$, $R_C = 3k\Omega$

Plots done with $\beta = 150$
DC Operating Points

- $R_E$ is set with $V_E = I_E R_E$
- $R_G$ is set as $R_{in}/\beta$
- DC bias points must be reasonable for the circuit to work as designed!
AC Gain

- $|A_v| = 29.4\text{dB} = 29.5\text{V/V}$
\( R_{\text{in}} \)

- \( R_{\text{in}} = 80.7\, \text{dB}\, \Omega = 10.8\, \text{k}\Omega \)
Transient Response

- Response with 35.5mV_{pk} input signal
- Signal is beginning to compress
Total Harmonic Distortion

- THD = 3.16% = -30dB
\[ R_{\text{out}} = 69.4 \text{dB} \Omega = 2.95 \text{k} \Omega \approx R_C \]
Lab 1 Design Specs

- $|A_v| \geq |-15|$
- $R_{in} \geq 5k\Omega$
- $R_L = 10k\Omega$
- $V_{omax} = 1V_{pk}$ w/ THD $\leq 5\%$ ($-26.0dB$)
- $V_{CC} = 5V$
- $V_E \geq 0.5V$
- $I_{supply} \leq 4mA$
- Nominal operation at 5kHz