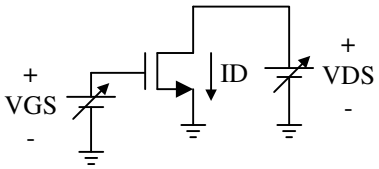
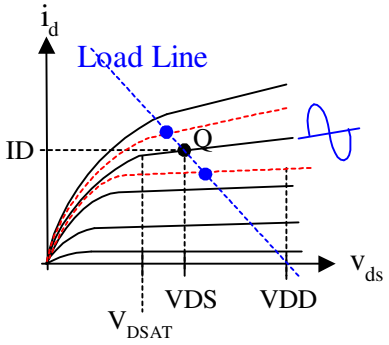
MOSFET DEVICES

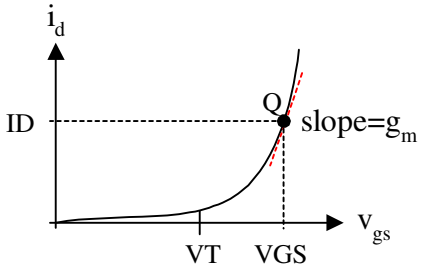
If the MOSFET is operating in saturation, then the following conditions are satisfied:

$$V_{GS} > V_T$$
$$V_{GS} - V_T = V_{DSAT} < V_{DS}$$
$$I_D = \frac{K_P}{2}\frac{W}{L}(V_{DSAT})^2(1+\lambda V_{DS})$$

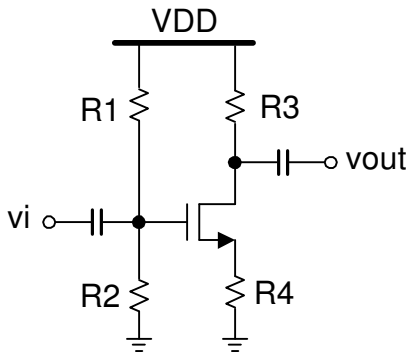


The design procedure starts finding the main parameters of the technology used, specially K_P, VT and lambda. Usually these parameters are given by the technology vendor; if this is not the case you have to simulate a single transistor and find these parameters. By sweeping both VDS and VGS and plotting the variations on ID you can obtain the output characteristics of the MOSFET, as shown below. For the selected VGS> VT, the slope of the ID-VDS curve gives you the value of the transistor's output conductance. Notice that once the bias point is selected, the linear range of the output is limited by VDD and VDSAT (=VGS-VT) for the largest and smallest drain-source voltages, respectively. Keeping VDS>VDSAT, the drain current can also be plotted as function of VGS; this relationship follows a quadratic function with little effect of the VDS voltage. The slope of this plot, around the selected operating point, gives you the value of the small signal transconductance gm, which is one of the fundamental parameters of the MOS transistor.





The typical amplifier when the transistor is biased using resistor is following below. R1 and R2 defines the gate voltage while R3 and R4 determines the source and drain voltage, respectively.



For the definition of the operating point, similarly to the case of bipolar devices, two equations must be solved. For the output, we can write

$$VDD = VDS + I_D(R3 + R4)$$

This equation can be plotted on top of the transistor's output characteristic leading to the load line; selecting the proper VGS (defined by R1 and R2), the intersection of the transistor curve (corresponding to the selected VGS) and the load line determines the operating point Q. The transistor's drain current must be computed by the following equation.

$$I_D = \frac{K_P}{2}\frac{W}{L}(V_{DSAT})^2(1 + \lambda V_{DS})$$

For hand calculations, and to solve the equations more easily, you can neglect the lambda effects; usually the error introduced is less than 5 %.
Similarly, for the gate voltage and since IG=0, we obtain

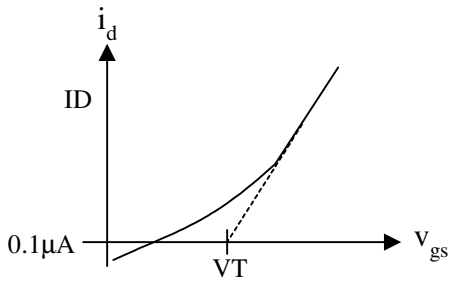
$$VG = \left(\frac{R2}{R1 + R2}\right)VDD$$

and

$$VG = VGS + ID * R4$$

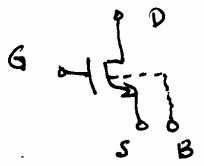
For the analysis and design of circuits using MOS devices you should follow the following procedure:

1. Get the value of the threshold voltage VTO (1 V in this case, but this value depends on the technology used). IF THIS VALUE IS NOT GIVEN, MAKE A VGS-ID CHARACTERIZATION, PLOT IT IN LOG SCALE AND MAKE AN EXTRAPOLATION TO FIND IT.



2. Find the value of KP (=uo*COX), this parameter and the gate dimensions W/L and VDSAT define the transconductance gain of the selected technology (KP ~ 10^{-4} A/V^2 and $0.4*10^{-4}$ A/V^2 for the N-MOS and P-MOS devices, respectively).
3. The lambda factor is very important for the computation of transistor's output resistance. Find it from the ID-VDS characteristics, similarly to the case of the BJT.

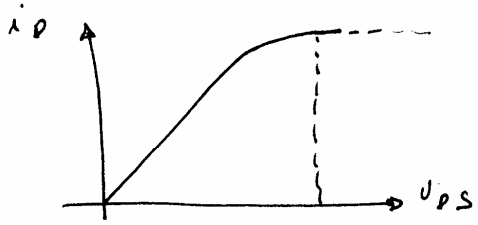
CMOS DEVICES



TRIODE ⇒

i) $i_{DS} = k_p\left(\frac{W}{L}\right)\left(V_{GS} - V_T - \frac{V_{DS}}{2}\right)V_{DS}$ ✓

ii) $V_{DS} < V_{DSAT} = V_{GS} - V_T$ ✓

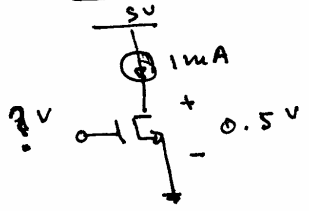


TRIODE ⟵

For small V_{DS} then

$$i_{DS} \simeq k_p \frac{W}{L}\left(V_{GS} - V_T\right)V_{DS}$$

EXAMPLE:



If $\frac{W}{L} = 10$ and $V_T = 1\,V$ then

$V_{GS} = ?$

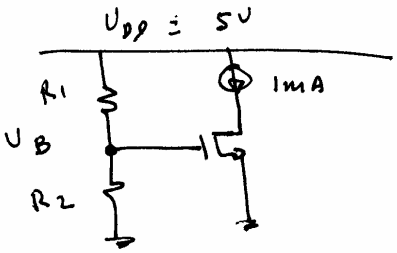
If $k_p = 10^{-4}\ A/V^2$ ⇒

$$1mA = 10^{-4}(10)\left(V_{GS} - 1 - 0.25\right)0.5$$

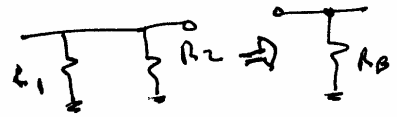
then $V_{GS} = \frac{10^{-3}}{0.5\times10^{-3}} + 1.25 = 2.25$

$V_{DSAT} = V_{GS} - V_T = 2.25 - 1 = 1.25$

If you want to ~~reduce~~ increase the input impedance of your CMOS Amplifier select a proper R_B



$$V_B = V_{GS} = \frac{R_2}{R_1 + R_2} U_{DD}$$

$Z_i \rightarrow$ 

$$U_B = \frac{R_2 V_{DD}}{R_1 + R_2} = \frac{R_1 R_2}{R_1 + R_2} \cdot \frac{V_{DD}}{R_1} = \frac{R_B}{R_1} U_{DD}$$

Then select a proper R_B and compute R_1 and R_2:

Example: $R_B = 1 M\Omega$ then

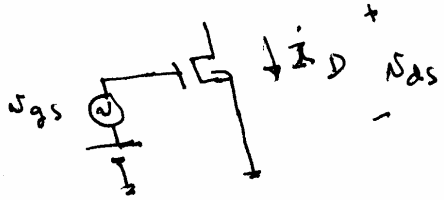
$$R_1 = R_B \frac{V_{DD}}{V_B} = 10^6 \frac{5}{2.25} \simeq 2.2\ M\Omega$$

$$\frac{R_1 R_2}{R_1 + R_2} = R_B \Rightarrow R_2 = \frac{R_1 R_B}{R_1 - R_B} = \frac{2.2 \times 10^{12}}{1.2 \times 10^6}$$

$$R_2 \simeq 1.8\ M\Omega$$

MODEL FOR small signal analysis

$$i_D = K_P \frac{W}{L} \left(V_{GS} - V_T - \frac{1}{2} V_{DS} \right) V_{DS}$$



$i_D(v_{gs}, v_{ds})$ then

Δi_d is function of Δv_{gs} and Δv_{ds}

$$i_d = I_D + \left.\frac{\partial i_d}{\partial v_{gs}}\right|_Q v_{gs} + \left.\frac{\partial i_d}{\partial v_{ds}}\right|_Q v_{ds} + \frac{1}{2}\left.\frac{\partial^2 i_d}{\partial v_{gs}^2}\right|_Q v_{gs}^2$$

$$+ \frac{1}{2}\left.\frac{\partial^2 i_d}{\partial v_{ds}^2}\right|_Q v_{ds}^2 + \cdots$$

$$\left.\frac{\partial i_d}{\partial v_{gs}}\right|_Q = k_p \frac{W}{L} v_{ds}\Big|_Q = k_p \frac{W}{L} \underline{V_{DS}}$$

dc value

$$\left.\frac{\partial i_d}{\partial v_{ds}}\right|_Q = k_p \frac{W}{L}\left(\underline{V_{GS}} - V_T - \underline{V_{DS}}\right)$$

dc values

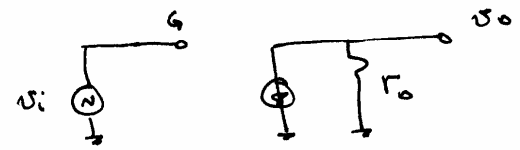
therefore

$$i_D \simeq I_D + \left(k_p \frac{W}{L} V_{DS}\right) v_{gs} + \left(k_p \frac{W}{L}\right)\left(V_{GS} - V_T - V_{DS}\right) v_{ds} +$$

$$+ \text{high order terms}$$

If both v_{gs} and v_{ds} are smaller than V_{OSAT} then the higher order terms can be neglected leading to the small signal model:

AC analysis



$v_o = -g_m r_o v_i$

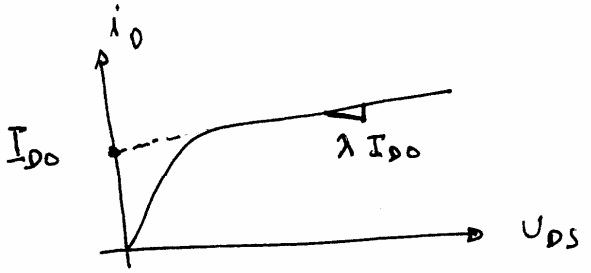
$\frac{v_o}{v_i} = -\frac{g_m}{g_o} = -\frac{5\times10^{-4}}{0.75\times10^{-3}}$

$\boxed{\frac{v_o}{v_i} = -0.66}$

Gain < 1 than signal is attenuated

TRANSISTOR OPERATING IN SATURATION REGION

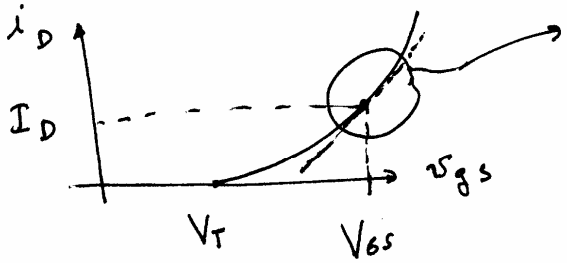
- $U_{DS} > U_{DSAT}$
- $i_D = \frac{K_P}{2}\frac{W}{L}(V_{GS} - V_T)^2(1 + \lambda V_{DS})$



$I_{DO} = \frac{K_P}{2}\frac{W}{L}V_{DSAT}^2$

λ is a result of channel length modulation.

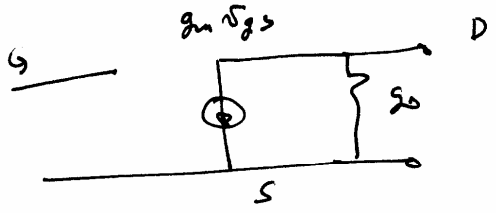
for small signals v_{gs} then



$\left.\frac{\partial i_D}{\partial v_{gs}}\right|_Q = \frac{K_P}{2}\frac{W}{L}(V_{GS} - V_T)(1 + \lambda V_{DS})$

$$\left.\frac{\partial i_D}{\partial v_{DS}}\right|_Q = I_{DO}\,\lambda$$

then



$$g_m = k_p \frac{W}{L}(V_{GS} - V_T)(1+\lambda V_{DS}) = k_p \frac{W}{L} V_{DSAT}(1+\lambda V_{DS})$$

$$\boxed{g_o = \lambda I_{DO}} = \lambda\left(\frac{k_p}{2}\frac{W}{L} V_{DSAT}^2\right)$$

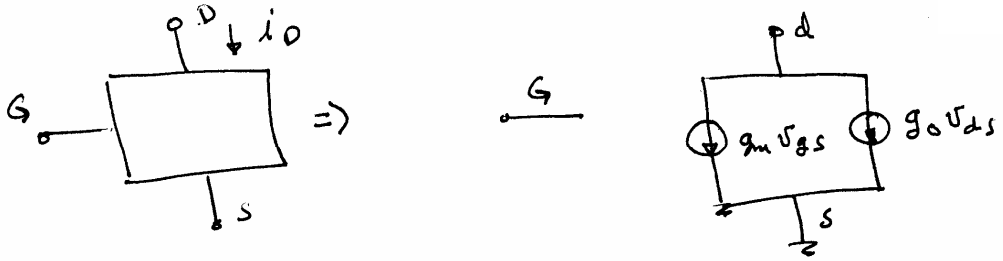
For hand computations

$$\boxed{g_m \simeq k_p \frac{W}{L} V_{DSAT}}$$

and since $I_{DO} = \frac{k_p}{2}\frac{W}{L} V_{DSAT}^2$ then

$$V_{DSAT} \simeq \sqrt{\frac{2 I_{DO}}{k_p \frac{W}{L}}}$$

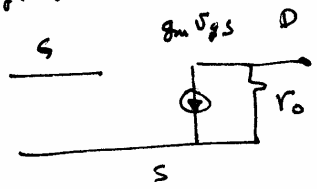
$$\boxed{g_m \simeq \sqrt{2 k_p \frac{W}{L} I_{DO}}}$$



g_m is a transconductance: current flows from drain to source, but it is controlled by gate-source voltage then $g_m v_{gs}$ is a VCCS

g_o is a conductance (why??)

Small signal model for the MO device operating in triode region:



$$g_m = k_p \frac{W}{L} V_{DS}$$

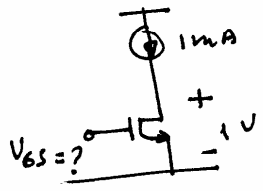
$$r_o = \frac{1}{g_o} = \frac{1}{k_p \frac{W}{L}(V_{GS} - V_t - V_{DS})}$$

From the DC analysis you can compute the small signal parameters g_m and r_o. For instance, for the example previously discussed

$$g_m = 10^{-4}(10)(0.5) = 5 \times 10^{-4} \text{ A/V}$$

$$g_o = 10^{-4}(10)(2.25 - 1 - 0.5) = 10^{-3}(0.75)$$

Example



$V_T = 1V$; $\frac{W}{L} = 100$; $\lambda = 0.02$

then

$$10^{-3} = \frac{10^{-4}}{2}(100)(V_{DSAT}^2)(1 + 0.02)$$

$$V_{DSAT}^2 = \frac{0.2}{1.02} \simeq 0.2$$

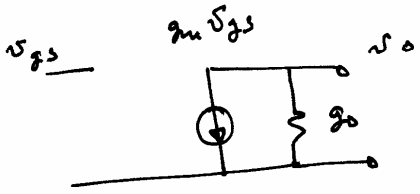
$$V_{DSAT} \simeq 0.447$$

notice that $V_{DSAT} < V_{DS}$ then $V_{GS} = V_T + V_{DSAT} = \underline{1.447V}$

AC analysis: $g_m = k_p \frac{W}{L} V_{DSAT} = 10^{-4} \times 10^2 \times 0.447$

$$g_m = 4.47 \times 10^{-3} \; A/V$$

$$g_o = \lambda I_{DD} = (0.02)(10^{-3}) = 2 \times 10^{-5}$$

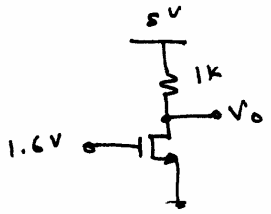


$$v_o = -\frac{g_m v_{in}}{g_o} = \frac{-4.47 \times 10^{-3}}{2 \times 10^{-5}} v_{in}$$

$$\boxed{\frac{v_o}{v_{in}} = -2.23 \times 10^2}$$

EXAMPLE 2

If $V_T = 1V$; GAMMA $= 0$; $K_p = 10^{-4}\ A/V^2$ and $\lambda = 0.02\ V^{-1}$ then



$\frac{W}{L} = \frac{100\ \mu m}{1\ \mu m}$; $V_{GS} = 1.6V$

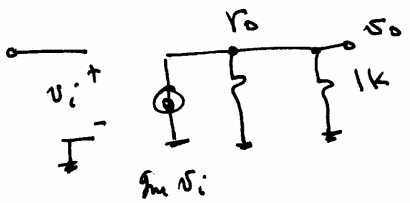
$$I_{DO} = \frac{K_p}{2}\frac{W}{L} V_{DSAT}^2 = \frac{10^{-4}}{2}(100)(1.6-1)^2 = 1.8\ mA/V$$

$$V_{DS} = 5V - I_{DO}(1K) = 5 - 1.8 = 3.2\ V$$

$V_{DSAT} = 0.6\ V \Rightarrow V_{DS} > V_{DSAT}$ TRANSISTOR IS SATURATED

$\Rightarrow$ Small signal parameters: $g_m = K_p \frac{W}{L} V_{DSAT} \cong 6\ mA/V$

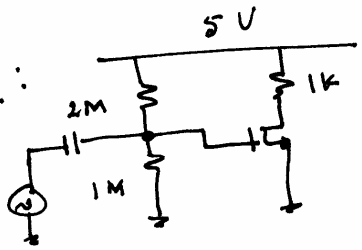
$$r_o = \frac{1}{\lambda I_{DO}} \cong 28K\Omega$$

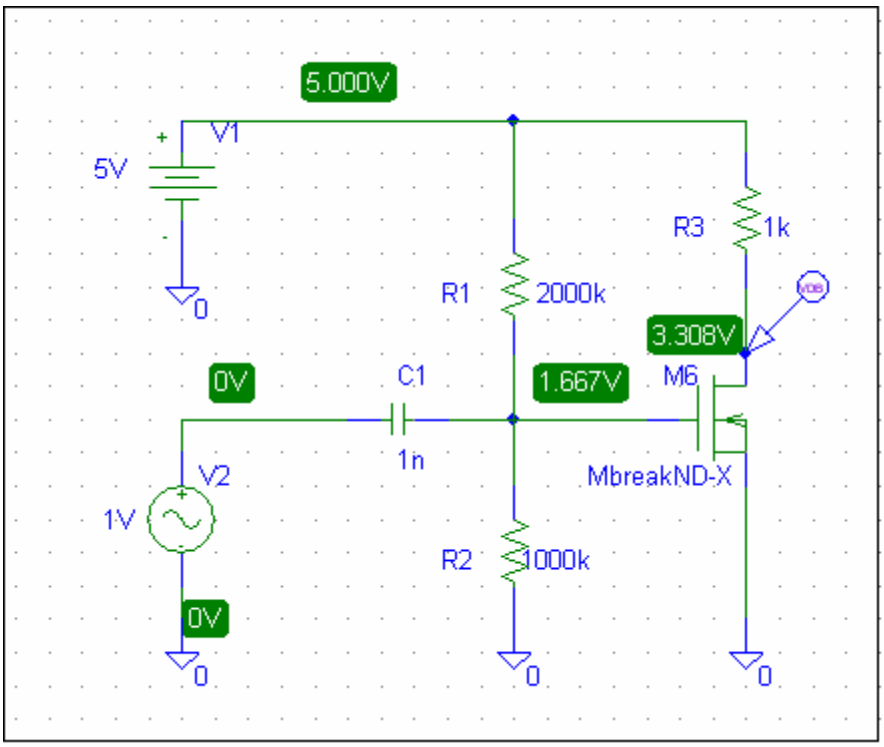


$$\frac{v_o}{v_i} = -g_m(28K \| 1K)$$

$$A_v \cong -6\ V/V$$

FINAL CIRCUIT:





Schematic used for SPICE simulations

Before you start the simuations, YOU MUST TO EDIT THE MODEL OF YOUR TRANSISTOR:

1) SELECT IT FROM THE SCHEMATIC
2) GO TO EDIT, AND SELECT MODEL
3) EDIT THE MODEL AS FOLLOWS (I'm using transistor MbreakND-X)

.model MbreakND-X NMOS
level=2
vto=1.0
tox=238e-10
nsub=33.3e15
ld=-0.05e-6
uo=515
ucrit=28.7e4
vmax=77.3e3
delta=0.0
nfs=0.45e12
rsh=25
js=.01e-3
cgdo=2.9e-10
cgso=2.9e-10
cj=3.4e-4
cjsw=2.5e-10
mj=0.430
mjsw=0.19

pb=0.96
wd=0.40e-6
xj=0.175e-6
cgbo=1.7e-10
uexp=0.251
kf=0.101e-25
neff=5.25
utra=0
af=1.33
*$

Check the operating point of your transistor (DC ANALYSIS). Analyze the result of the output file. You can find the following information:

**** MOSFETS

NAME	M_M6
MODEL	MbreakND-X
ID	**1.69E-03**
VGS	**1.67E+00**
VDS	**3.31E+00**
VBS	**0.00E+00**
VTH	**9.43E-01**
VDSAT	**4.89E-01**
Lin0/Sat1	-1.00E+00
if	-1.00E+00
ir	-1.00E+00
TAU	-1.00E+00
GM	**4.28E-03**
GDS	**7.08E-05**
GMB	1.17E-03
CBD	3.67E-14
CBS	5.90E-14
CGSOV	2.88E-14
CGDOV	2.88E-14
CGBOV	1.87E-16
CGS	1.06E-13
CGD	0.00E+00
CGB	0.00E+00

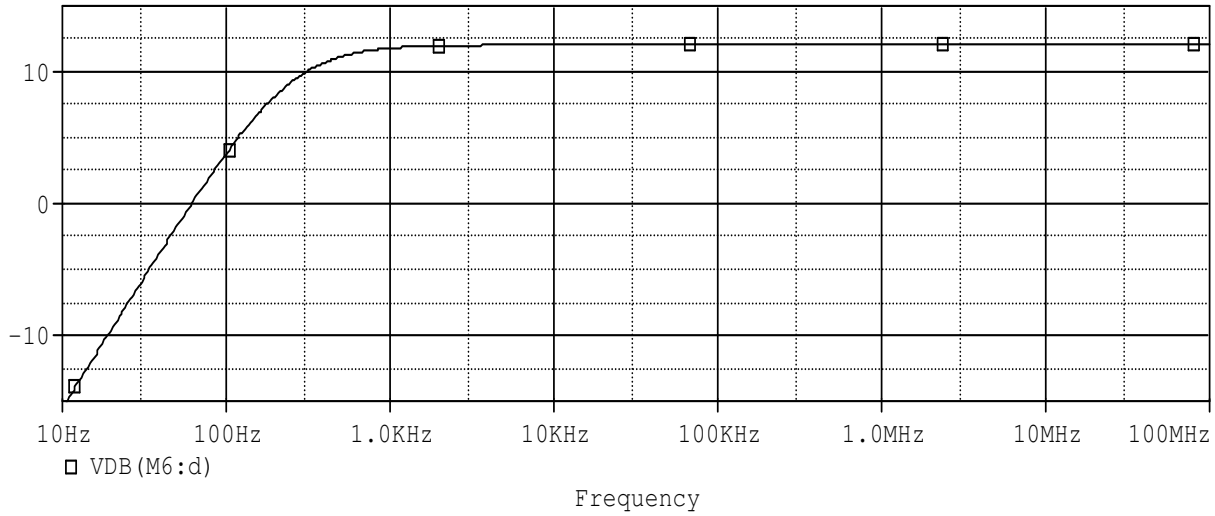
$$A_V = -g_m\left(R_L \,||\, r_o\right)$$

Compare your hand calculations with SPICE results!
The hand calculations give us the following parameters:

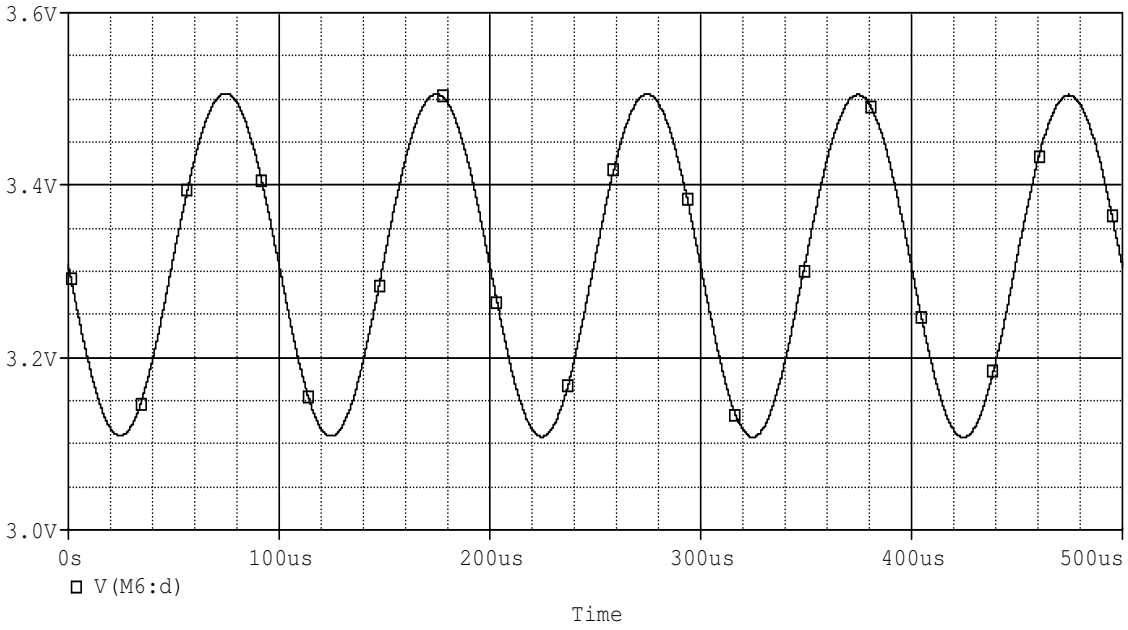
Parameter	Computed	PSPICE
Voltage Gain	-6 (15 dB)	-4 (12 dB)
Drain Current	1.8 mA	1.67 mA
Gm	6 mA/V	4.2 mA/V
KP	100 $\mu A/V^2$	74 $\mu A/V^2$

Note that the voltage gain is off by a large percentage. The explanation of this difference is the value used for KP! For hand calculations we used KP=100 $\mu A/V^2$, but using KP=74 $\mu A/V^2$, it leads to a gm=4.4 mA/V and the voltage gain is around -4.4 V/V, which is very close to the results obtained from SPICE.

After these considerations, analyze both AC and transient results!



AC results for the circuit

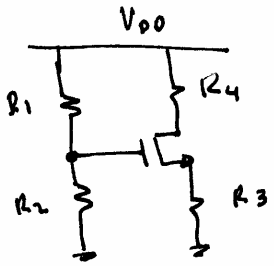


Transient response of the CMOS amplifier with an input signal of 50 mVpk.

AC output is close to 200 mVpk, leading to a gain of 4 (12 dB); this value is in good agreement with the result obtained form the AC analysis.

DO SOME SIMULATIONS YOURSELF!
Try two or 3 stage amplifiers! For gain of 100 for instance!

GENERAL COMMON-SOURCE CONFIGURATION :



- $V_G = \frac{R_2}{R_1 + R_2} V_{DD}$
- $V_{DD} = V_{DS} + I_{D0}(R_3 + R_4)$
- $I_{D0} = \frac{k_P}{2} \frac{W}{L} (V_G - V_S - V_T)^2$
- $Z_i = R_B = \frac{R_1 R_2}{R_1 + R_2}$

⇒ Z_i and V_G ARE defined by R_1 and R_2

SOLVE (?) $V_{DD} = V_{DS} + I_D (R_3 + R_4)$ (1)

$I_{D0} = \frac{k_P}{2} \frac{W}{L} (V_G - V_S - V_T)^2$ (2)

Can you solve the non-linear equations for DC analysis? Just try to solve:

$$I_{D0} = 0.5K_P\left(\frac{W}{L}\right)(V_G - V_S - V_T)^2$$

$$= 0.5K_P\left(\frac{W}{L}\right)(V_G - I_{D0}R_3 - V_T)^2$$

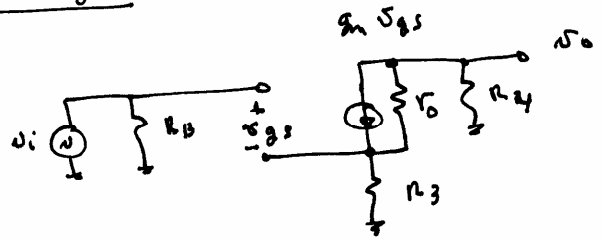
2nd order equation needs to be solved! For that reason, circuit designers prefer to use DC current sources for biasing the CMOS transistor.

Unknowns: I_D, $\frac{W}{L}$, I_{D0}, R_3 and R_4

V_S is defined by I_D as $I_D R_3$

2 equations and 5 variables: are those the only conditions ??

⇒ AC analysis



$v_{gs} = v_i - v_s$ then

$$\left[g_4 + g_o\right] v_o + \left[-g_o - g_m\right] v_s = -g_m v_i$$

$$\left[-g_o\right] v_o + \left[g_m + g_3 + g_o\right] v_s = g_m v_i$$

$$\frac{v_o}{v_i} = \frac{-g_m\left(g_m + g_3 + g_o\right) + g_m\left(g_o + g_m\right)}{\left(g_4 + g_o\right)\left(g_m + g_3 + g_o\right) - g_o\left(g_o + g_m\right)}$$

$$= \frac{-g_m g_3}{g_4\left(g_m + g_3 + g_o\right) + g_o g_3} = -\frac{g_m}{\left(g_m + \frac{1}{r_o}\right)\frac{R_3}{R_4} + \frac{1}{R_4} + \frac{1}{r_o}}$$

$$\boxed{\frac{v_o}{v_i} = -\frac{g_m R_4}{g_m R_3 + \frac{R_3}{r_o} + 1 + \frac{R_4}{r_o}}}$$

Some approximations: If $r_o >> R_3, R_4$ then

$$\boxed{\frac{v_o}{v_i} \cong -\frac{g_m R_4}{1 + g_m R_3}}$$

Notice that If $g_m R_3 >> 1$ then the voltage gain is determined by R_4 / R_3

Design Approach: Fundamental equations.

i) $\underline{R_i} = R_B = R_1 \| R_2$ defined by specs ✓

ii) $\underline{V_{DS}} = V_{DD} - I_D (R_3 + R_4)$ Be sure that V_{DS} is large enough to allocate signal swing (variations)

iii) $I_{DO} = \frac{K_P}{2} \frac{W}{L} (V_{GS} - V_T)^2$

iv) $\frac{v_o}{v_i} \cong - \frac{g_m R_4}{1 + g_m R_3}$

v) $g_m = K_P \frac{W}{L} V_{DSAT} = K_P \frac{W}{L} (V_{GS} - V_T)$

In eqns ii) – v) you have 5 unknowns and 4 equations: Just 1 degree of freedom

Add a reasonable condition:

e.g. – If power is a major issue then

fix $\underline{I_D}$

– Large swing then optimize $\underline{V_{DS}}$

– Precision, then $g_m R_3 > 5-6$ such that

$A_v \cong - R_4/R_3$