

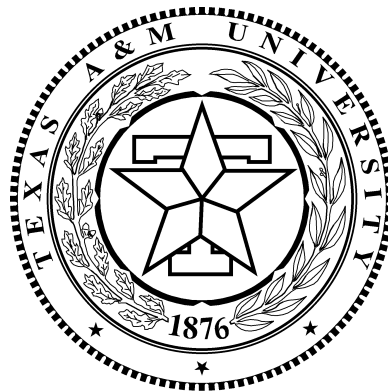
# ECEN 325

## Electronics

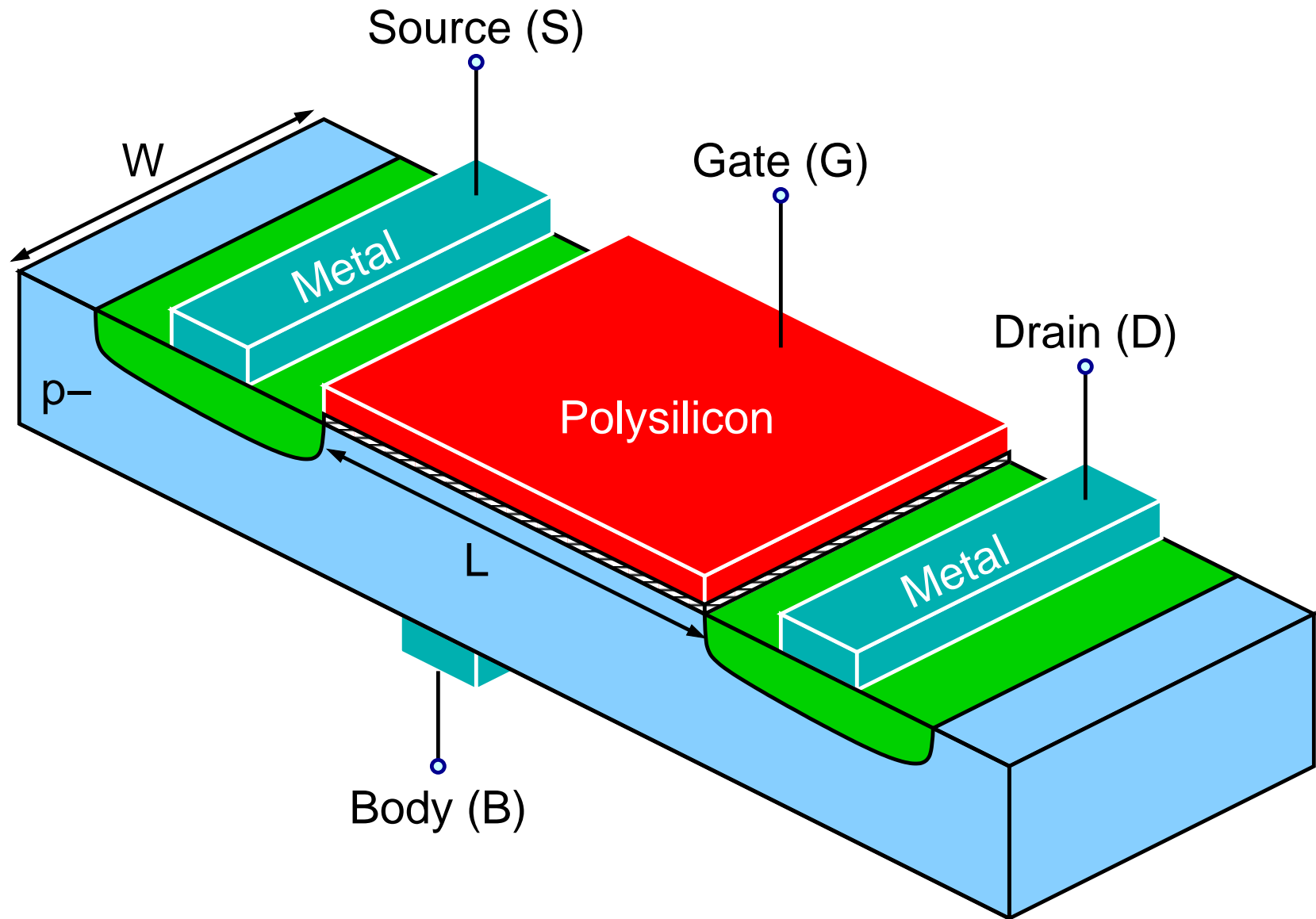
MOS Field-Effect Transistors

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Texas A&M University  
Department of Electrical and Computer Engineering

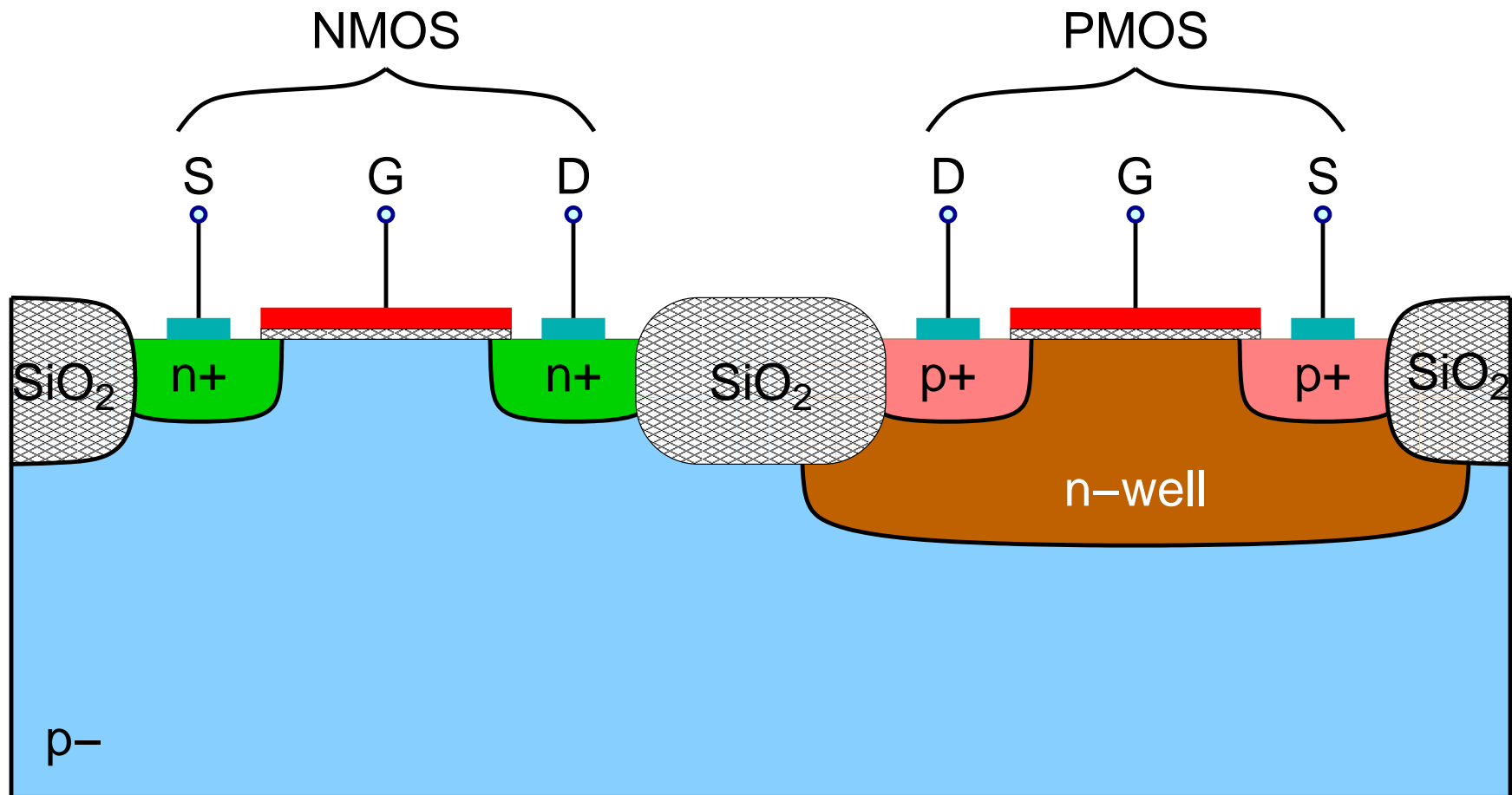


# NMOS Physical Structure



# CMOS Physical Structure

Cross-section



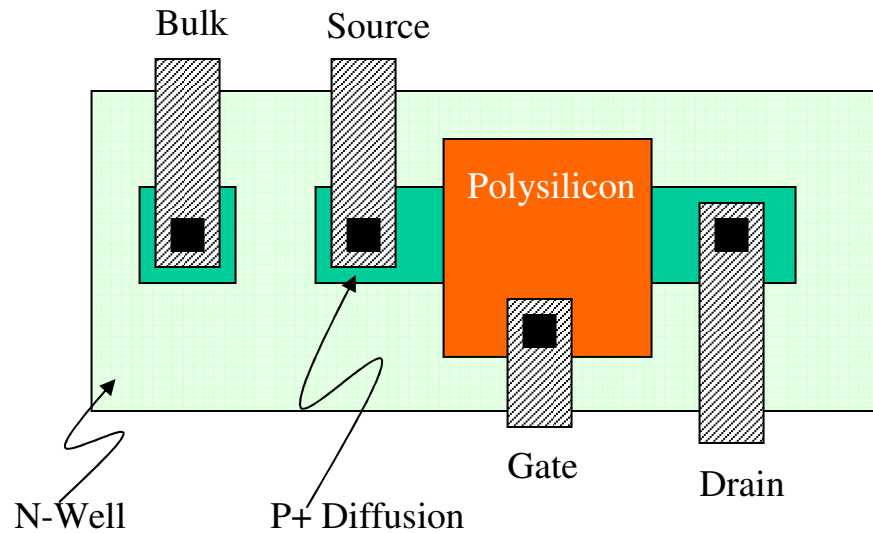
*ELEN - 325*

**Jose Silva-Martinez**

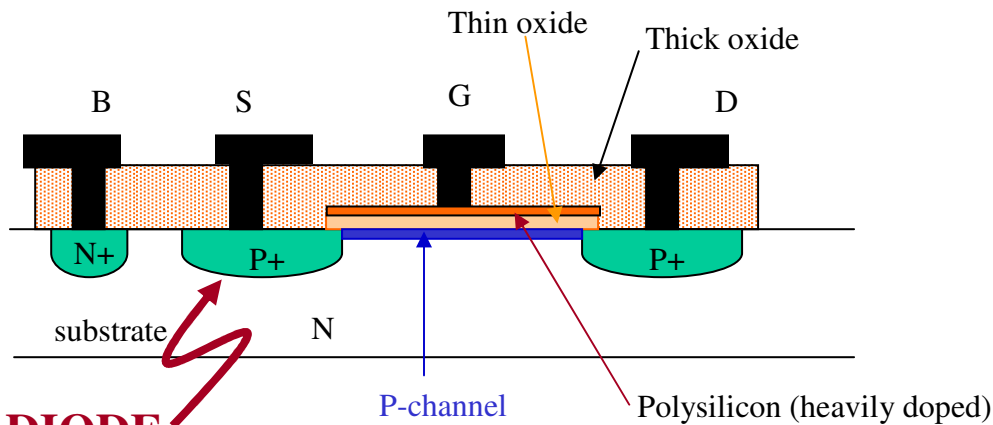
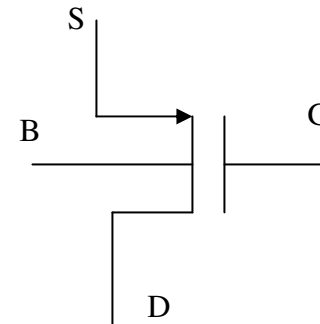
**Texas A&M University  
Department of Electrical Engineering  
Analog and Mixed Center  
College Station, TX**

**[jsilva@ee.tamu.edu](mailto:jsilva@ee.tamu.edu)**

# P-MOS Transistor



## P-type transistor

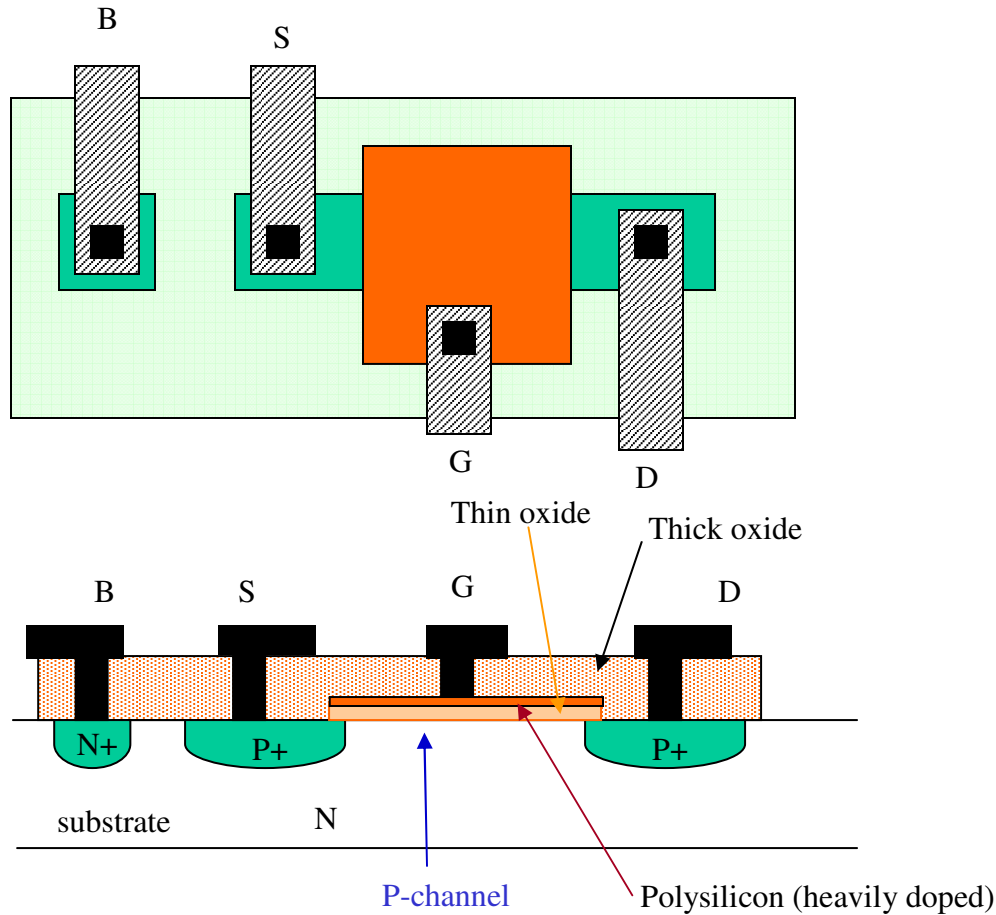


**Basic elements:**

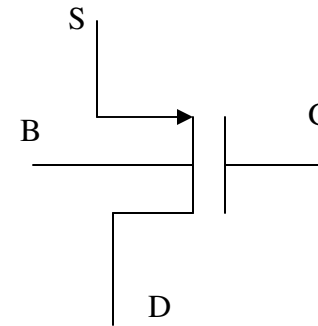
**Diffusions  
+  
Oxidations  
+  
Polysilicon**

**DIODE**

# P-MOS Transistor



## P-type transistor



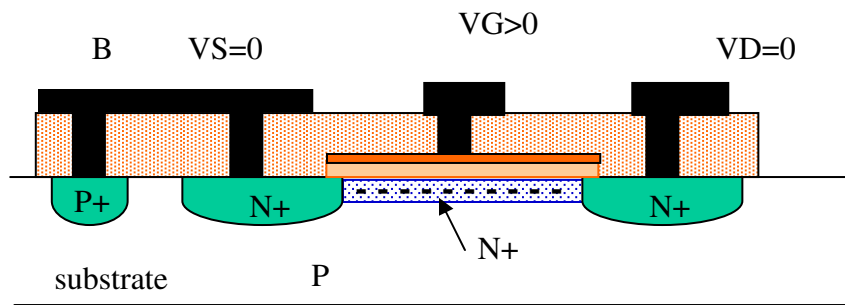
### BASIC IDEA:

**DRAIN-SOURCE CURRENT IS CONTROLLED BY THE GATE.**

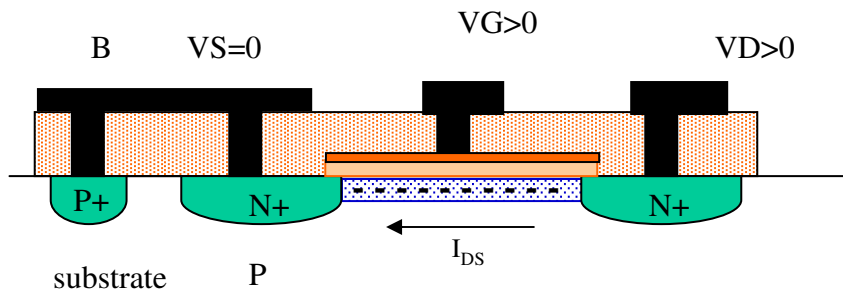
The system is “isolated” if the diodes are biased in reverse using the Bulk terminal.

# N-MOS Transistor

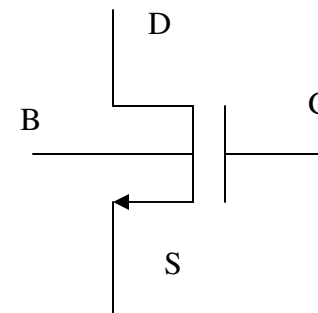
Inversion: channel is created  
D-S current is zero



Inversion: Channel connects D and S  
D-S current is possible



## N-type transistor



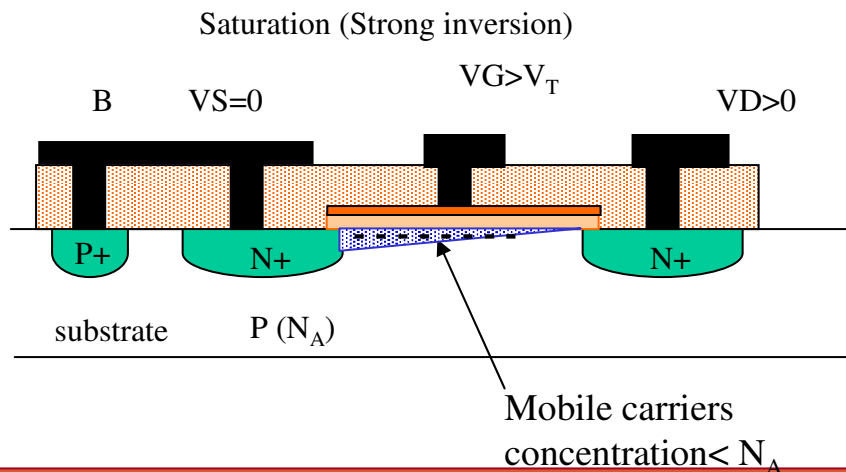
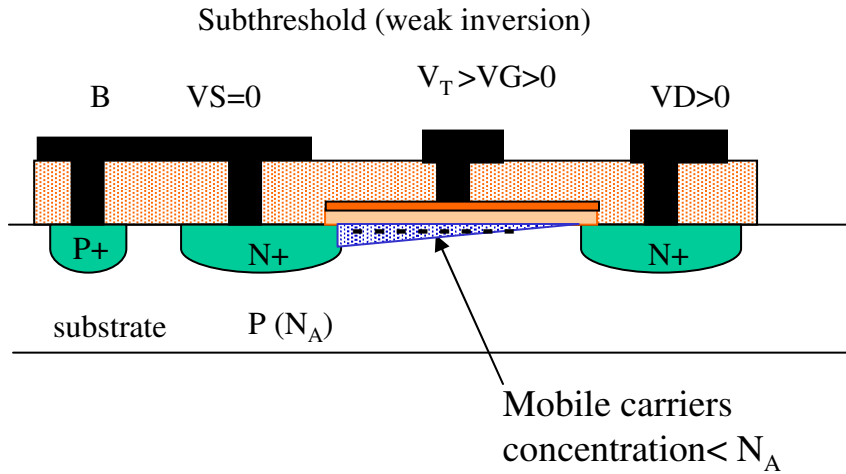
Under this condition, there are 3 possible applications:

**Subthreshold** (extremely low-voltage low-power applications)

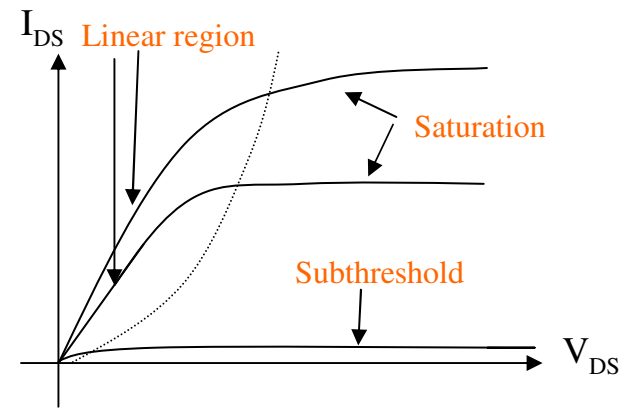
**Linear region** (voltage controlled resistor)

**Saturation region** (Amplifiers)

# MOS Transistor



## N-type transistor



**Subthreshold** (extremely low-voltage low-power applications)

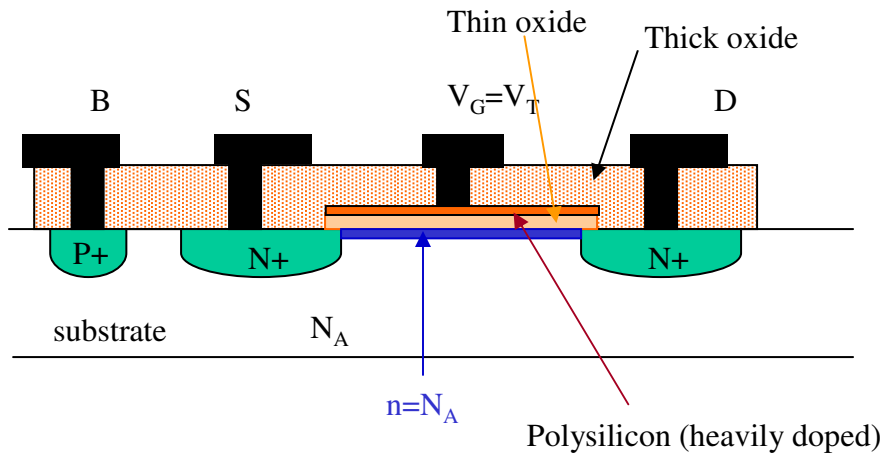
**Linear region** (voltage controlled resistor, linear OTA's, multipliers)

**Saturation region** (Amplifiers)



# MOS Transistor

## STRONG INVERSION : BODY EFFECTS



$$V_T = V_{T0} + \gamma \sqrt{\phi_{j0}} - \gamma \left[ \sqrt{\phi_{j0}} - \sqrt{\phi_{j0} - V_{\text{Channel-B}}} \right]$$

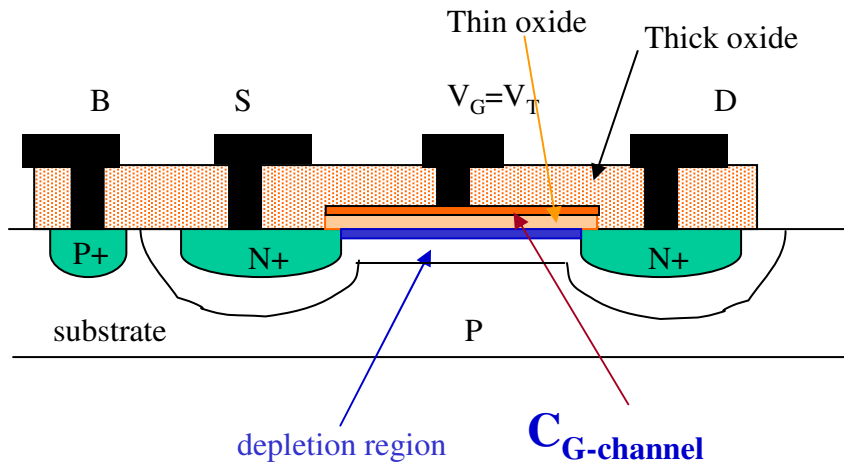
$$\gamma = \frac{\sqrt{2q\epsilon_{si} N_{\text{Bulk}}}}{C_{\text{OX}}} \quad \gamma = \text{BODY FACTOR}$$

### Threshold voltage:

Voltage needed at the gate to create an inversion layer such that the number of carriers in the channel equals the bulk concentration ( $\sim 10^{17}$ - $10^{18}$  electrons /cm<sup>3</sup>)

# MOS Transistor

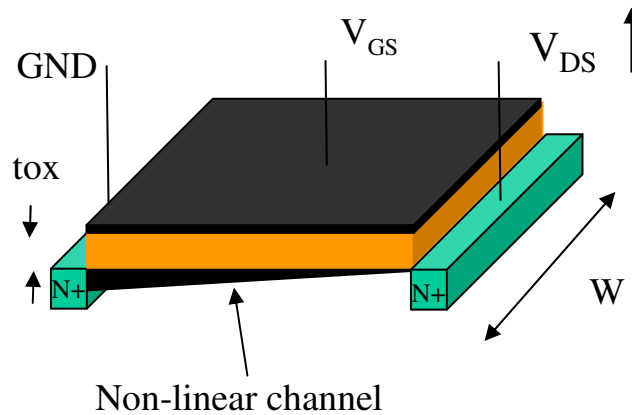
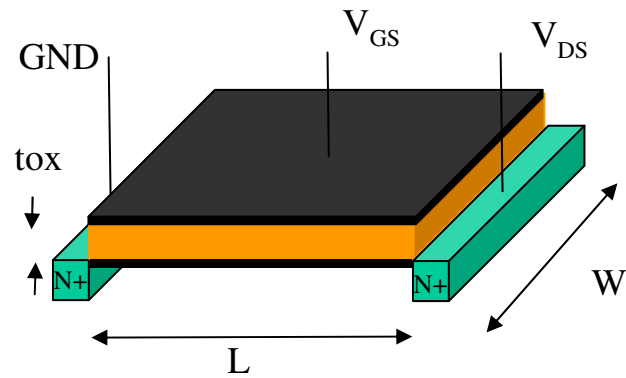
Two control capacitors:  $C_{G\text{-channel}}$  and  $C_{B\text{-channel}}$



**$C_{G\text{-channel}}$**   
**Voltage independent**  
**Its value depends of the gate area**  
**Gate-channel resistance is extremely large**

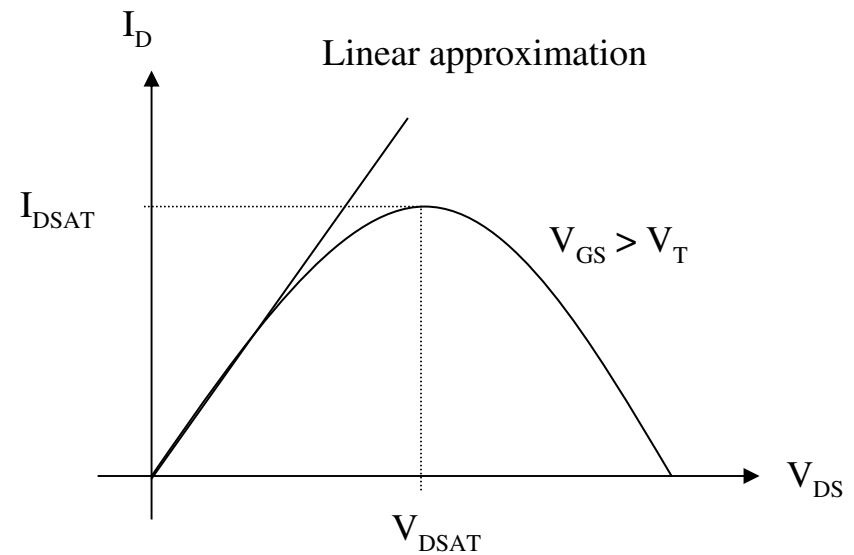
**Channel substrate capacitance:**  
**Voltage dependent ( $\epsilon_{si}/t_{si}$ ) and non-linear**  
**Depends of the gate area**  
**Depends of the square root of the bulk doping**

## MOS Equations in **Linear Region**

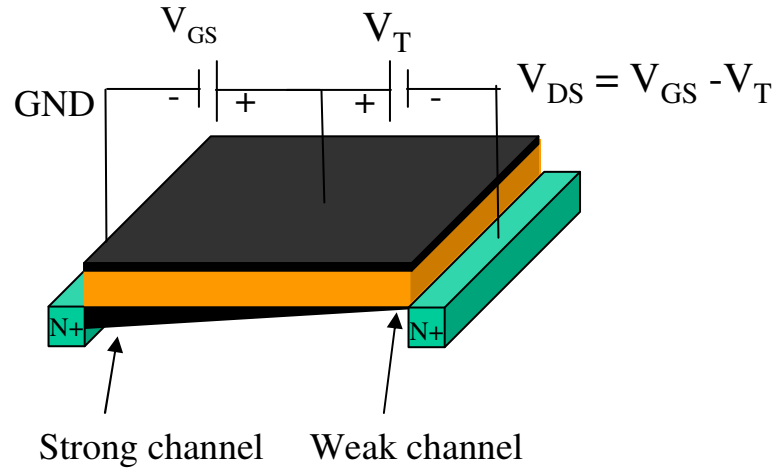


Drain current: Expression used in SPICE level 1

$$I_D = \frac{W}{L} \mu_n C_{OX} (V_{GS} - V_T - 0.5V_{DS}) V_{DS}$$



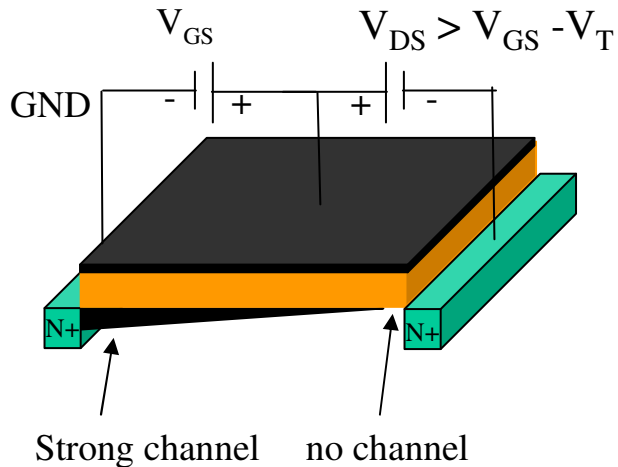
## MOS Equations in Saturation and Linear Region



$$I_D = \frac{W}{2L} \mu_n C_{OX} (V_{GS} - V_T)^2$$

SATURATION REGION ( $V_{DS} > V_{GS} - V_T$ )

Carriers are attracted to the drain, and swept in the region where channel is incomplete (why??)



Current is still given by

$$I_D = \frac{W}{2L} \mu_n C_{OX} (V_{GS} - V_T)^2$$

or

$$I_{DSAT} = \frac{W}{2L} \mu_n C_{OX} (V_{DSAT})^2$$

SPICE level 1

# MOS MODEL: Fundamental equations

- Drain current, Triode region

$$i_D = \mu C_{OX} \frac{W}{L_{eff}} [V_{GS} - V_T - 0.5V_{DS}] V_{DS}$$

- Drain Current, Saturation region

$$i_D = \frac{\mu C_{OX}}{2} \frac{W}{L_{eff}} [V_{GS} - V_T]^2 [1 + \lambda V_{DS}]$$

- Threshold voltage (zero bias)

$$V_{T0} = V_{FB} + 2\phi_F + \gamma \sqrt{2\phi_F}$$

- Threshold voltage

$$V_T = V_{T0} + \gamma [\sqrt{2\phi_F + V_{SB}} - \sqrt{2\phi_F}]$$

- KP (Spice Model)

$$KP = \mu C_{OX}$$

# MOS MODEL: Some values frequently used

•KP

•N-MOS  $10^{-4}$  A/V

•P-MOS  $0.3 \cdot 10^{-4}$  A/V

•VT0

N-MOS 0.7V

P-MOS 1V

•Vearly

N-MOS 10 V/ $\mu$ m

P-MOS 15 V/ $\mu$ m