ECEN325: Electronics
Spring 2024

Metal-Oxide-Semiconductor Field Effect Transistor (MOSFET)

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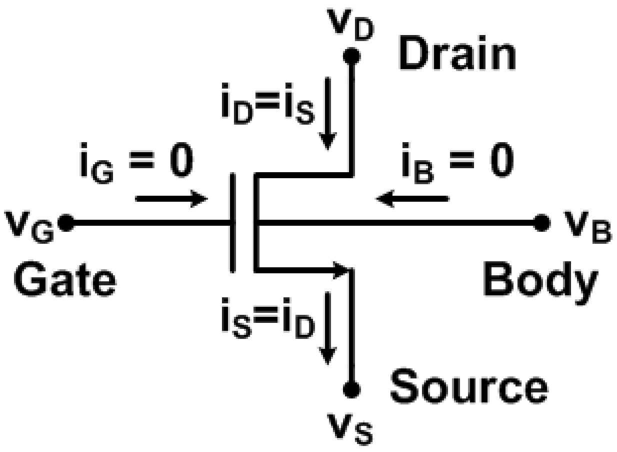
Announcements & Reading

- HW 6 due Apr 25

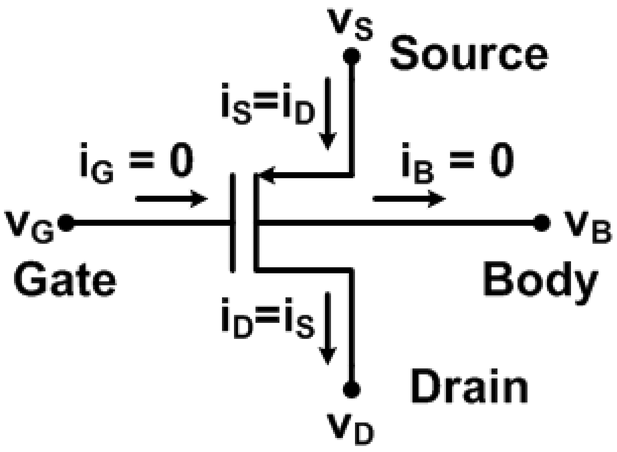
- MOSFET Reading
  - Razavi Ch6 – MOSFET Models
  - Razavi Ch7 – MOSFET Amplifiers

MOSFET Circuit Symbols

NMOS

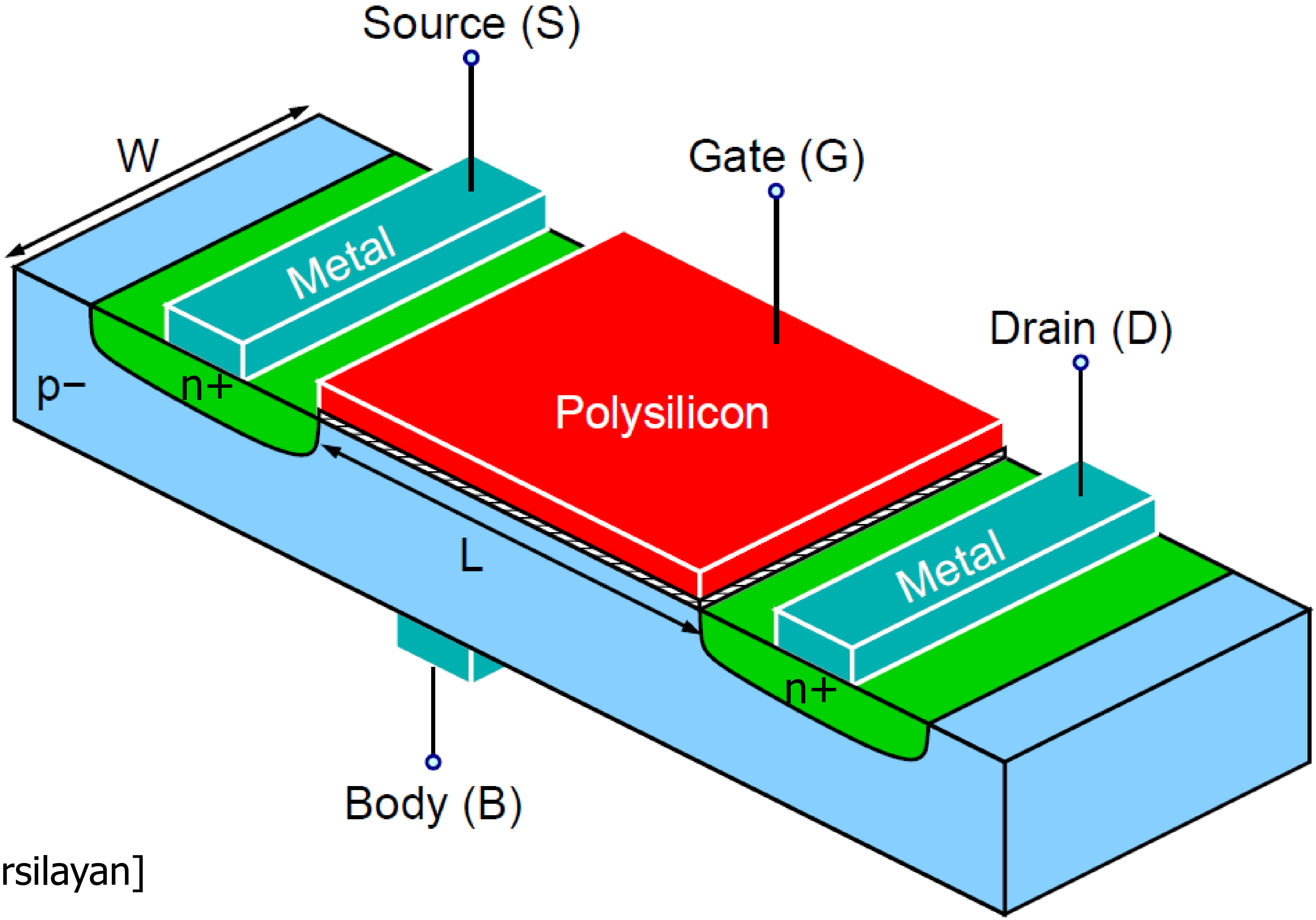


PMOS



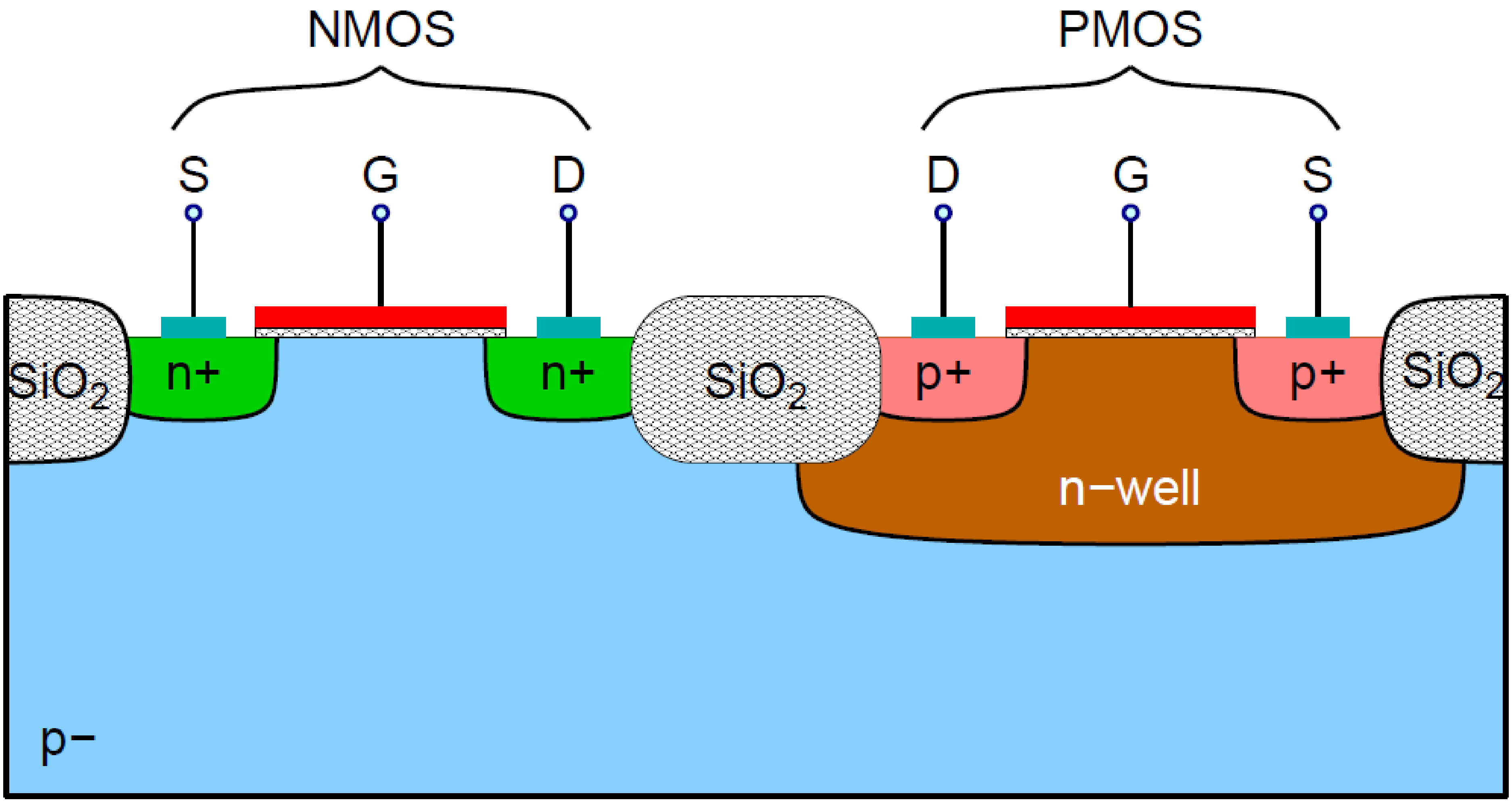
- MOSFETs are 4-terminal devices
  - Drain, Gate, Source, & Body
- Body terminal generally has small impact in normal operation modes, thus device is generally considered a 3-terminal device
  - Drain, Gate, and Source are respectively similar to the Collector, Base, and Emitter of the BJT
- 2 complementary MOSFETS: NMOS, PMOS

NMOS Physical Structure



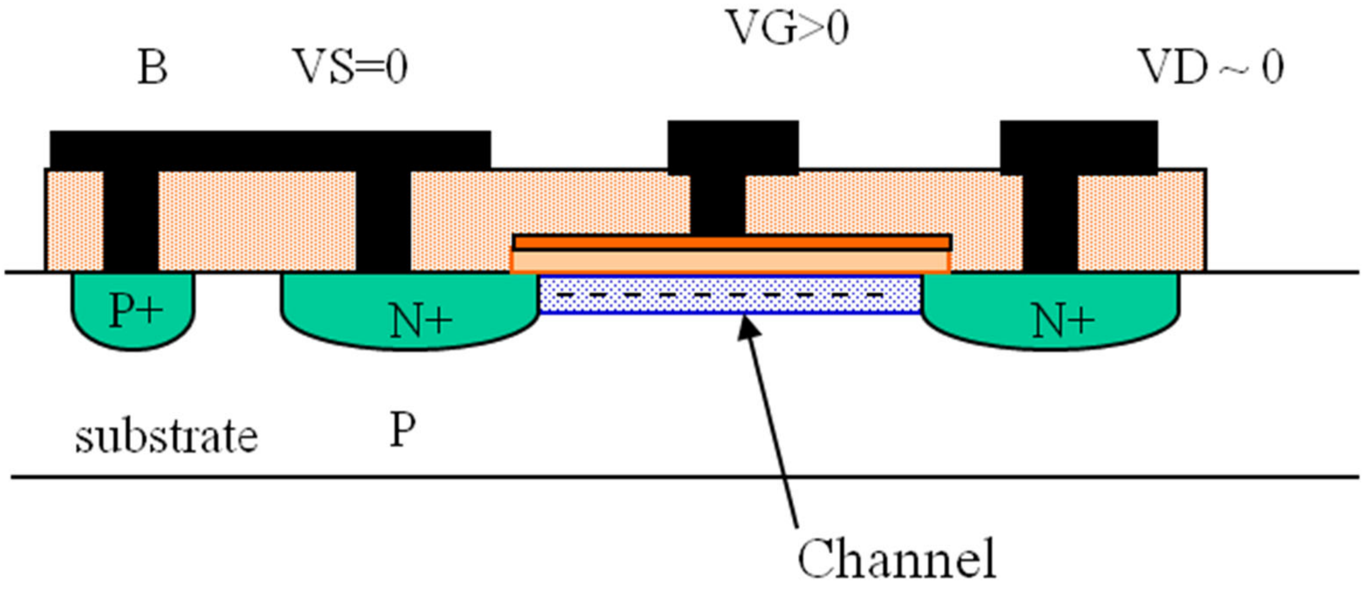
[Karsilayan]

CMOS Physical Structure



[Karsilayan]

V_{TH} Definition

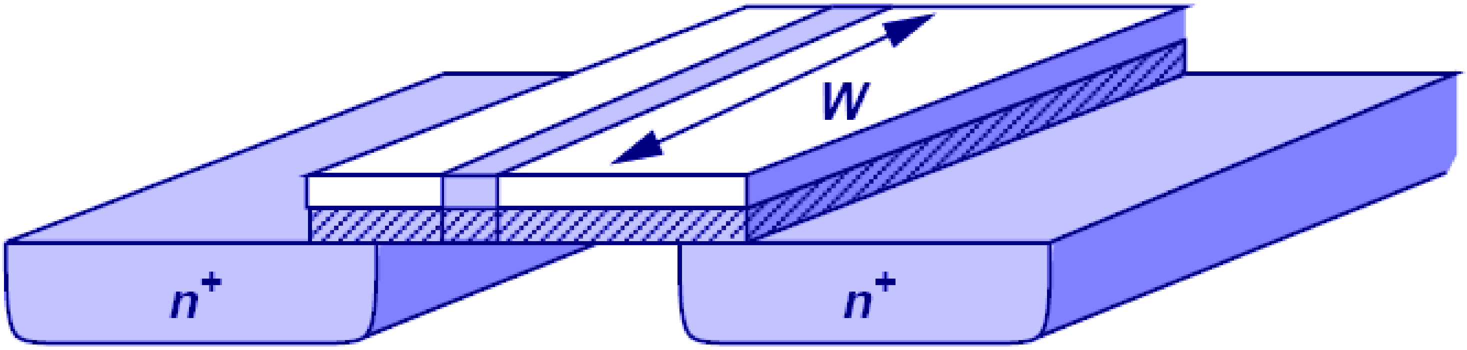


[Silva]

- The threshold voltage, V_{TH}, is the voltage at which an "inversion layer" is formed
  - For an NMOS this is when the concentration of electrons equals the concentration of holes in the p^- substrate

Drain Current Derivation: Channel Charge Density

[Razavi]

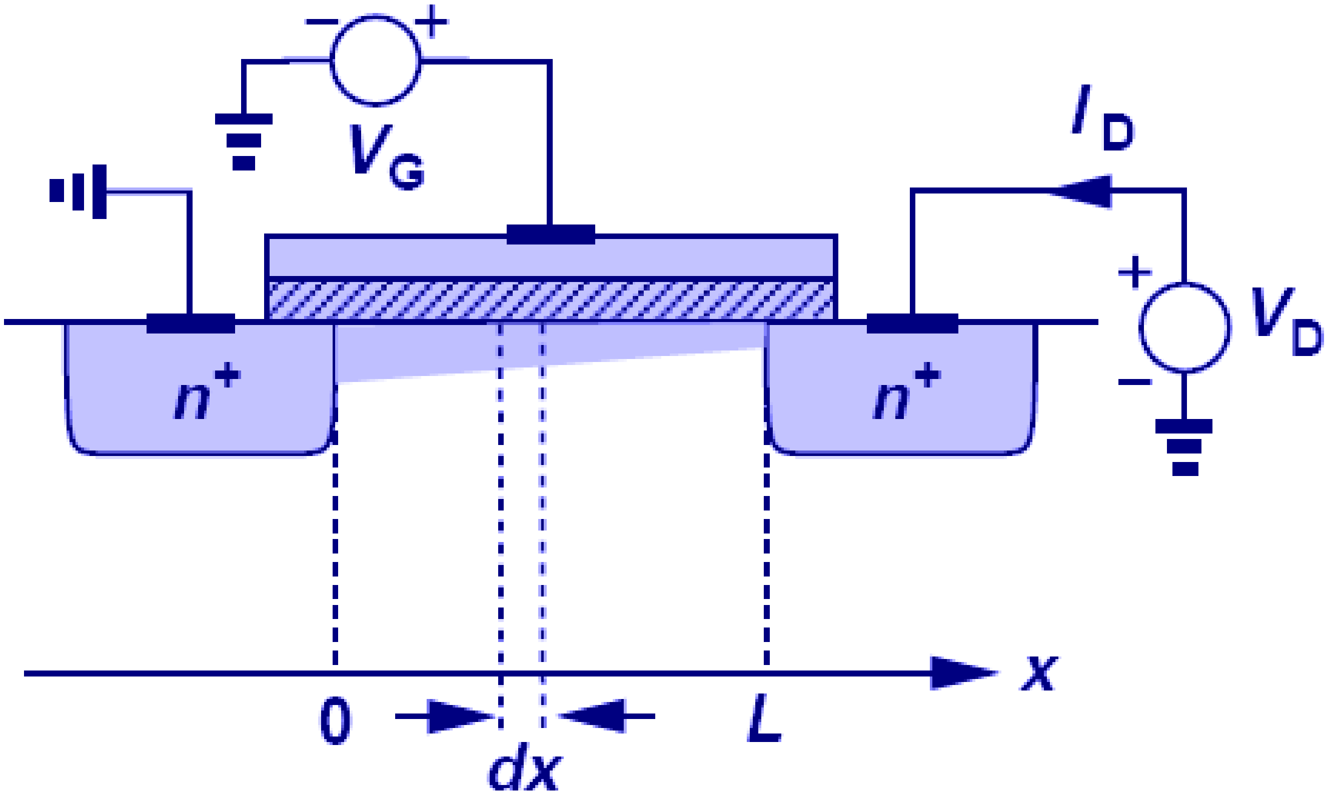


$$Q = WC_{ox}(V_{GC} - V_{TH})$$

$$\text{where Capacitane per unit gate area}: C_{ox} = \frac{\varepsilon_{ox}}{t_{ox}}$$

- **The incremental channel charge density is equal to the gate capacitance times the gate-channel voltage in excess of the threshold voltage.**

Drain Current Derivation: Charge Density at a Point



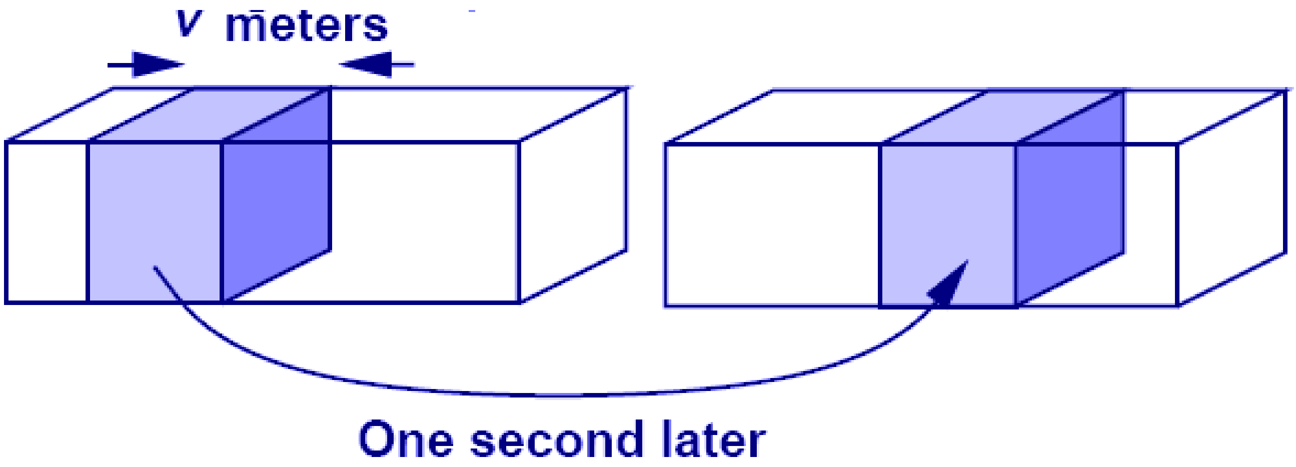
[Razavi]

$$Q(x) = WC_{ox}\left[V_{GS} - V(x) - V_{TH}\right]$$

- Let x be a point along the channel from source to drain, and V(x) its potential; the expression above gives the charge density (per unit length).

Drain Current Derivation: Charge Density and Current

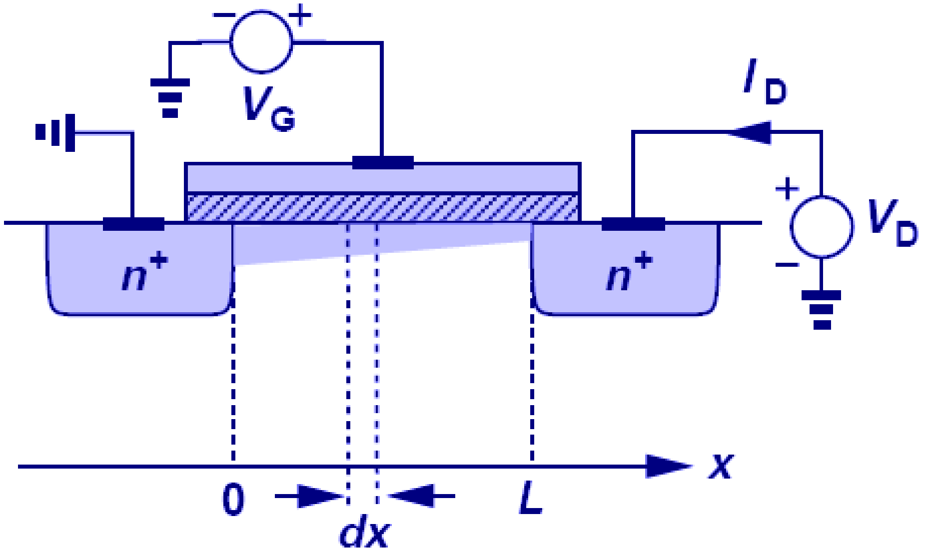
[Razavi]



$$\boxed{I = Q \cdot v}$$

- **The current that flows from source to drain (electrons) is related to the charge density in the channel by the charge velocity.**

Drain Current Derivation: Triode Region (Small V_{DS}) Current Equation



[Razavi]

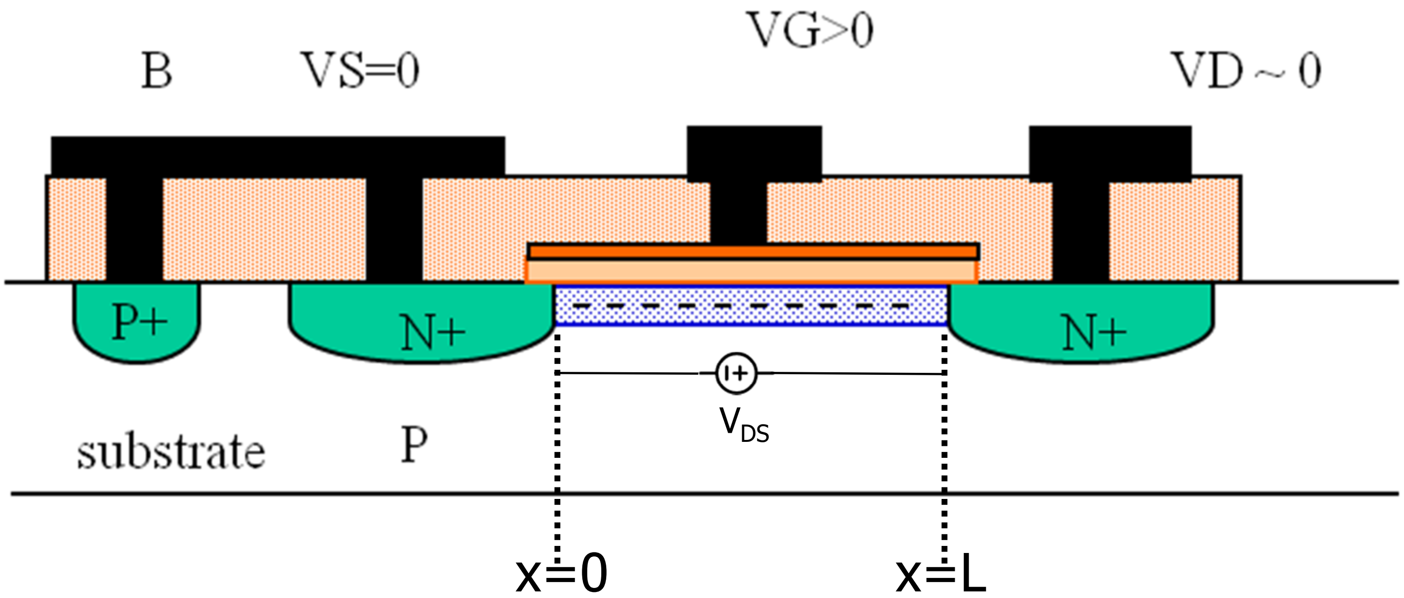
$$\text{Electron Velocity:} \quad v = +\mu_n \frac{dV}{dx}$$

$$I_D = Q(x)v = WC_{ox}\left[V_{GS} - V(x) - V_{TH}\right]\mu_n \frac{dV(x)}{dx}$$

$$\int_{x=0}^{x=L} I_D dx = \int_{V(x)=0}^{V(x)=V_{DS}} \mu_n C_{ox} W\left[V_{GS} - V(x) - V_{TH}\right] dV(x)$$

$$\boxed{I_D = \mu_n C_{ox} \frac{W}{L}\left[V_{GS} - V_{TH} - \frac{1}{2}V_{DS}\right]V_{DS}}$$

Triode or Linear Region



[Silva]

$$V(0)=0 \qquad V(x)=V_{DS}\frac{x}{L} \qquad V(L)=V_{DS}$$

$$V_{GC}(x)=V_{GS}-V(x)=V_{GS}-V_{DS}\frac{x}{L}$$

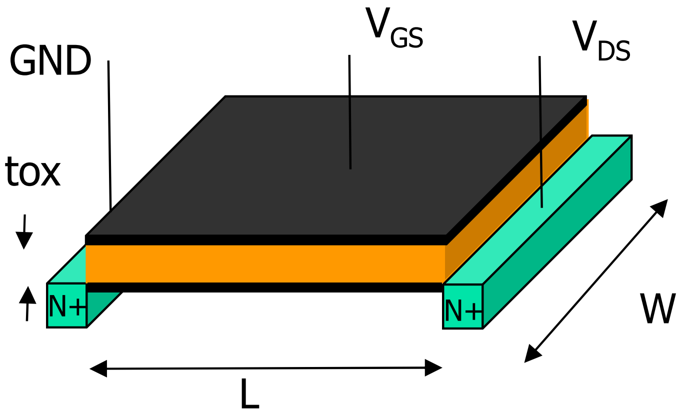
- Channel depth and transistor current is a function of the overdrive voltage, V_{GS}-V_T, and V_{DS}
- Because V_{DS} is small, V_{GC} is roughly constant across channel length and channel depth is roughly uniform

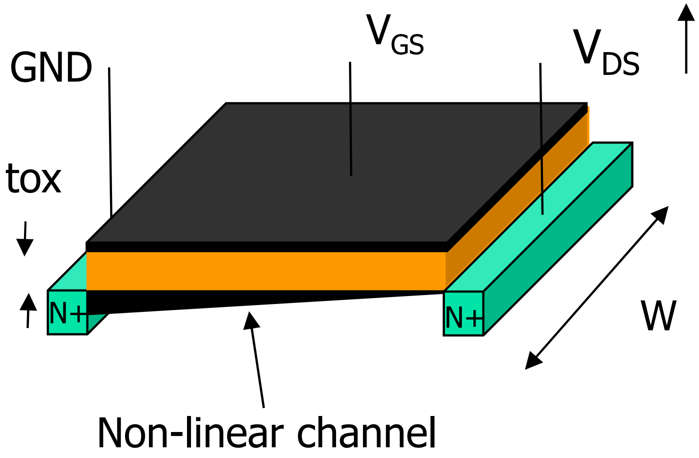
$$\boxed{I_{DS}=\frac{W}{L}\mu_n C_{OX}\left(V_{GS}-V_{Tn}-0.5V_{DS}\right)V_{DS}}$$

→ For small V_{DS}

$$\boxed{R_{DS}\approx\frac{1}{\frac{W}{L}\mu C_{ox}\left(V_{GS}-V_{Tn}\right)}}$$

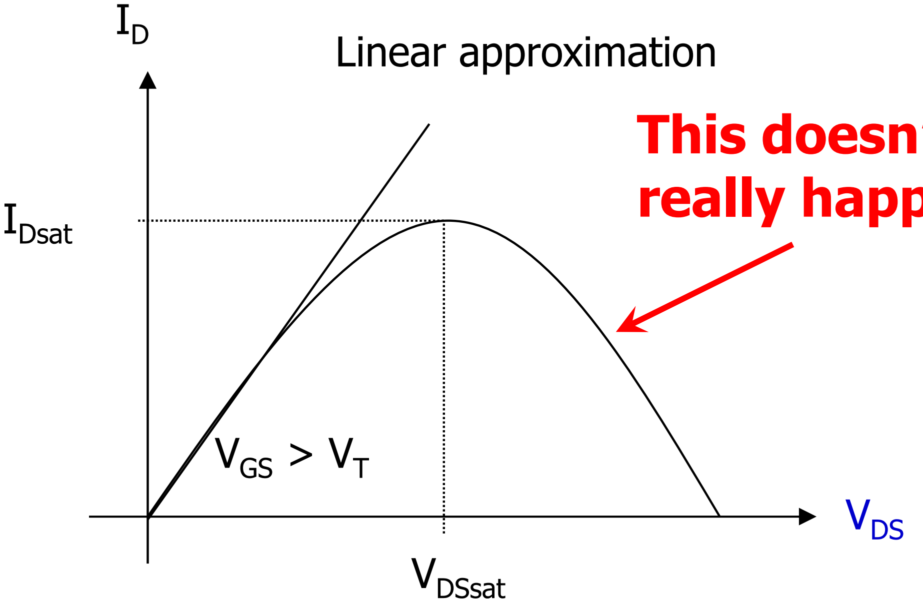
MOS Equations in Triode Region (Large V_{DS})





Drain current: Expression used in SPICE level 1

$$I_{DS} = \frac{W}{L}\mu_n C_{OX}\left(V_{GS} - V_{Tn} - 0.5V_{DS}\right)V_{DS}$$



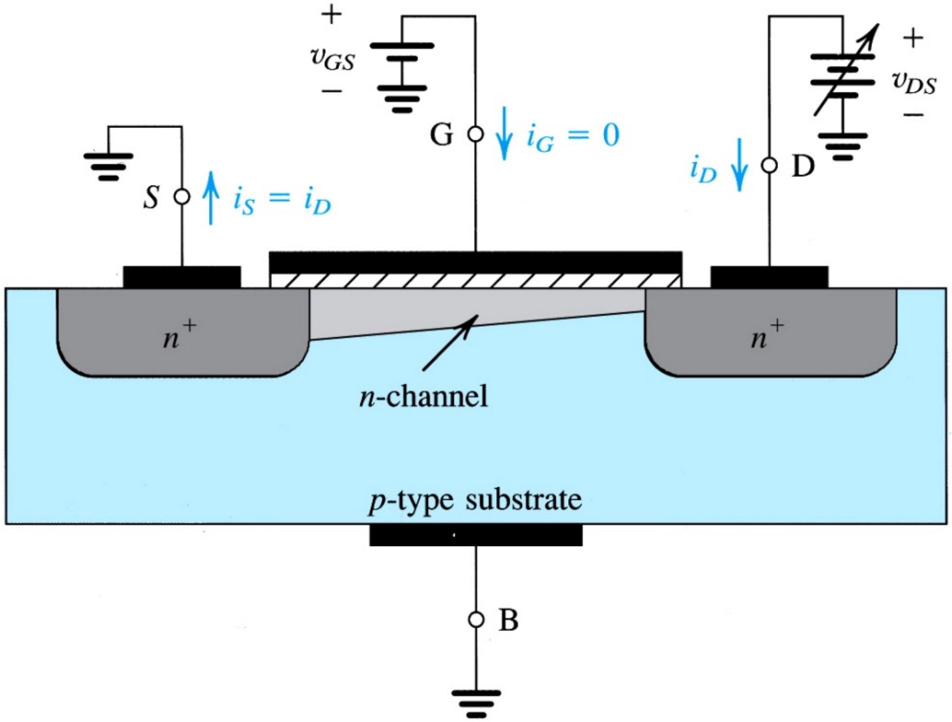
This doesn't really happen

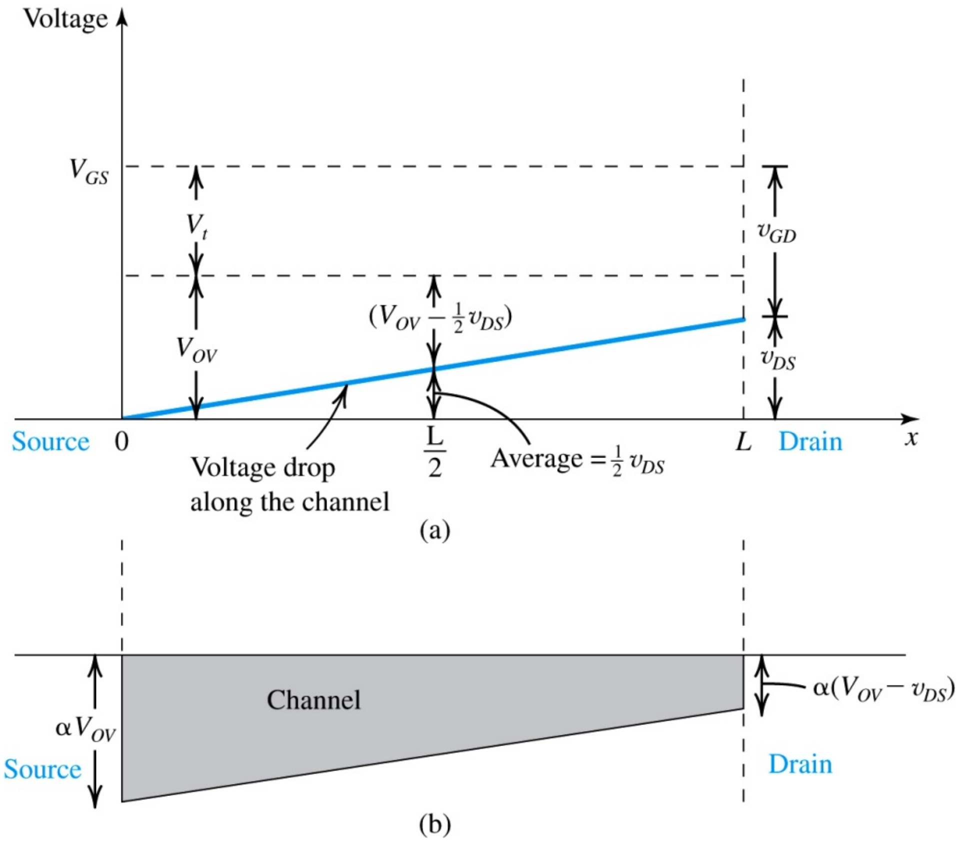
$$V_{DSsat} = V_{GS} - V_{Tn}$$

Triode Region Channel Profile

[Sedra/Smith]

$$V_{GC}(x) = V_{GS} - V(x) = V_{GS} - V_{DS}\frac{x}{L}$$



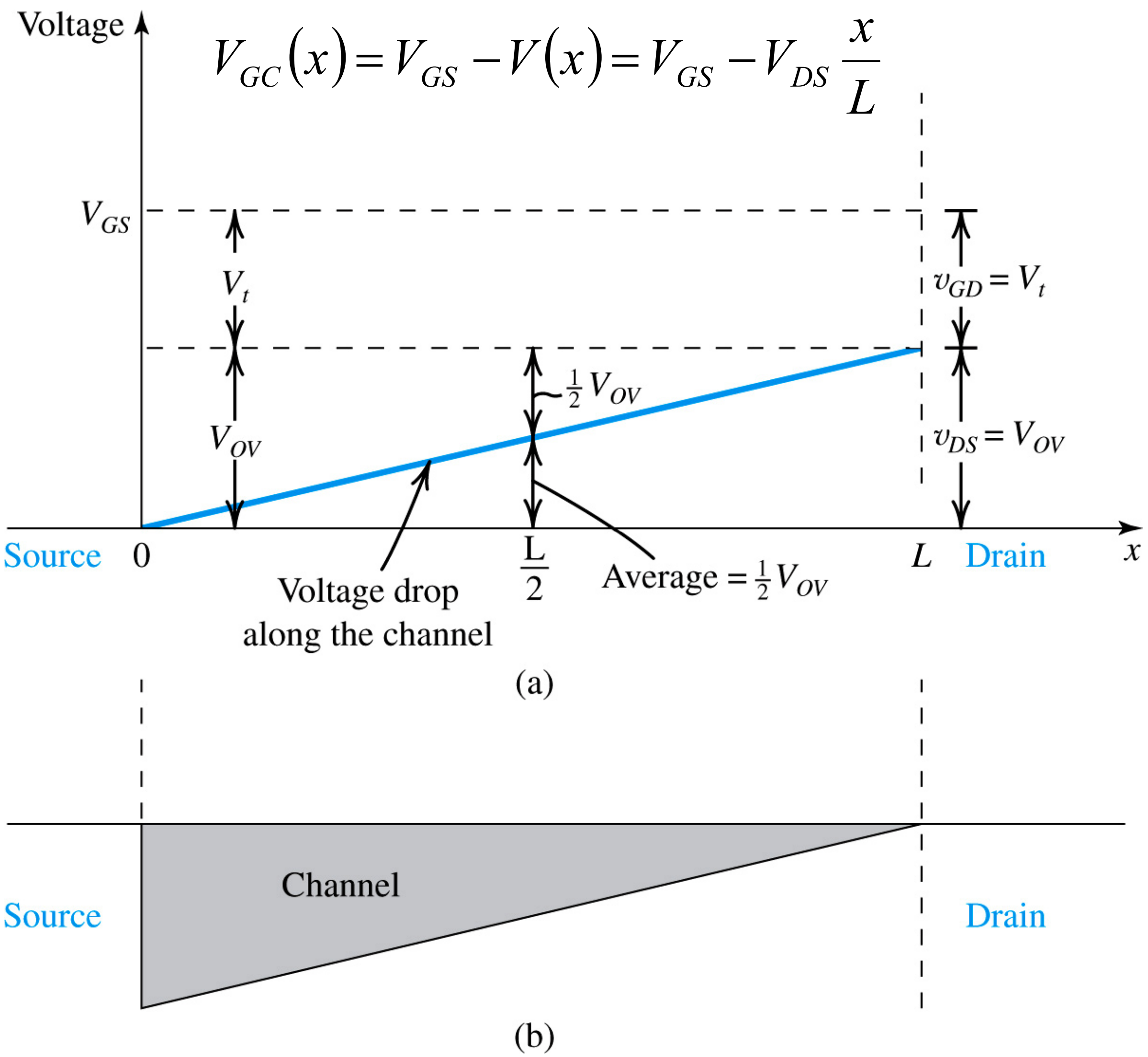


(a)

(b)

- If V_{GC} is always above V_T throughout the channel length, the transistor current obeys the triode region current equation

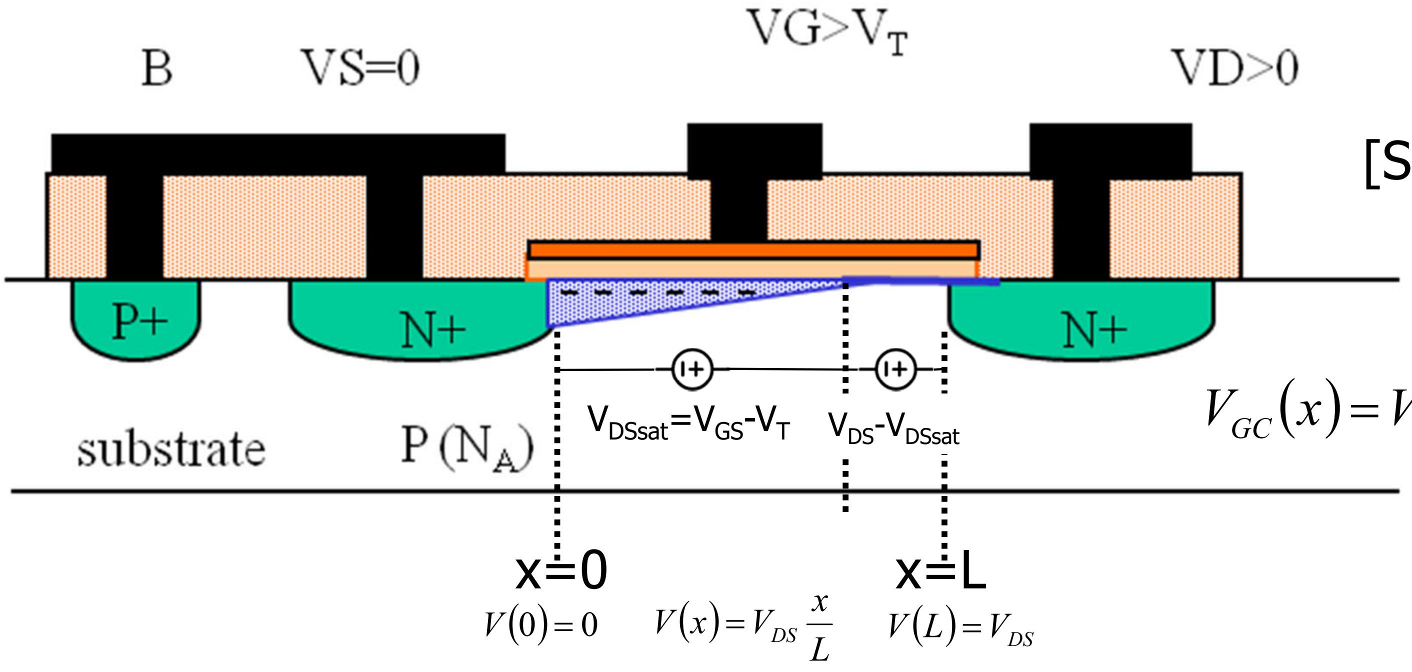
Saturation Region Channel Profile



[Sedra/Smith]

- When $V_{DS} \geq V_{GS}-V_{TH}=V_{OV}$, V_{GC} no longer exceeds V_{TH}, resulting in the channel “pinching off” and the current saturating to a value that is no longer a function of V_{DS} (ideally)

Saturation Region



[Silva]

$$V_{GC}(x)=V_{GS}-V(x)=V_{GS}-V_{DS}\frac{x}{L}$$

- Channel “pinches-off” when $V_{DS}=V_{GS}-V_{TH}$ and the current saturates
- After channel charge goes to 0, the high lateral field “sweeps” the carriers to the drain and drops the extra V_{DS} voltage

$$I_{DS}=\mu_n C_{OX}\frac{W}{L}\left(V_{GS}-V_{Tn}-\frac{V_{DS}}{2}\right)V_{DS}\Bigg|_{V_{DS}=V_{GS}-V_{Tn}}$$

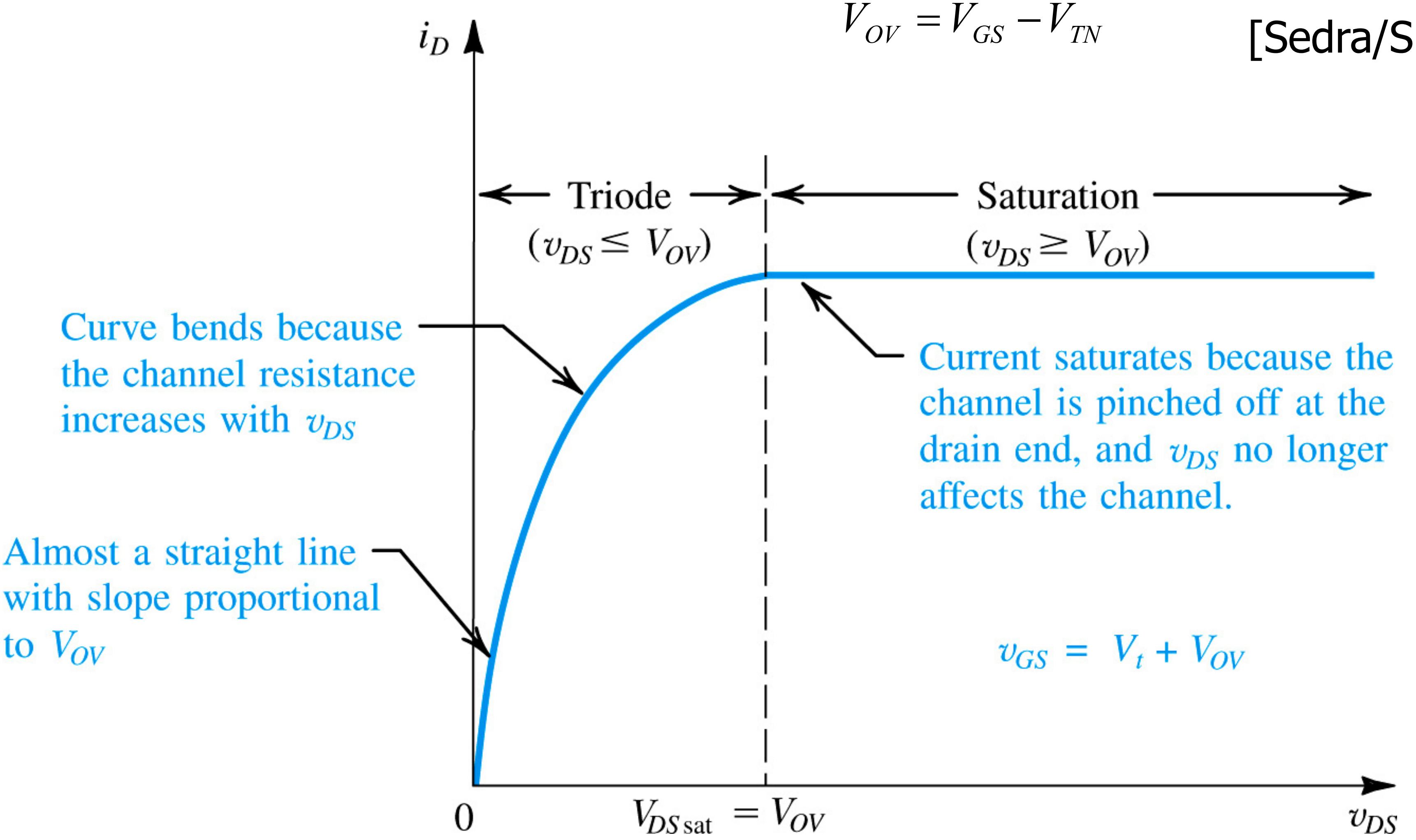
$$\boxed{V_{DSsat}=V_{GS}-V_{Tn}}$$

$$\boxed{I_{DS}=\frac{\mu_n C_{OX}}{2}\frac{W}{L}(V_{GS}-V_{Tn})^2}$$

NMOS I_D – V_{DS} Characteristics

$V_{OV} = V_{GS} - V_{TN}$

[Sedra/Smith]



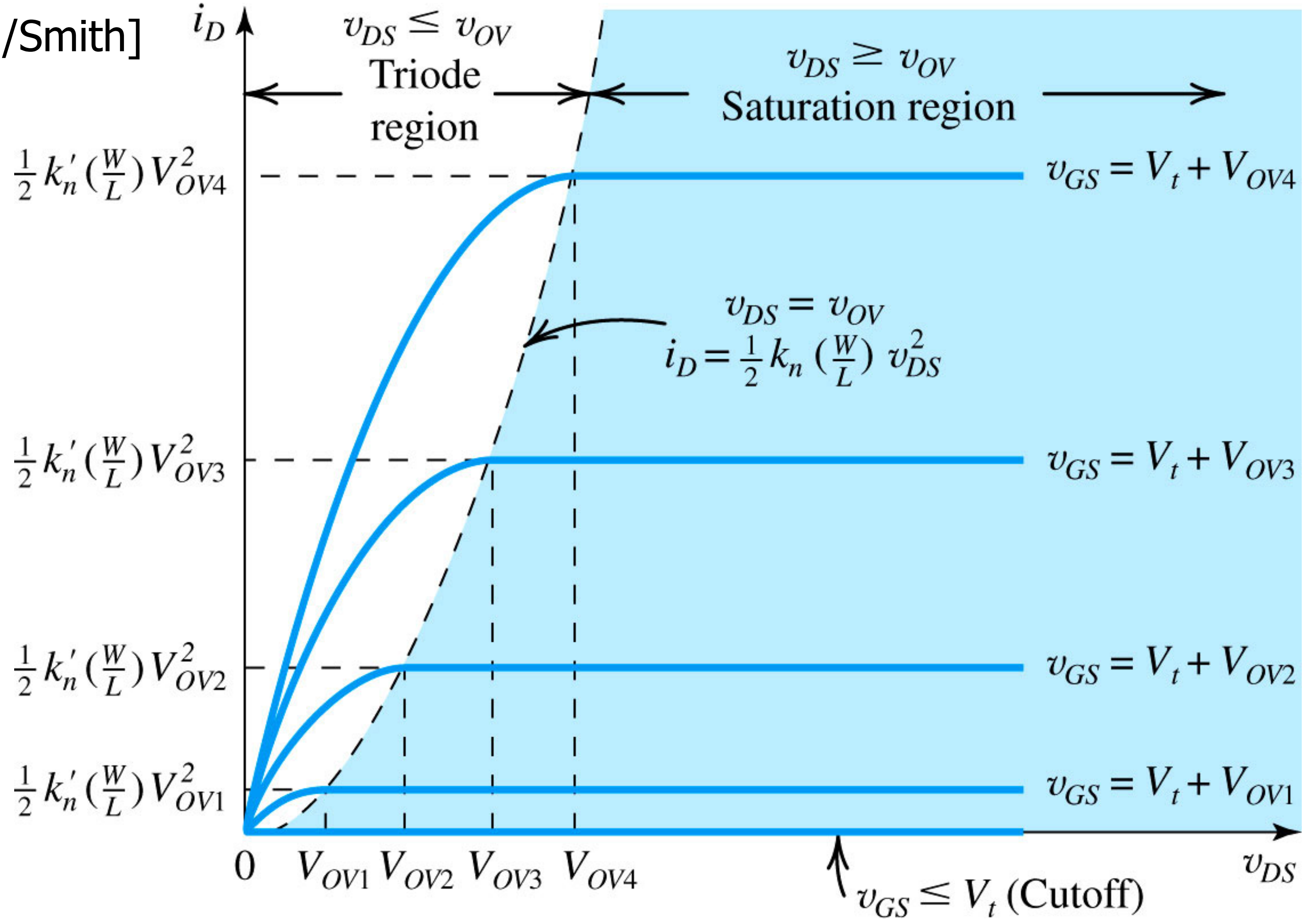
Curve bends because the channel resistance increases with v_{DS}

Almost a straight line with slope proportional to V_{OV}

Current saturates because the channel is pinched off at the drain end, and v_{DS} no longer affects the channel.

MOS "Large-Signal" Output Characteristic

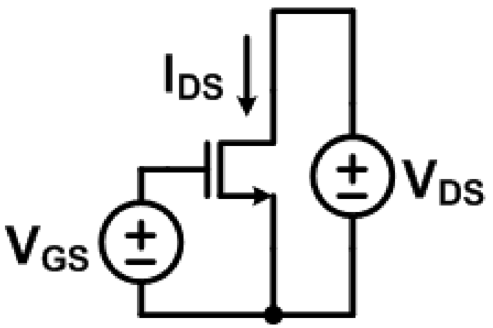
[Sedra/Smith]



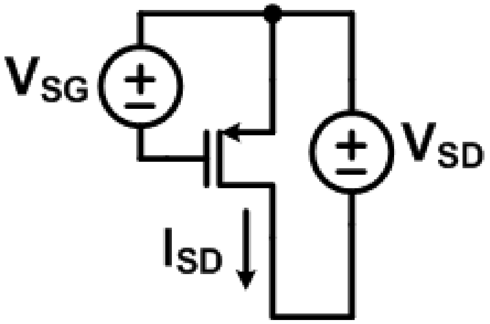
Note: $V_{ov}=V_{GS}-V_T$

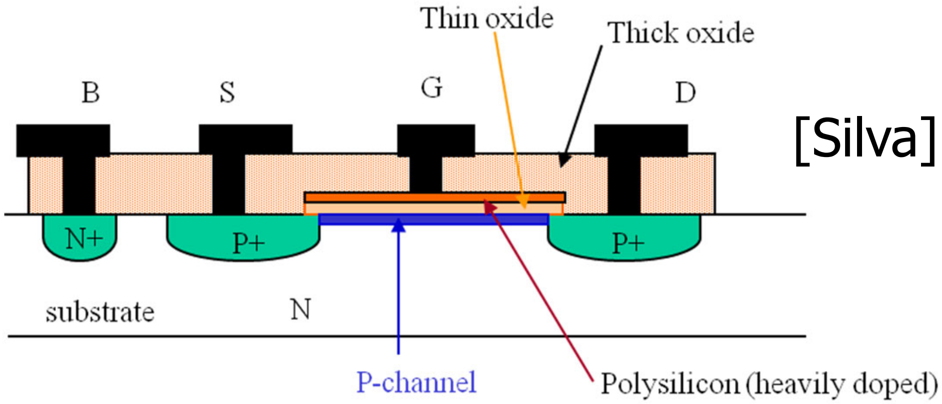
What about the PMOS device?

NMOS



PMOS



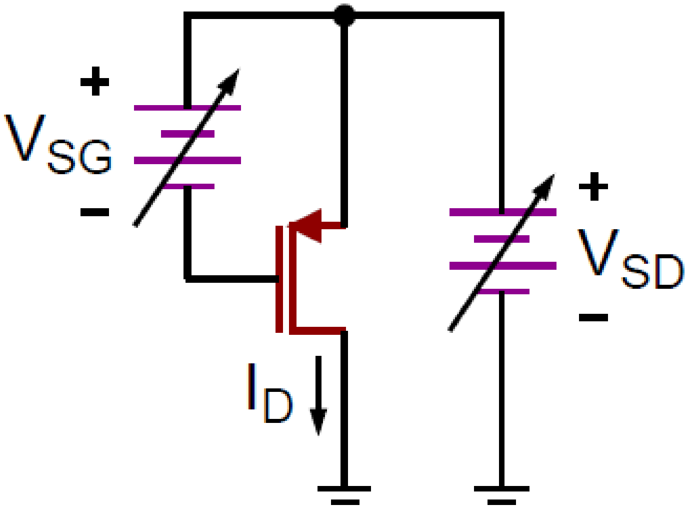


[Silva]

- The current equations for the PMOS device <u>are the same</u> as the NMOS **EXCEPT** you swap the current direction and all the voltage polarities

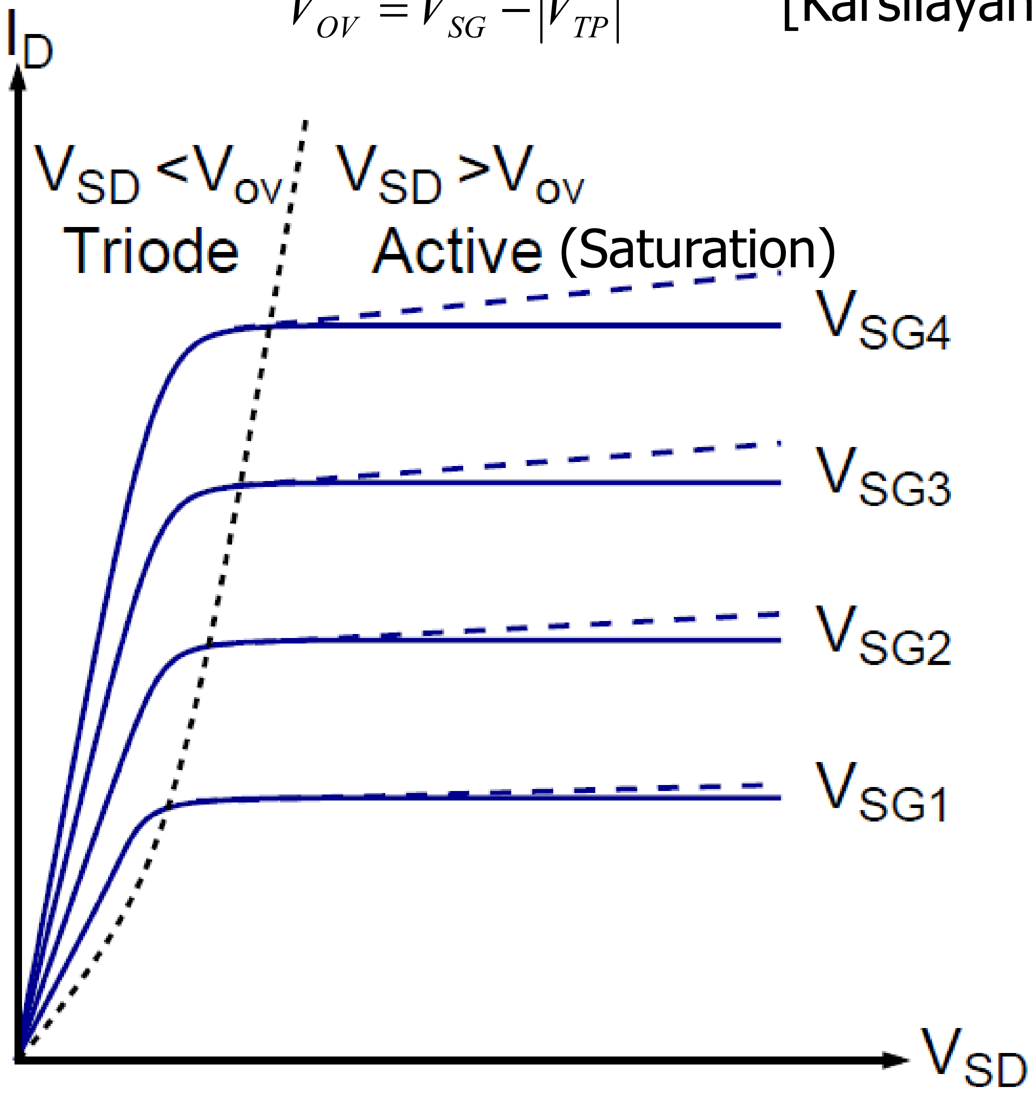
	NMOS	**PMOS**
Linear:	$I_{DS} = \frac{W}{L}\mu_n C_{OX}\left(V_{GS} - V_{Tn} - 0.5V_{DS}\right)V_{DS}$	$I_{SD} = \frac{W}{L}\mu_p C_{OX}\left(V_{SG} - \lvert V_{Tp}\rvert - 0.5V_{SD}\right)V_{SD}$
Saturation:	$I_{DS} = \frac{W}{2L}\mu_n C_{OX}\left(V_{GS} - V_{Tn}\right)^2$	$I_{SD} = \frac{W}{2L}\mu_p C_{OX}\left(V_{SG} - \lvert V_{Tp}\rvert\right)^2$

PMOS I_D – V_{SD} Characteristics



$V_{OV} = V_{SG} - |V_{TP}|$

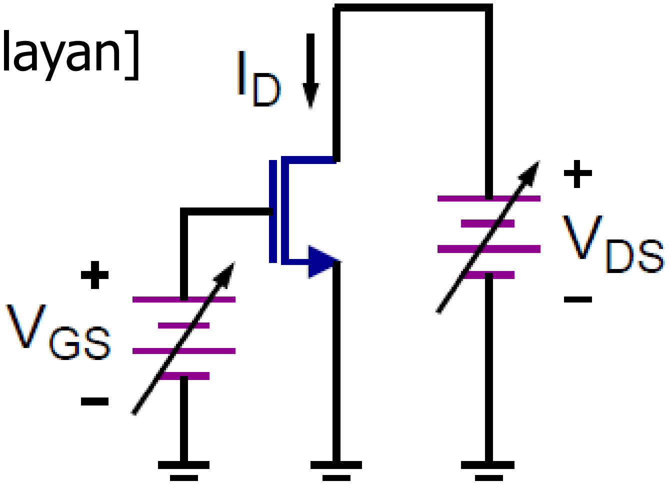
[Karsilayan]



NMOS DC Operation (w/ infinite r_{out})

Region	Bias Condition	I_{DS}
Cutoff	$V_{GS} < V_{TN}$	$I_{DS} = 0$
Triode (Linear)	$V_{GS} > V_{TN}, V_{DS} < V_{GS} - V_{TN}$	$I_{DS} = \mu_n C_{ox} \frac{W}{L}\left(V_{GS} - V_{TN} - \frac{V_{DS}}{2}\right)V_{DS}$
Saturation (Active)	$V_{GS} > V_{TN}, V_{DS} > V_{GS} - V_{TN}$	$I_{DS} = \frac{\mu_n C_{ox}}{2}\frac{W}{L}(V_{GS} - V_{TN})^2$

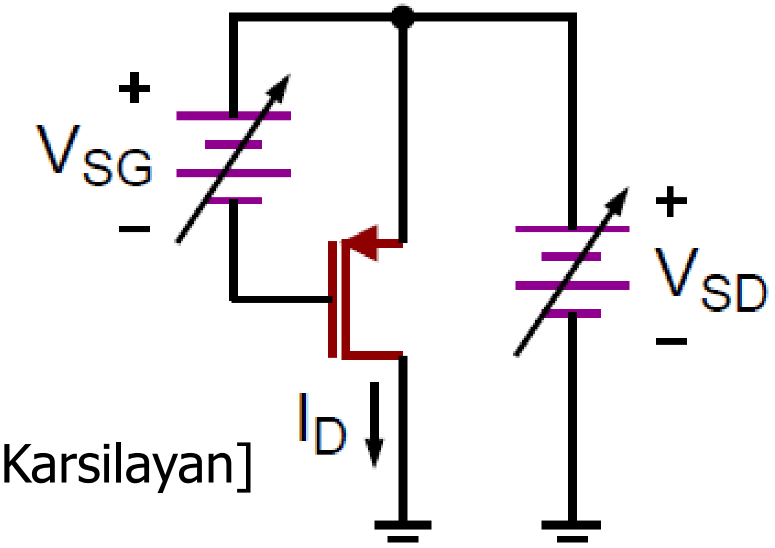
[Karsilayan]



- In transistor model, often combine $\mu_n C_{ox}$ term as a parameter KP_N with units A/V^2
- In lab, we combine $\mu_n C_{ox}(W/L)$ term as a parameter β_N with units A/V^2

PMOS DC Operation (w/ infinite r_{out})

Region	Bias Condition	I_{SD}
Cutoff	$V_{SG} < \lvert V_{TP} \rvert$	$I_{SD} = 0$
Triode (Linear)	$V_{SG} > \lvert V_{TP} \rvert, V_{SD} < V_{SG} - \lvert V_{TP} \rvert$	$I_{SD} = \mu_p C_{ox} \frac{W}{L}\left(V_{SG} - \lvert V_{TP} \rvert - \frac{V_{SD}}{2}\right)V_{SD}$
Saturation (Active)	$V_{SG} > \lvert V_{TP} \rvert, V_{SD} > V_{SG} - \lvert V_{TP} \rvert$	$I_{SD} = \frac{\mu_p C_{ox}}{2} \frac{W}{L}\left(V_{SG} - \lvert V_{TP} \rvert\right)^2$



[Karsilayan]

- In transistor model, often combine $\mu_p C_{ox}$ term as a parameter KP_P with units A/V^2
- In lab, we combine $\mu_p C_{ox}(W/L)$ term as a parameter β_P with units A/V^2