ECEN325: Electronics
Spring 2024

A Graphical Approach to BJT Amplifier Design

Sam Palermo

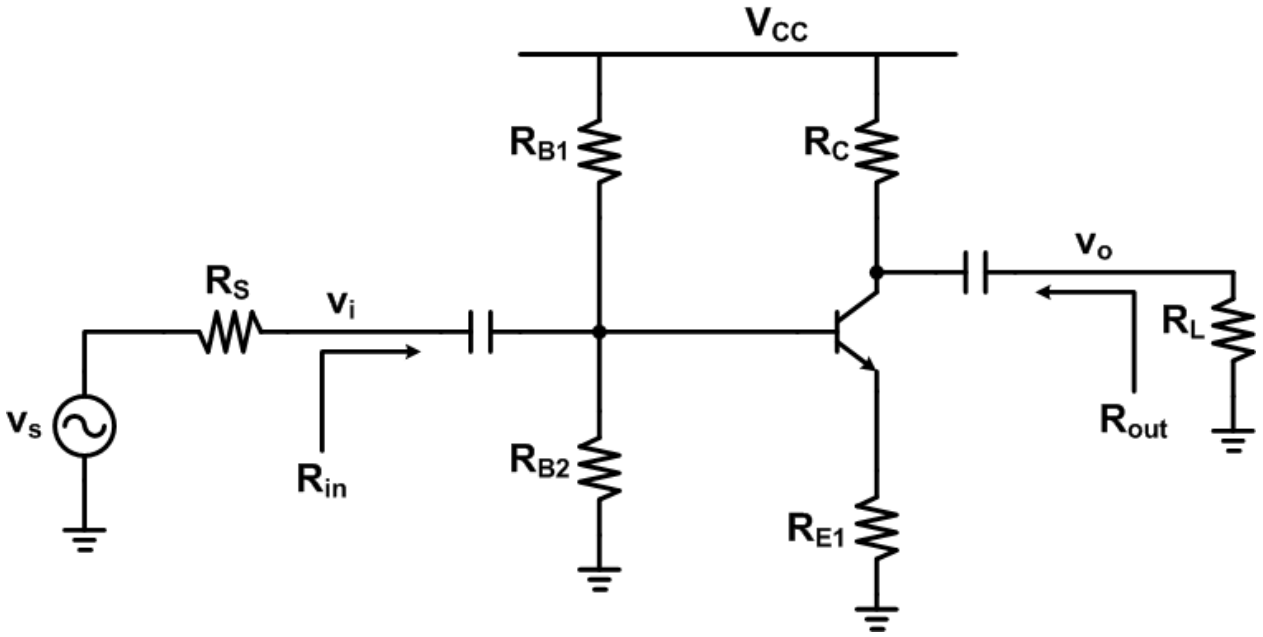
Analog & Mixed-Signal Center

Texas A&M University

Announcements

- HW 5 due Apr 2

Common Emitter Amp w/ Emitter Resistor



$$A_v = -\frac{g_m\left(R_C \| R_L\right)}{1+\frac{g_m R_{E1}}{\alpha}}$$

$$R_{in} = R_B \| \left(r_\pi + \left(\beta+1\right)R_{E1}\right)$$

$$R_{out} = R_C$$

Typical Design Specifications

- Loaded voltage gain, A_v
- Max output swing, v_{omax}
  - This must be satisfied at a given linearity (total harmonic distortion)
- Input and output resistance, R_{in} & R_{out}
- Power Supply, V_{CC}

How to set DC Biasing Conditions?

- In order to meet all design specifications, the DC biasing conditions (I_C, R_C) must be set appropriately

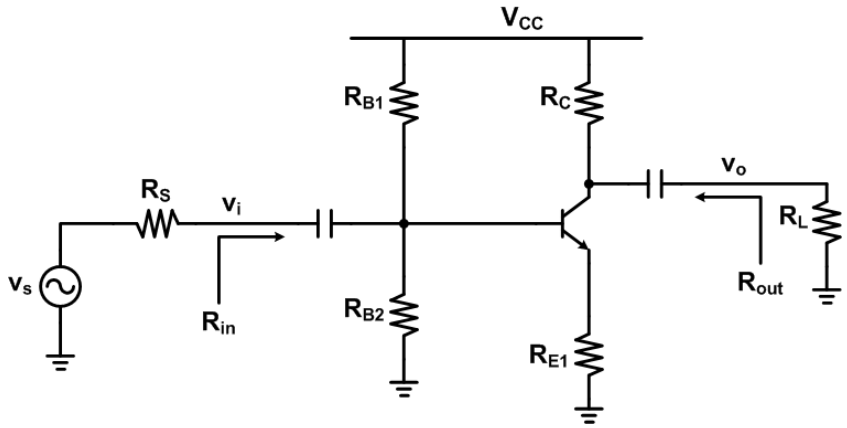
- Can transform design specifications into functions of I_C & R_C and graph them to find acceptable solution space

R_{in}, V_{CC}, & Neg. v_{omax} Specifications

- R_{in} Spec

$$R_{in} = R_B \left\| \left(r_\pi + (\beta + 1) R_{E1} \right) \approx \beta R_{E1} \right.$$

$$R_{E1} \approx \frac{R_{in}}{\beta}$$



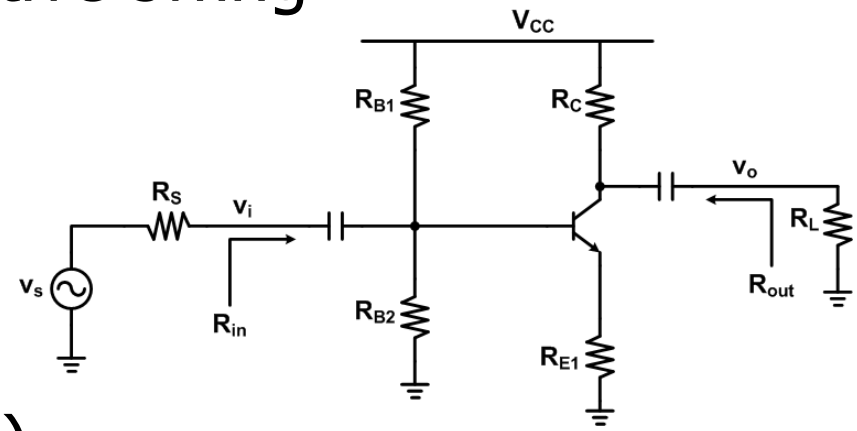
- Input resistance is primarily set by R_{E1}

R_{in}, V_{CC}, & Neg. v_{omax} Specifications

- Need a minimum V_{CE} to keep transistor in active mode with maximum negative swing

$$\text{Set } V_{CE\min} = 500mV$$

(w/ 200mV design margin)



- V_{CC} Spec (w/ max negative swing)

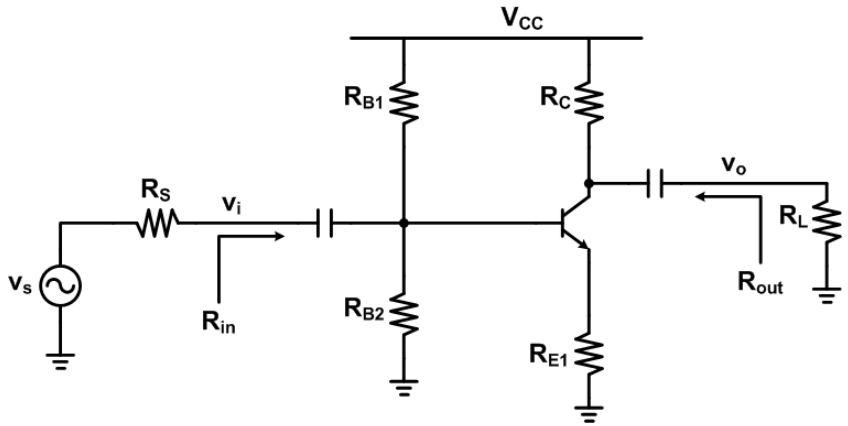
$$V_{CC} = \frac{I_C}{\alpha} R_{E1} + V_{CE\min} + v_{o\max} + I_C R_C$$

$$V_{CE\min} = V_{CC} - I_C R_C - v_{o\max} - \frac{I_C}{\alpha} R_{E1} \geq 500mV$$

R_{in}, V_{CC}, & Neg. v_{omax} Specifications

- Can solve for I_C

$$I_C \le \frac{V_{CC} - v_{o\max} - 0.5V}{R_C + \frac{R_{E1}}{\alpha}}$$



- Combining R_{in} spec $\quad R_{E1} \approx \frac{R_{in}}{\beta}$

$$I_C \le \frac{V_{CC} - v_{o\max} - 0.5V}{R_C + \frac{R_{in}}{\alpha\beta}}$$

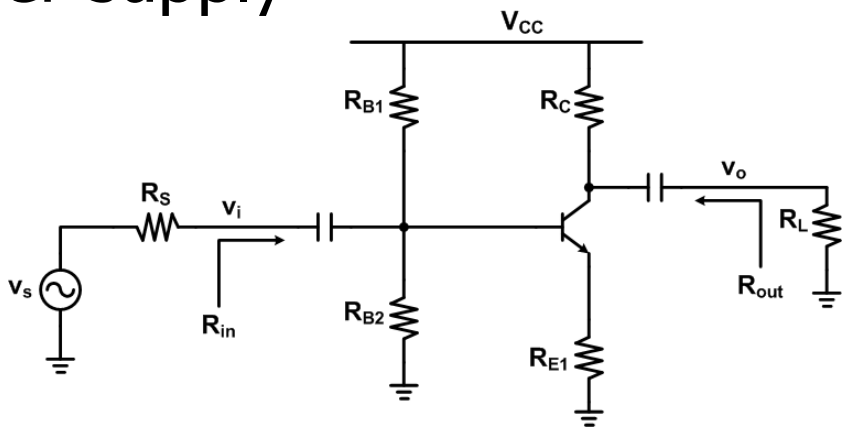
- Minimum negative AC Swing constraint sets an upper bound on I_C

Pos. v_{omax} Specification

- Need to insure with a positive swing that the output signal doesn't clip the power supply

$$V_{CC} - I_C R_C + v_{o\max} \le V_{CC}$$

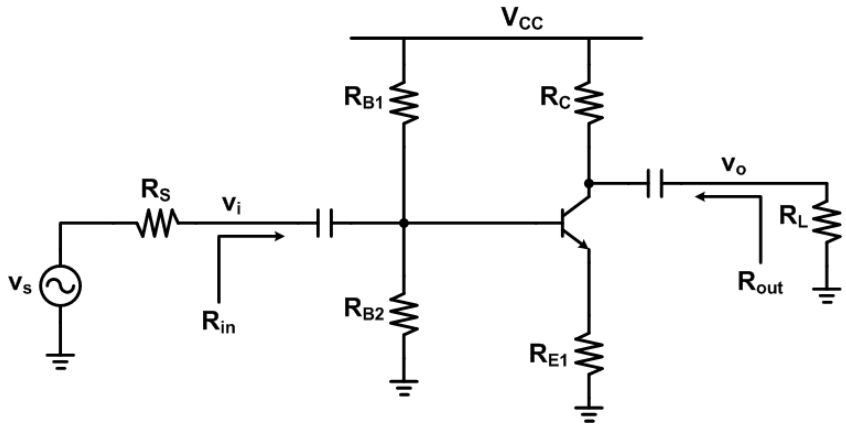
$$I_C \ge \frac{v_{o\max}}{R_C}$$



- Positive AC Swing constraint sets a lower bound on I_C
- Additional linearity constraint (harmonic distortion) generally sets a tighter bound

Gain Specification

$$|A_v| = \left|\frac{v_o}{v_i}\right| \le \frac{g_m\left(R_C \| R_L\right)}{1+\frac{g_m R_{E1}}{\alpha}} = \frac{\frac{I_C}{V_{th}}\left(R_C \| R_L\right)}{1+\left(\frac{I_C}{V_{th}}\right)\frac{R_{E1}}{\alpha}}$$

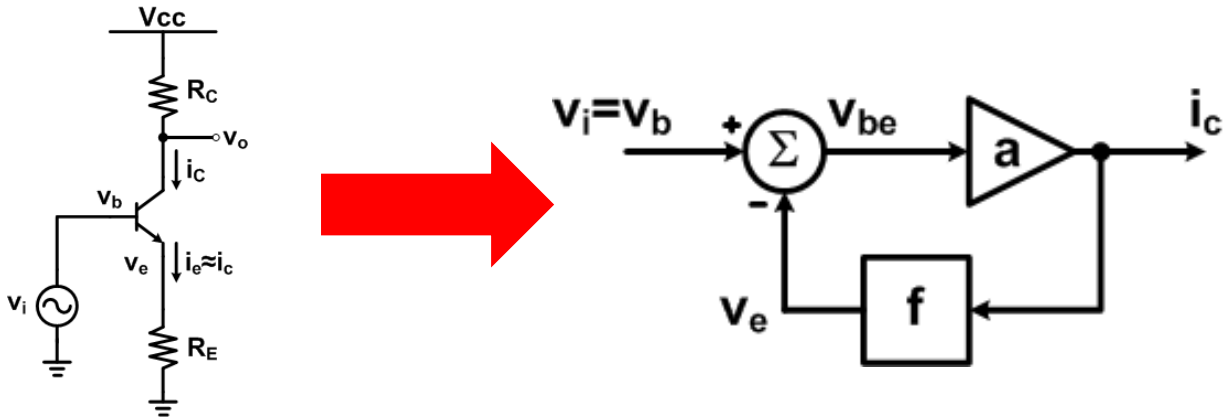


$$I_C \ge \frac{|A_v| V_{th}}{R_C \left\| R_L - \frac{|A_v| R_{E1}}{\alpha}\right.} = \frac{|A_v| V_{th}}{R_C \left\| R_L - \frac{|A_v| R_{in}}{\alpha\beta}\right.}$$

- Gain constraint sets a lower bound on I_C

Harmonic Distortion Specification

- Need a minimum amount of bias current to insure that the AC swing doesn't distort



Model a as a system which distorts

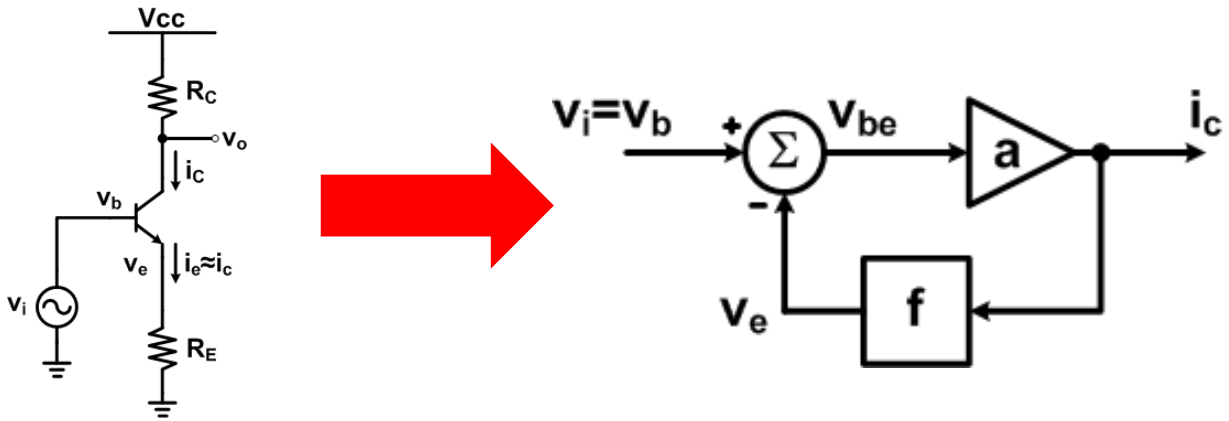
$$i_c = av_{be} = a_1 v_{be} + a_2 v_{be}^2 + a_3 v_{be}^3 + \ldots$$

where $a_1 = g_m, \quad a_2 = \frac{1}{2}\frac{I_{CQ}}{V_{th}^2}, \quad \ldots$

Here $v_{be} = v_b - v_e \approx v_b - fi_c$

where $f = R_E$

Harmonic Distortion Specification



We want to express i_c as a function of v_b because that is our input

$$i_c = bv_b = b_1 v_b + b_2 v_b^2 + b_3 v_b^3 + \ldots.$$

Can show that *

$$b_1 = \frac{g_m}{1 + g_m R_E}, \quad b_2 = \frac{1}{2} \frac{I_{CQ}}{V_{th}^2 (1 + g_m R_E)^3}, \quad \ldots$$

- For single-ended amplifiers with low-distortion, HD2 will dominate the distortion terms

The second - order harmonic distortion is

$$HD2 = \frac{1}{2} \frac{b_2}{b_1^2} i_{c\max} = \frac{1}{4} \left(\frac{1}{1 + g_m R_E} \right) \left(\frac{i_{c\max}}{I_{CQ}} \right)$$

Harmonic Distortion Specification

To satisfy a given HD2 specification

$$i_{c\max} \le 4HD2\left(1+g_m R_E\right)I_{CQ}$$

$$I_C \ge \frac{\frac{v_{o\max}}{R_C}}{4HD2\left(1+g_m R_E\right)} \approx \frac{\frac{v_{o\max}}{R_C}}{4HD2\left(\frac{I_C}{V_{th}}\right)R_E}$$

$$I_C \ge \frac{1}{2}\sqrt{\frac{V_{th}v_{o\max}}{R_C R_E HD2}}$$

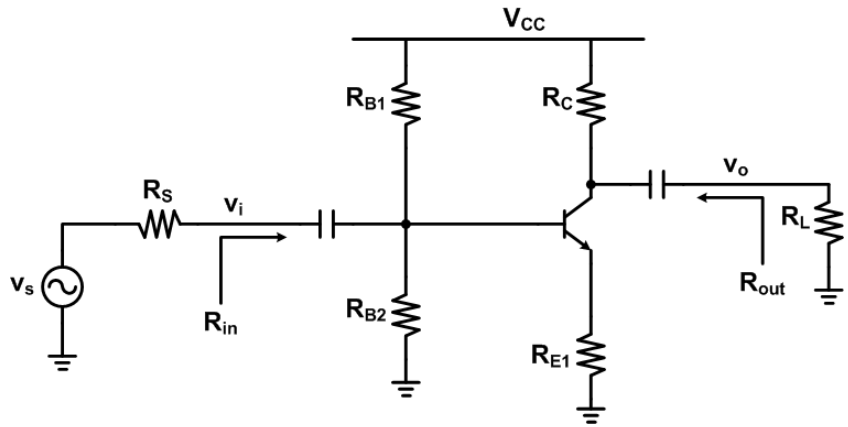
Using $R_E \approx \frac{R_{in}}{\beta}$

$$\boxed{I_C \ge \frac{1}{2}\sqrt{\frac{V_{th}v_{o\max}\beta}{R_C R_{in} HD2}}}$$

- HD2 will dominate, but is not the only distortion term
- For a -30dB THD, perhaps set HD2 to -40dB or (0.01)

Output Resistance Specification

- Neglecting transistor output resistance, R_{out} is determined by RC



$$R_C \leq R_{out,spec}$$

Key CE Amp Design Equation Summary

$$\text{Neg. Swing, Rin, } V_{CC}: \quad I_C \le \frac{V_{CC} - v_{o\max} - 0.5V}{R_C + \dfrac{R_{in}}{\alpha\beta}}$$

$$\text{Pos. Swing}: \quad I_C \ge \frac{v_{o\max}}{R_C}$$

$$\text{Gain}: \quad I_C \ge \frac{|A_v| V_{th}}{R_C \left\| R_L - \dfrac{|A_v| R_{in}}{\alpha\beta} \right.}$$

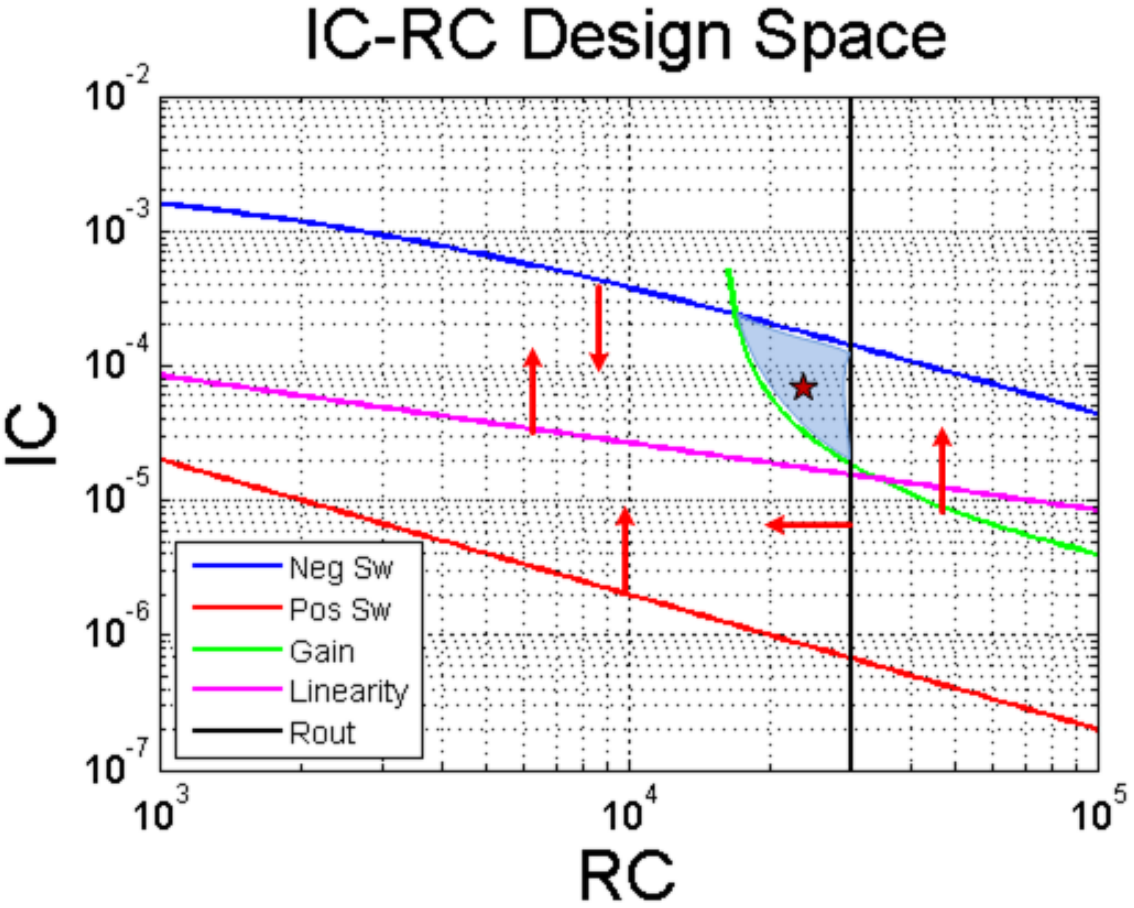
$$\text{Harmonic Distortion}: \quad I_C \ge \frac{1}{2}\sqrt{\frac{V_{th} v_{o\max} \beta}{R_C R_{in} HD2}}$$

$$\text{Output Resistance}: \quad R_C \le R_{out,spec}$$

Design Example - Specifications

- $|A_v| \geq |-8|$
- $R_L = 200k\Omega$
- $R_{in} \geq 200k\Omega$
- $R_{out} \leq 30k\Omega$
- $V_{omax} = 20mV_{pk}$ w/ THD $\leq$ -30dB
- $V_{CC} = 5V$

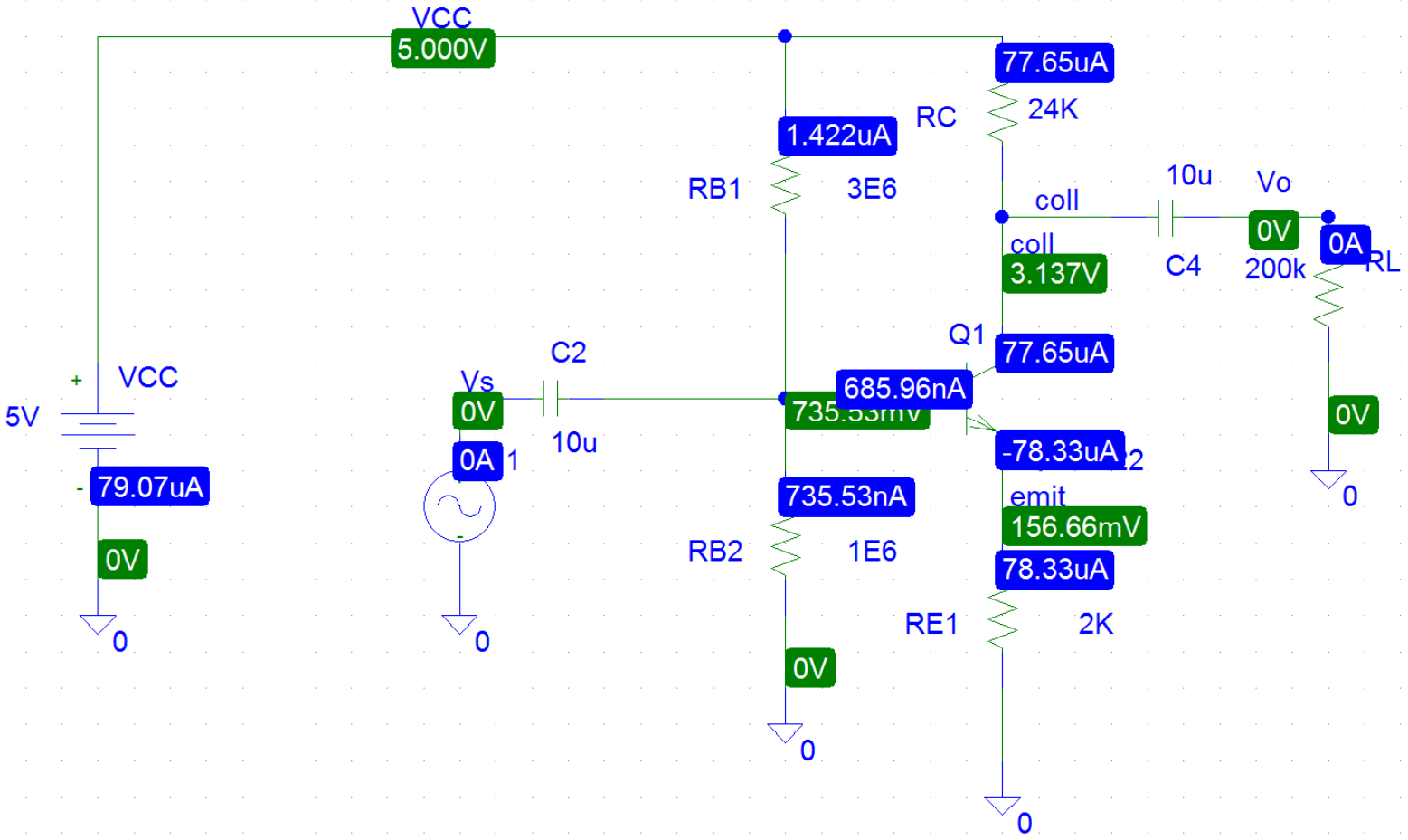
Design Equation Plots



Plots done with β=110 due to low current level necessary for high Rin

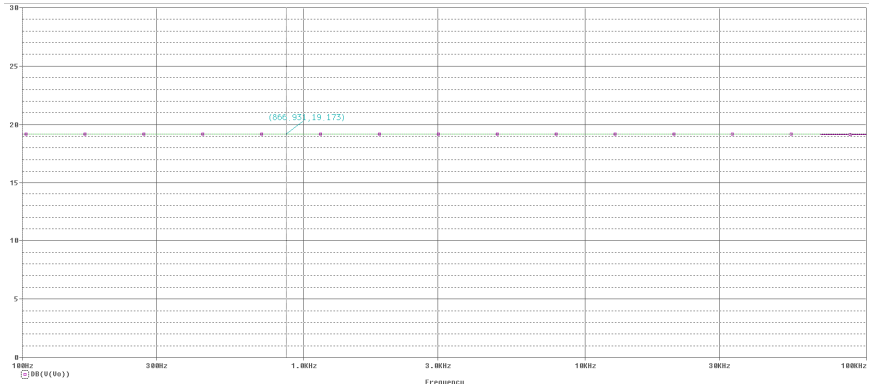
- Pick a design point in the middle for margin
- I_C=78μA, R_C=24kΩ

DC Operating Points

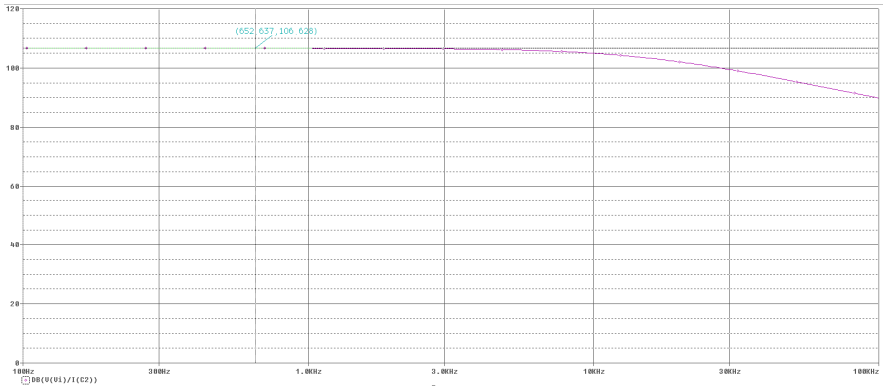


- DC bias points must be reasonable for the circuit to work as designed!

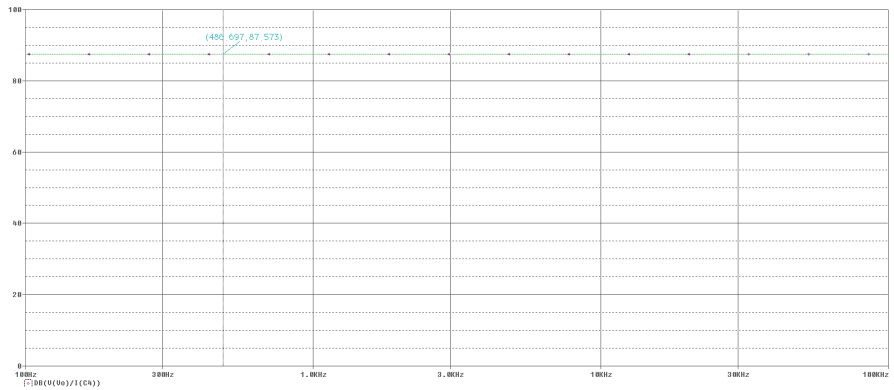
AC Gain, Rin, & Rout



- $|A_v| = 19.2dB = 9.12$



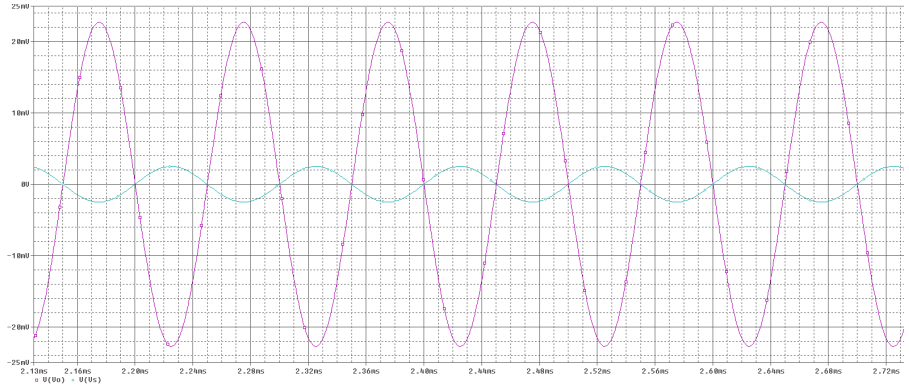
- $R_{in} = 106.6dB\Omega = 214k\Omega$



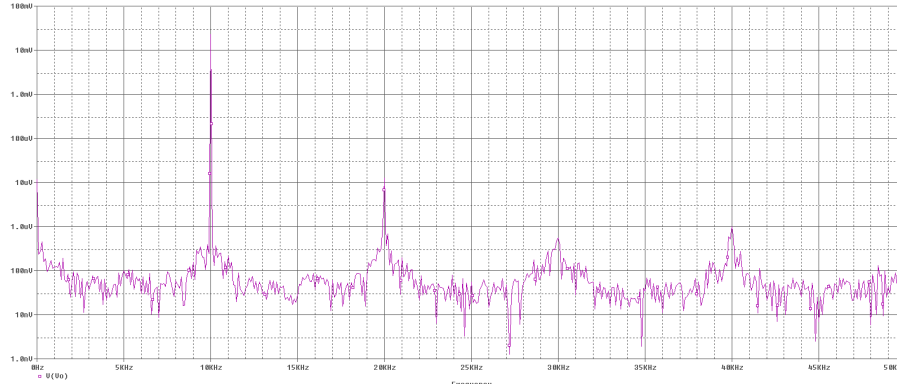
- $R_{out} = 87.7dB\Omega = 24.0k\Omega$

Transient & Distortion

- Output with swing > v_{omax}



- FFT of output signal



HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+04	2.273E-02	1.000E+00	1.795E+02	0.000E+00
2	2.000E+04	1.462E-05	6.433E-04	2.901E+01	-3.301E+02
3	3.000E+04	1.164E-05	5.121E-04	1.718E+02	-3.669E+02
4	4.000E+04	1.168E-05	5.139E-04	2.415E+01	-6.940E+02
5	5.000E+04	1.084E-05	4.771E-04	-1.235E+02	-1.021E+03

TOTAL HARMONIC DISTORTION = 1.080592E-01 PERCENT
This is equal to a THD of -59.3dB.

Fourier/THD Simulation in Multisim

1.8 Total Harmonic Distortion (Fourier Simulation)

- Click on "Select Active Analysis" in Fig. 3, then click on "Fourier" (Fig. 7)

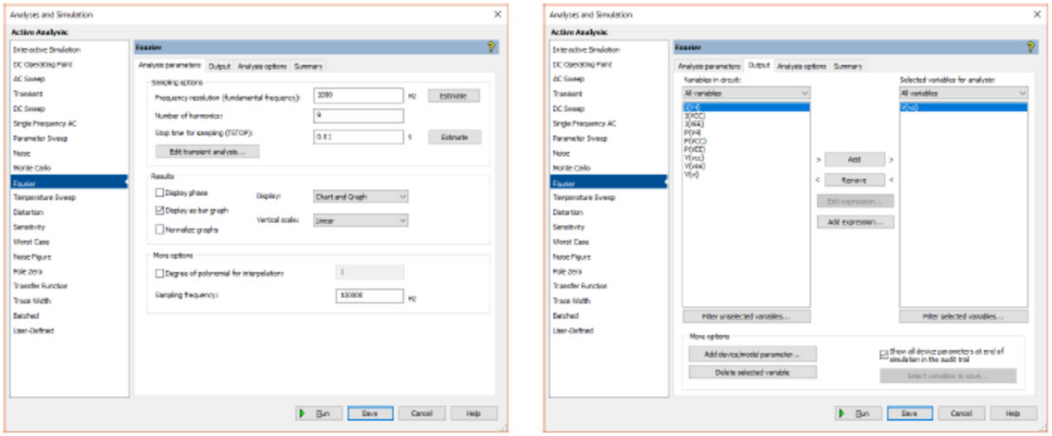


Figure 7: Fourier simulation setup

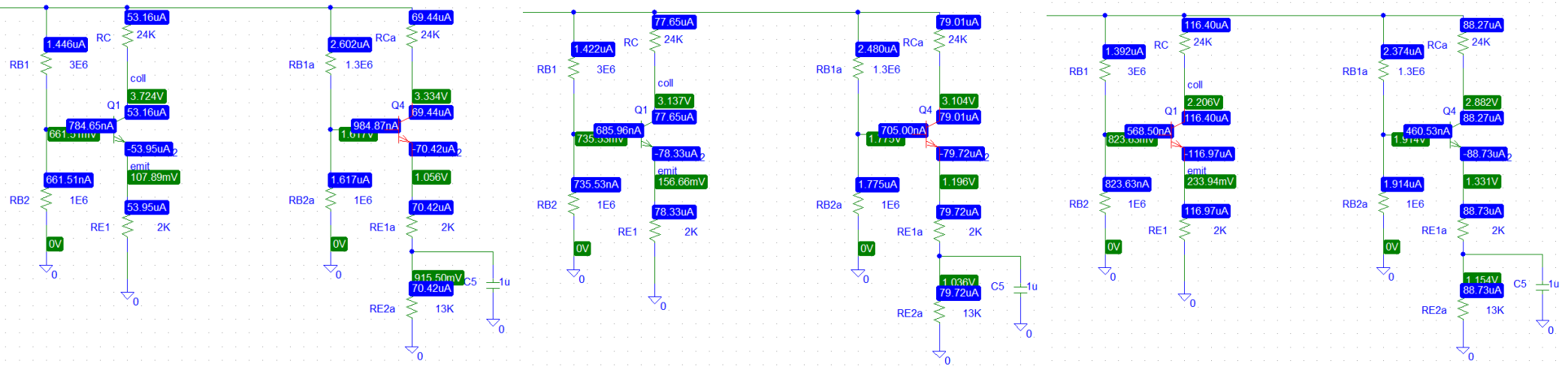
- Calculate $T = 1/f_i$, where f_i is the input frequency, and set $N = 9$
- On the "Analysis Parameters" tab, select:
  - Frequency resolution (fundamental frequency): f_i
  - Number of harmonics: N
  - Stop time for sampling (TSTOP): $10T$
- Click on "Edit transient analysis", select:
  - Start time (TSTART): 0
  - End time (TSTOP): $10T$
  - Check "Maximum time step (TMAX)" and enter the value: $\frac{T}{100(N+1)}$
- On the "Output" tab, click on "V(Vo)", then "Add", then "Save"
- Click on "Run" in Fig. 3

- https://people.engr.tamu.edu/spalermo/ecen325/MultiSim-AnalogDiscovery2-Keysight-Manual.pdf
- See page 5

Adding R_{E2} to Stabilize DC Biasing

- Adding RE2 can help to make the DC biasing less sensitive to the absolute transistor Beta value
  - Assume I want I_C~80μA
  - While the nominal β is 110, assume that it can vary from 70-200
  - What is the difference in designs with R_{E2}=0 and with 1V across R_{E2}?

β~70 **β~110** **β~200**



Beta	I_c (No R_{E2})	% Diff. from β=110	I_C (w/ 1V R_{E2})	% Diff. from β=110
70	53μA	-32.1%	69μA	-12.7%
110	78μA	N/A	79μA	N/A
200	116μA	48.7%	88μA	11.4%

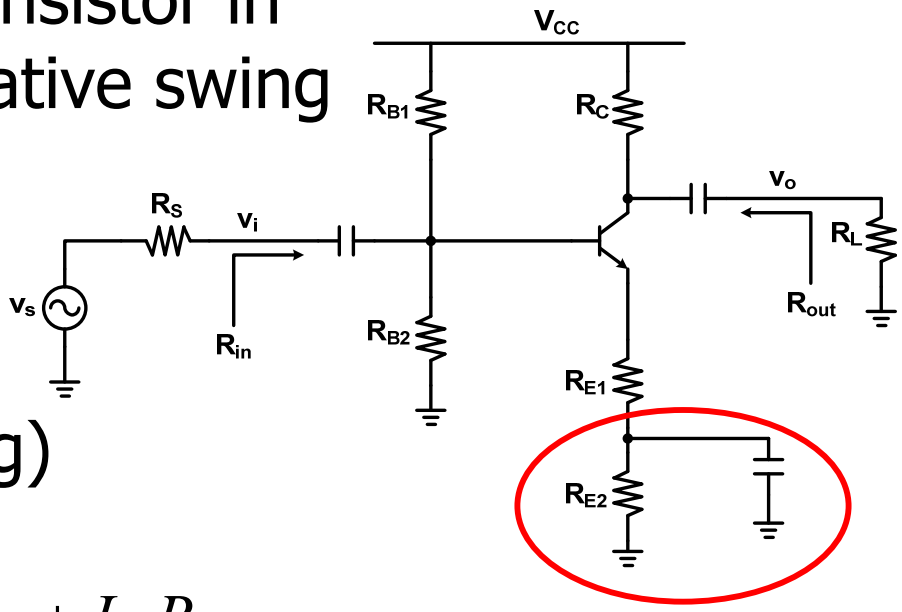
- What is the impact on the graphical design procedure?

R_{in}, V_{CC}, & Neg. v_{omax} Specs w/ R_{E2}

- The only equation impacted is the Neg. v_{omax}
- Need a minimum V_{CE} to keep transistor in active mode with maximum negative swing

$$\text{Set } V_{CE\min} = 500mV$$

$$(\text{w/ } 200\text{mV design margin})$$



- V_{CC} Spec (w/ max negative swing)

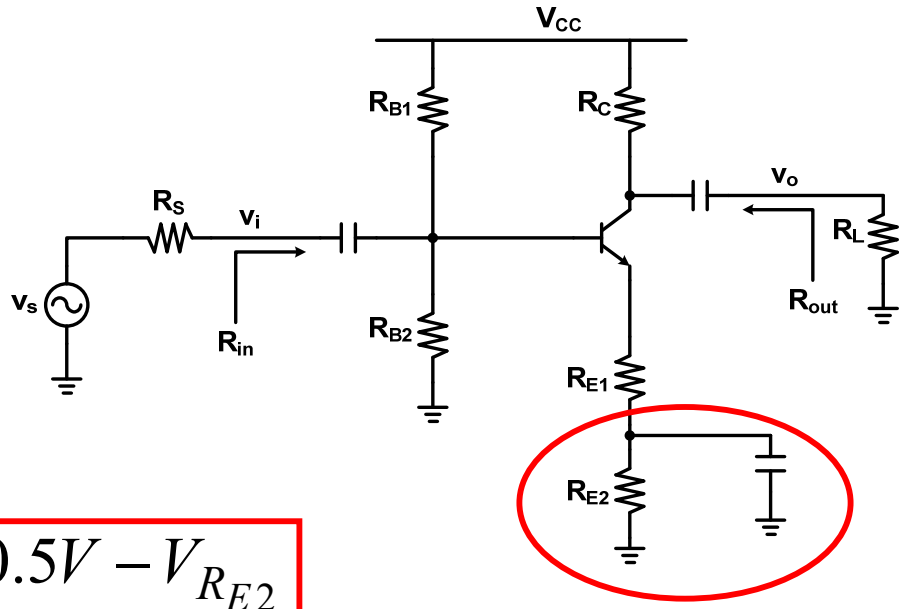
$$V_{CC} = \frac{I_C}{\alpha}(R_{E1} + R_{E2}) + V_{CE\min} + v_{o\max} + I_C R_C$$

$$V_{CE\min} = V_{CC} - I_C R_C - v_{o\max} - \frac{I_C}{\alpha} R_{E1} - I_E R_{E2} \geq 500mV$$

R_{in}, V_{CC}, & Neg. v_{omax} Specs w/ R_{E2}

- Can solve for I_C, assuming a V_{RE2} across R_{E2}

$$I_C \le \frac{V_{CC} - v_{o\max} - 0.5V - V_{R_{E2}}}{R_C + \frac{R_{E1}}{\alpha}}$$



- Combining R_{in} spec $\quad R_{E1} \approx \frac{R_{in}}{\beta}$

$$I_C \le \frac{V_{CC} - v_{o\max} - 0.5V - V_{R_{E2}}}{R_C + \frac{R_{in}}{\alpha\beta}}$$

- Minimum negative AC Swing constraint sets an upper bound on I_C which is reduced with R_{E2}

Key CE Amp Design w/ R_{E2} Eq. Summary

$$\text{Neg. Swing, Rin, } V_{CC}: \quad I_C \le \frac{V_{CC} - v_{o\max} - 0.5V - V_{R_{E2}}}{R_C + \frac{R_{in}}{\alpha\beta}}$$

Only Eq. which changed

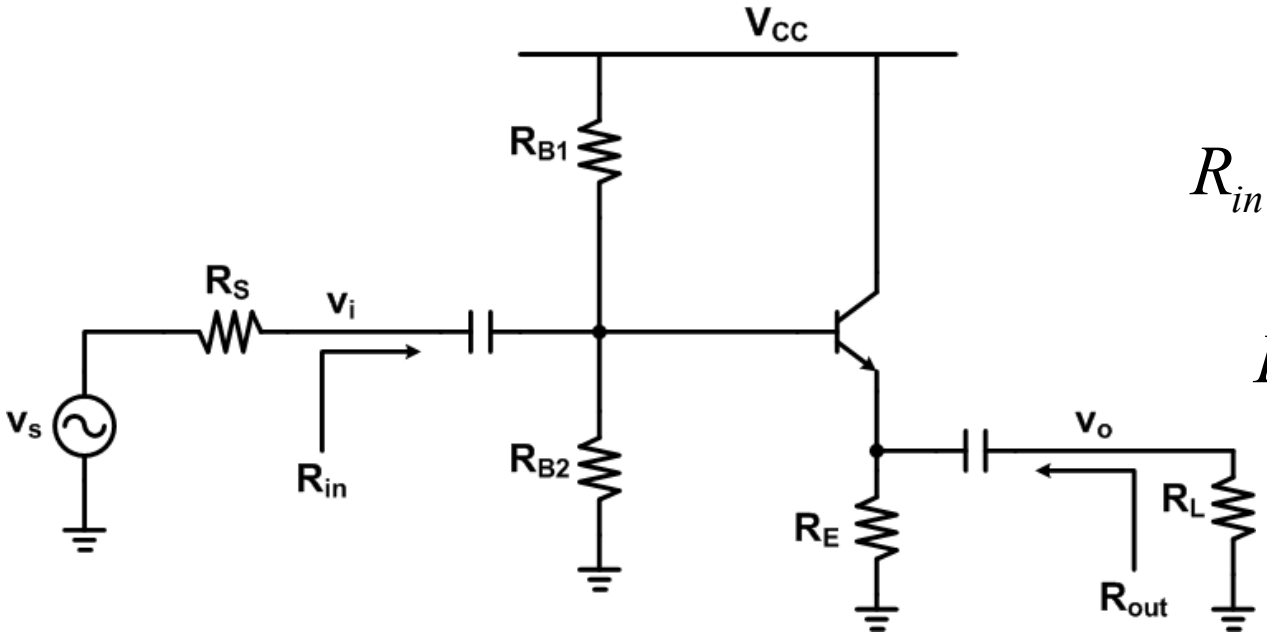
$$\text{Pos. Swing}: \quad I_C \ge \frac{v_{o\max}}{R_C}$$

$$\text{Gain}: \quad I_C \ge \frac{|A_v| V_{th}}{R_C \left\| R_L - \frac{|A_v| R_{in}}{\alpha\beta}\right.}$$

$$\text{Harmonic Distortion}: \quad I_C \ge \frac{1}{2}\sqrt{\frac{V_{th} v_{o\max} \beta}{R_C R_{in} HD2}}$$

$$\text{Output Resistance}: \quad R_C \le R_{out,spec}$$

Common Collector Amp



$$A_v = \frac{R_E \| R_L}{r_e + R_E \| R_L}$$

$$R_{in} = R_B \| \left(r_\pi + (\beta + 1) R_E \| R_L \right)$$

$$R_{out} = R_E \| \left[r_e + \frac{R_S \| R_B}{\beta + 1} \right]$$

Typical Design Specifications

- Loaded voltage gain, A_v
- Max output swing, v_{omax}
  - This must be satisfied at a given linearity (total harmonic distortion)
- Input and output resistance, R_{in} & R_{out}
  - If you know R_L, then R_{out} spec is somewhat redundant with A_v spec
- Power Supply, V_{CC}

How to set DC Biasing Conditions?

- In order to meet all design specifications, the DC biasing conditions (I_E, R_E) must be set appropriately

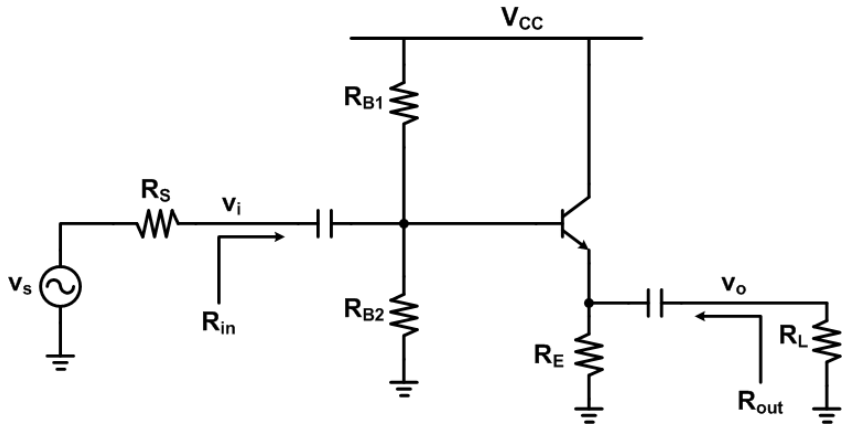
- Can transform design specifications into functions of I_E & R_E and graph them to find acceptable solution space

R_{in} Specification

- R_{in} Spec

$$R_{in} = R_B \left\| \left(r_\pi + (\beta + 1)(R_E \| R_L) \right) \approx \beta (R_E \| R_L) \right.$$

$$R_E \geq \left(\frac{\beta}{R_{in,spec}} - \frac{1}{R_L} \right)^{-1}$$



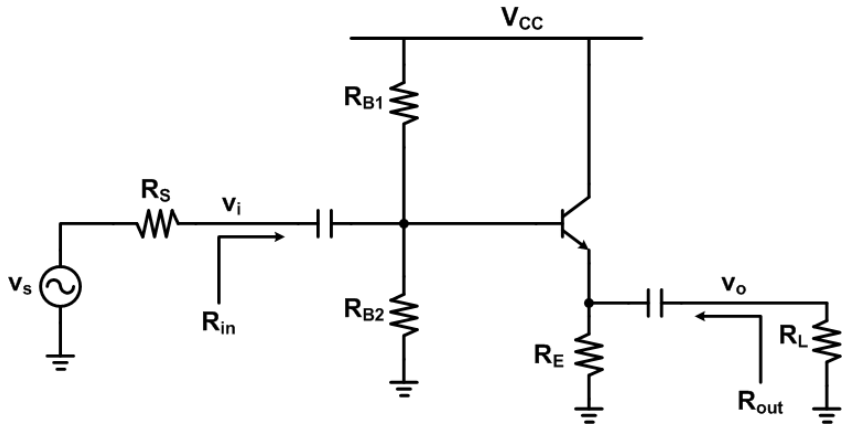
- Input resistance is primarily set by R_E and somewhat independent of I_E

Neg. v_{omax} Specification

- Need to insure with a negative swing that the output signal doesn't clip the power supply

$$I_E R_E - v_{o\max} \geq 0V$$

$$I_E \geq \frac{v_{o\max}}{R_E}$$



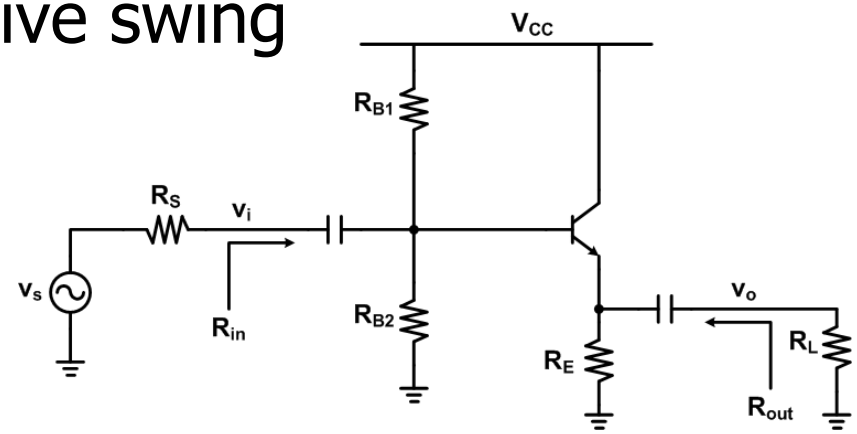
- Negative AC Swing constraint sets a lower bound on I_E
- Additional linearity constraint (harmonic distortion) generally sets a tighter bound

Pos. v_{omax} & V_{CC} Specifications

- Need a minimum V_{CE} to keep transistor in active mode with maximum positive swing

$$\text{Set } V_{CE\min} = 500mV$$

$$(\text{w/ } 200\text{mV design margin})$$



- V_{CC} Spec (w/ max positive swing)

$$V_{CC} = I_E R_E + v_{o\max} + V_{CE\min}$$

$$V_{CE\min} = V_{CC} - I_E R_E - v_{o\max} \geq 500mV$$

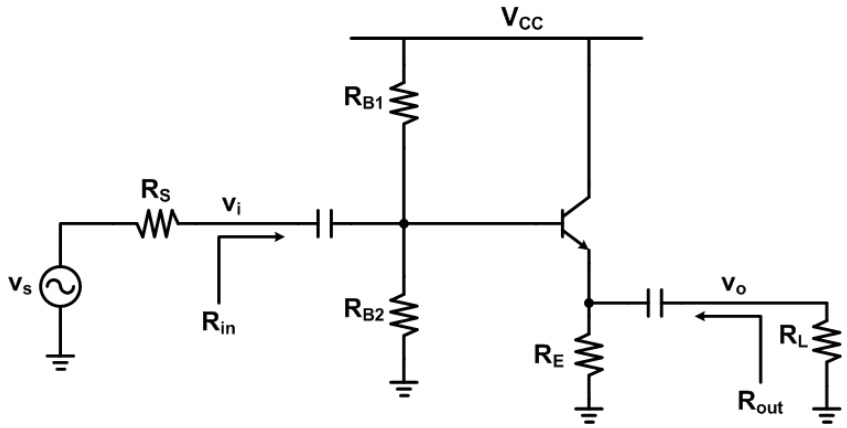
- Maximum positive AC swing constraint sets an upper bound on I_E

$$I_E \leq \frac{V_{CC} - v_{o\max} - 0.5V}{R_E}$$

Gain Specification

$$A_v = \frac{R_E \| R_L}{r_e + R_E \| R_L} = \frac{R_E \| R_L}{\frac{V_{th}}{I_E} + R_E \| R_L}$$

$$I_E \geq \frac{A_v V_{th}}{(R_E \| R_L)(1 - A_v)}$$



- Gain constraint sets a lower bound on I_E

Harmonic Distortion Specification

- Following a similar procedure as the Common-Emitter Amp, can relate the HD2 specification to the ratio of AC current i_c to I_{CQ}

$$i_c \le 4(HD2)\left(1+g_m\left(R_E \| R_L\right)\right)I_{CQ}$$

$$\text{Now, assuming a high } \beta \text{ or } \alpha \approx 1$$

$$i_e \le 4(HD2)\left(1+g_m\left(R_E \| R_L\right)\right)I_{EQ}$$

$$I_{EQ} \ge \frac{\frac{v_{o\max}}{R_E \| R_L}}{4(HD2)\left(1+g_m\left(R_E \| R_L\right)\right)} \approx \frac{\frac{v_{o\max}}{R_E \| R_L}}{4(HD2)\left(\frac{I_{EQ}}{V_{th}}\right)\left(R_E \| R_L\right)}$$

$$\boxed{I_{EQ} \ge \frac{1}{2\left(R_E \| R_L\right)}\sqrt{\frac{V_{th} v_{o\max}}{HD2}}}$$

- HD2 will dominate the distortion terms
- For a -30dB THD, perhaps set HD2 to -40dB or (0.01)

Key CC Amp Design Equation Summary

$$\text{Rin}: \quad R_E \geq \left(\frac{\beta}{R_{in,spec}} - \frac{1}{R_L} \right)^{-1}$$

$$\text{Neg. vomax}: \quad I_E \geq \frac{v_{o\max}}{R_E}$$

$$\text{Pos vomax, Vcc}: \quad I_E \leq \frac{V_{CC} - v_{o\max} - 0.5V}{R_E}$$

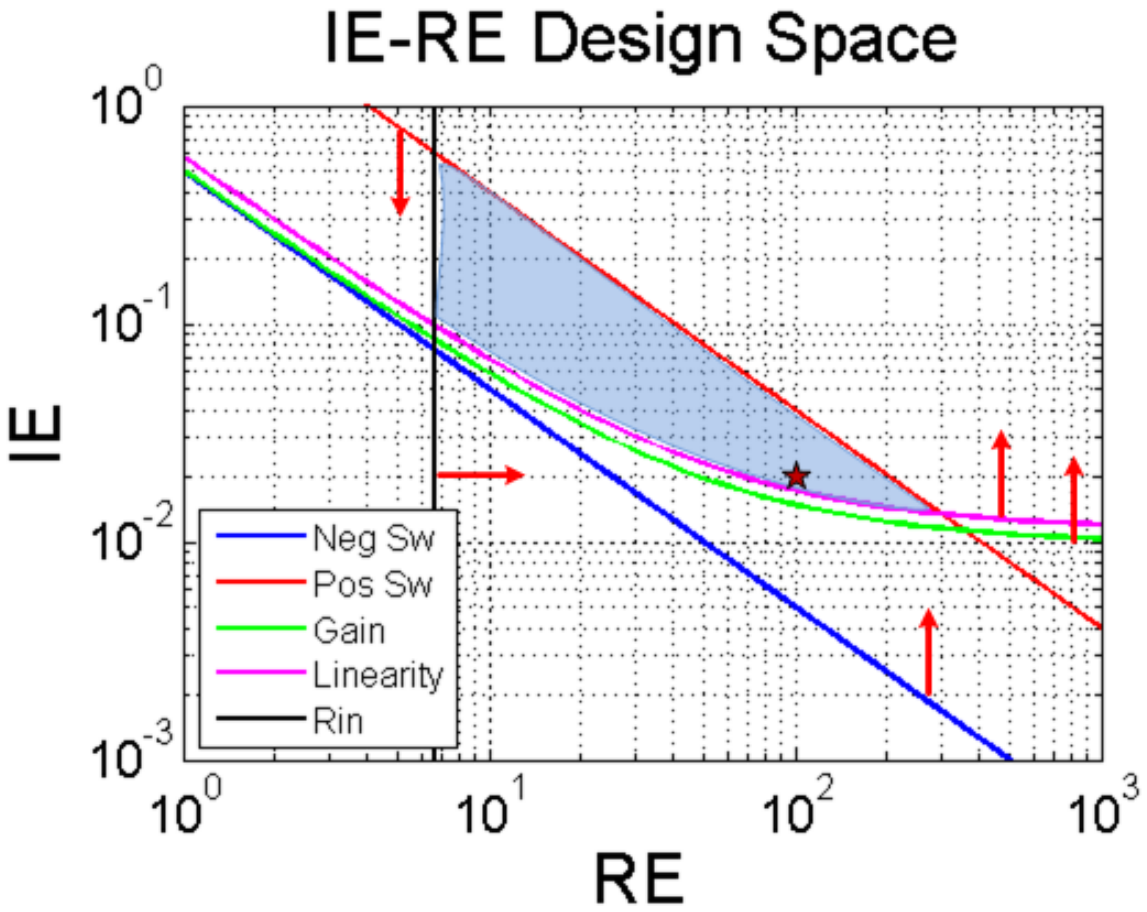
$$\text{Gain}: \quad I_E \geq \frac{A_v V_{th}}{\left(R_E \| R_L\right)\left(1 - A_v\right)}$$

$$\text{Harmonic Distortion}: \quad I_E \geq \frac{1}{2\left(R_E \| R_L\right)} \sqrt{\frac{V_{th} v_{o\max}}{HD2}}$$

Design Example - Specifications

- $A_v \geq 0.95$
- $R_{in} \geq 1k\Omega$
- $V_{omax} = 500mV_{pk}$ w/ THD $\leq$ -30dB
  - Here I set HD2=40dB or 0.01
- $V_{CC} = 5V$
- $R_L = 50\Omega$

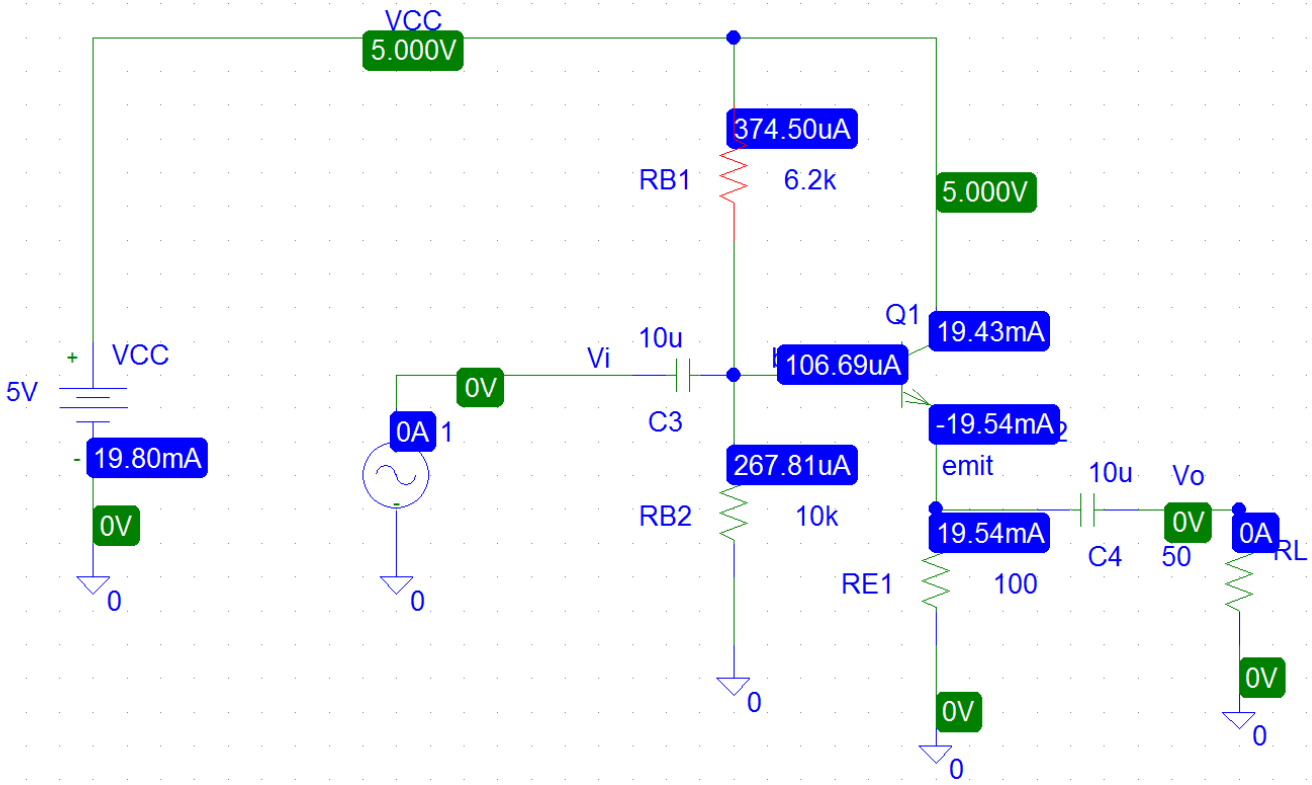
Design Equation Plots



Plots done with β=170 due to high current level

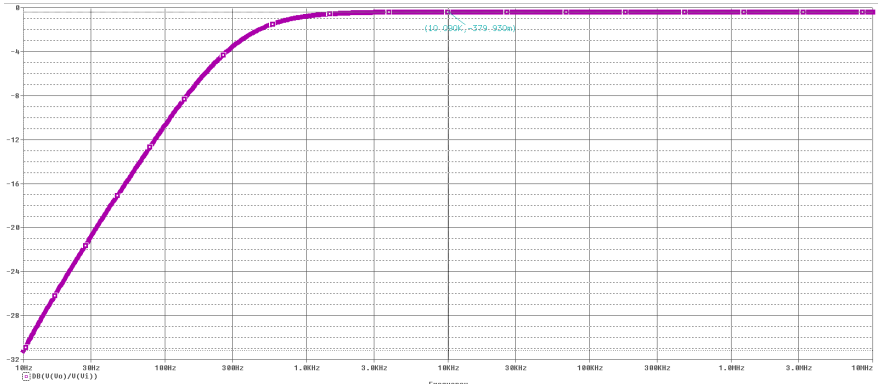
- Pick a low I_E design point to save power
- I_E=20mA, R_E=100Ω

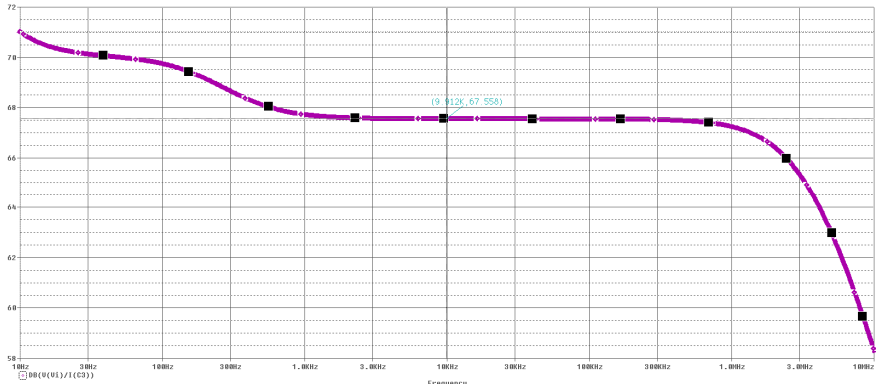
DC Operating Points



- DC bias points must be reasonable for the circuit to work as designed!

AC Gain & Rin

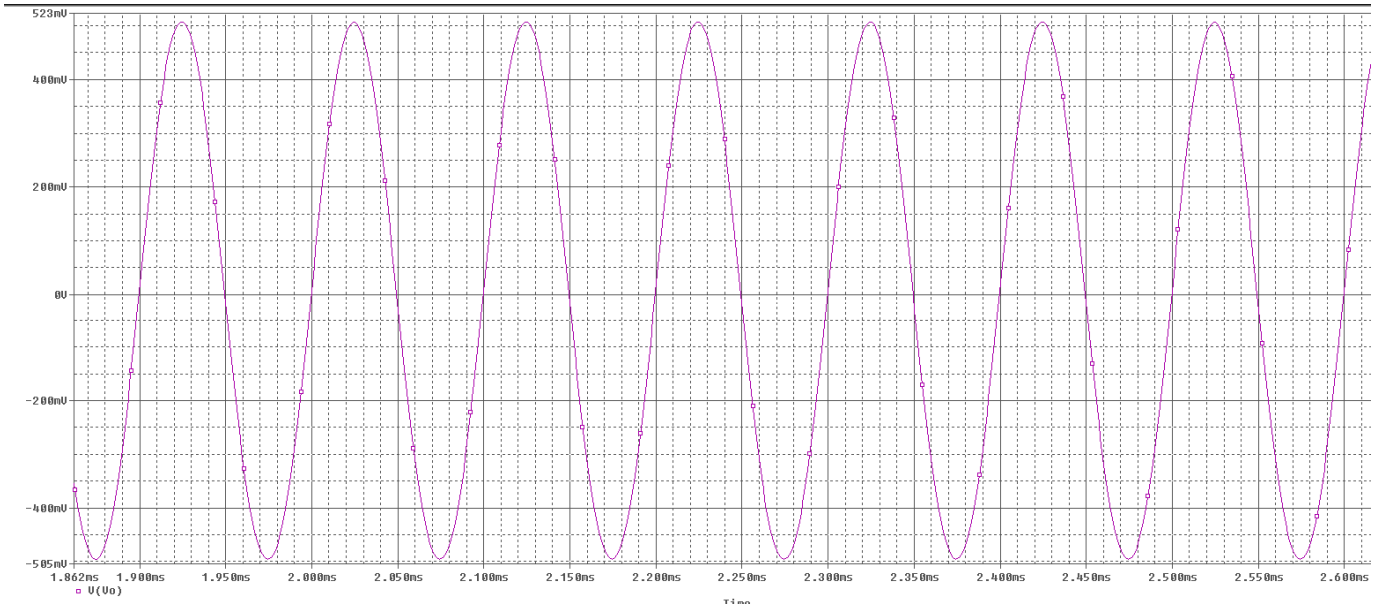




- $|A_v|$ = -0.38dB = 0.96
- R_{in} = 67.6dBΩ = 2.4kΩ

Transient & Distortion

- Output with swing > v_{omax}



HARMONIC NO	FREQUENCY (HZ)	FOURIER COMPONENT	NORMALIZED COMPONENT	PHASE (DEG)	NORMALIZED PHASE (DEG)
1	1.000E+04	5.032E-01	1.000E+00	1.770E+00	0.000E+00
2	2.000E+04	5.146E-03	1.023E-02	-8.968E+01	-9.322E+01
3	3.000E+04	1.798E-03	3.572E-03	2.109E+00	-3.200E+00
4	4.000E+04	4.937E-04	9.811E-04	1.251E+02	1.180E+02
5	5.000E+04	1.410E-04	2.801E-04	8.911E+01	8.027E+01

TOTAL HARMONIC DISTORTION = 1.088050E+00 PERCENT