Low-Power 8Gb/s Near-Threshold Serial Link Receivers Using Super-Harmonic Injection Locking in 65nm CMOS

Kangmin Hu[1], Tao Jiang[1], Sam Palermo[2] and Patrick Yin Chiang[1]
[1]Oregon State University, Corvallis, OR 97331
[2]Texas A&M University, College Station, TX 77843

***Abstract*- A testchip of 8Gb/s forwarded clock serial link receivers is presented. The receiver exploits a novel low-power super-harmonic injection-locked ring oscillator for symmetric multi-phase local clock generation and dekewing. Further power reduction is achieved by designing most the receiver circuits in the near-threshold region of 0.6V supply, with the exception of only the global clock buffer, test buffers and synthesized digital circuits at nominal 1V supply. At architectural level, 1:10 direct demultiplexing rate is chosen as a demonstration of achieving low supply operation by high-parallelism design. Fabricated in 65nm CMOS technology, two receiver prototypes are integrated in this testchip, one without and the other with front S/Hs. Including the amortized power of global clock distribution, they consume 1.3mW and 2mW respectively at 8Gb/s input data rate, which achieve the power efficiency of 0.163mW/Gb/s and 0.25mW/Gb/s. Measurement results show both receivers get BER < 10^{-12} across a 20-cm FR4 PCB channel.**

I. Introduction

Applications like many-core processor system require growing off-chip I/O bandwidth to enable continuous performance gains, elevating off-chip high-speed serial link power to one of the most critical issues in future VLSI systems. However, recent reported I/O power efficiency improves much slower than its increasing bandwidth [1]. As a result, I/O power is likely to limit the overall performance and thermal requirement of the processor system in the future if there is no significant improvement of its power efficiency.

The state-of-the-art low-power multi-Gb/s chip-to-chip transceivers [1], [2] have demonstrated the power efficiencies as low as nearly 1mW/Gb/s or about 0.5mW/Gb/s for receiver alone. These designs focus on reducing the clocking power by either sharing it within a bundle of links or using resonant-clock distribution. Relative to traditional phase interpolators, injection-locked oscillator (ILO) [3], [4] has been introduced as an energy-efficient technique for deskewing the clock phase position. In this paper, 8Gb/s serial link receivers improve upon a previous low-power receiver architecture [4] by leveraging additional mixed-signal circuit techniques including a super-harmonic injection-locked ring oscillator (super-harmonic ILO), lower operating supply voltage, and higher demultiplexing ratio, to achieve better power efficiency.

II. Receiver Implementation

Fig. 1 shows the architecture of the entire forwarded-clock receiver testchip. A half-rate clock source (4GHz) is forwarded and independently deskewed at each of the three data receivers, with the number of parallel receivers limited by the pad number, die area and driving strength of the clock buffer. Jitter of forwarded clock and that of the received data are correlated since they are from the same clock source in the transmitter side. A half-rate forwarded clock is desired in order to match the Nyquist frequency of the data channels, such that the data channels experience a loss/phase delay similar to the clock channel for better jitter tracking between clock and data. Since the received data is recovered from correlated forwarded clock, jitter tolerance in the receiver side can be improved. The received forwarded clock drives an on-chip CML clock buffer with cross-coupled resistor feedback, in order to extend its bandwidth (Fig.2). Operating with 1V supply, this CML buffer delivers a large-swing 4GHz clock waveform across a 600-um long clock distribution to the respective super-harmonic ILO in each receiver for multi-

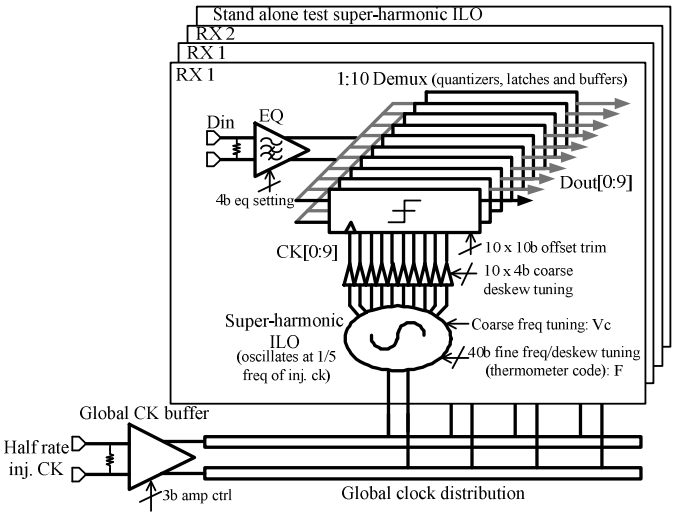


Fig. 1. Proposed receiver architecture.

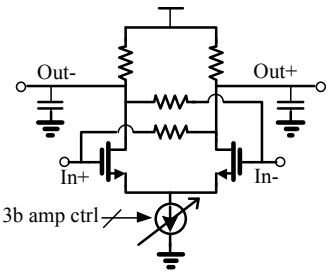


Fig. 2. Schematic of global clock buffer with parasitics.

978-1-4577-0223-5/11/$26.00 ©2011 IEEE

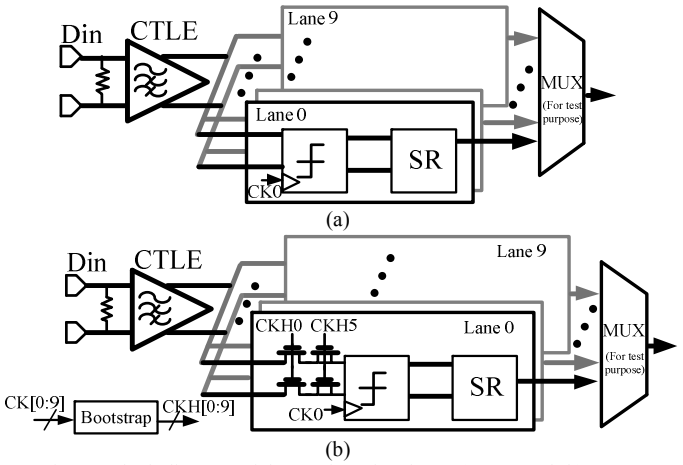


Fig. 3. Block diagram of the receiver data lane (a) RX1 and (b) RX2.

phase generation and deskewing.

For the data path, two prototypes (RX1 and RX2) are realized. As shown in Fig. 3(a), for RX1, the received the 8Gb/s data is first fed to a conventional source-degenerated continuous-time linear equalizer (CTLE) [6], and then directly sampled and demuxed by ten deskewed phases from super-harmonic ILO (to be discussed in detail in the following section) to ten-way 800Mb/s recovered data outputs. Finally they are muxed out for test purpose to save pads. In order to maximize the timing margin for the quantizers, sample-and-hold (S/H) circuits are employed in front of each quantizer in RX2, as shown in Fig. 3(b). Bootstrapped switches [7] are used in the S/H to get lower on-resistance and minimal signal-dependent distortion. Following the main switch, a conventional dummy switch is driven by complementary clock to minimize clock-feedthrough and charge injection.

In order to minimize power consumption, the super-harmonic ILO, CTLE, and quantizer circuits are designed to operate at 0.6V supply. A two-stage sense amplifier with only three stacks [8] is used as quantizer for low supply operation. While sub/near-threshold operation can enable significant improvement in power consumption and thus has become popularized for digital circuits, two disadvantages prevent its wide use for serial link applications: low operating frequency and worsened process variation. In order to address the low transistor speed, at the system level, a highly parallel architecture using 1:10 demultiplexing is chosen, such that sampling clock of each sub-lane quantizer can operate at a much lower frequency. To prevent potential process variation, extensive digital trimming bits are utilized throughout the entire receiver (i.e. quantizer offset calibration, oscillator frequency and phase deskew tuning). These calibrations are done at startup.

III. Design of Super-harmonic ILO

The schematic of the proposed near-threshold super-harmonic ILO is shown in Fig. 4. It generates ten evenly-spaced phases (P[0] - P[9]) using five stage differential delay cells, with a free-running frequency of around 800MHz. Negatively-skewed phase interpolation [9] is exploited to increase the ring oscillator frequency with a 0.6V supply. The

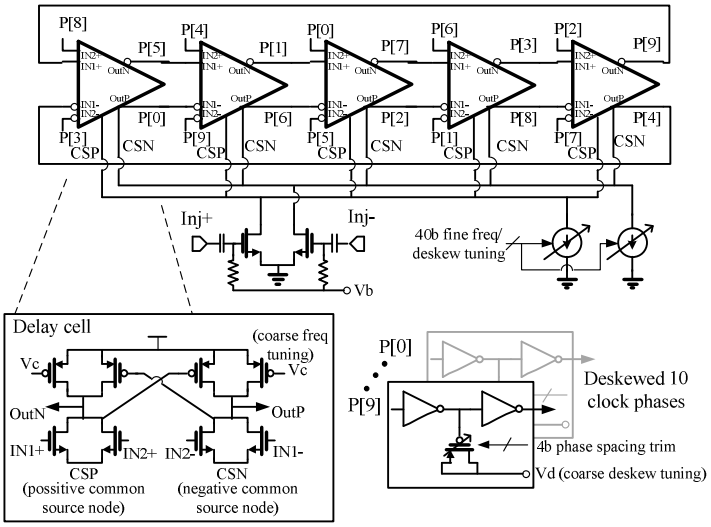


Fig. 4. Schematic of super-harmonic ILO.

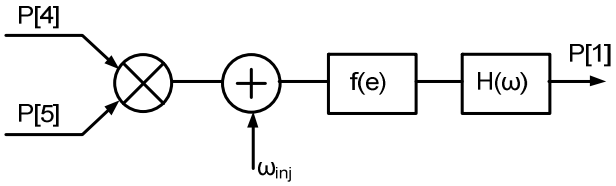


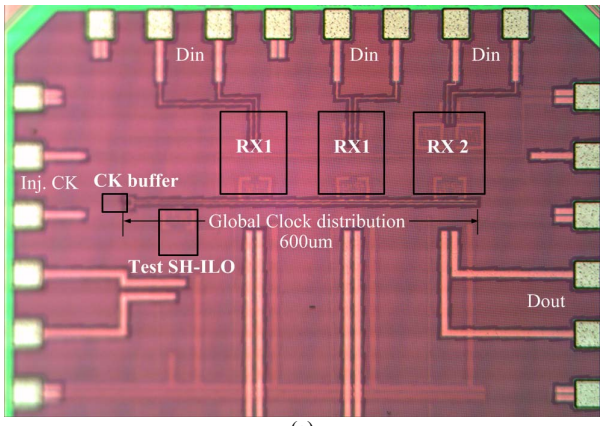
Fig. 5. Model of single stage of super-harmonic ILO.

ring incorporates three sources of frequency control: supply voltage, 40-b thermometer-encoded current-starving for fine tuning, and a DC-biased PMOS load (Vc) for coarse tuning.

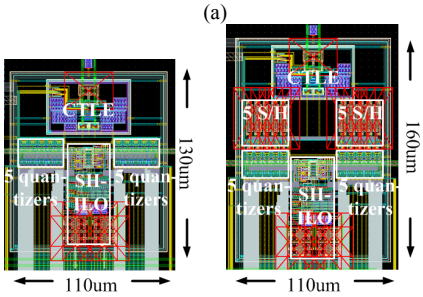
Since the differential half-rate (4GHz) clock source is now injected into the common source nodes (CSP and CSN) of the oscillator instead of directly loading any output phases, the proposed super-harmonic ILO relieves the problem of asymmetric injection and adjacent static phase error caused by different capacitance loading in 1st-harmonic injection-locking ring oscillators [4].

Following the principle of 1st-harmonic injection-locking [3-5], the frequency difference between the Nth sub-harmonic of the injection clock and the free-running frequency super-harmonic ILO will result in phase deskew when locked (N=5 for this design). Therefore, the 40-b fine frequency digital tuning bits can be used for deskew purposes. To further extend the deskew range to full UI, inversion-mode PMOS varactors are used as coarse deskew tuning (Vd) by adjusting the capacitance loading of the branches external to the oscillator (Fig. 4). Once Vd is set to roughly cover the phase difference between clock and data, digital controlled fine tuning will adjust to further deskew the phase.

Fig. 5 shows the simplified model of each stage of this super-harmonic ILO. Take 2nd stage as an example, clock phase P[4] and P[5] are first interpolated due to the negatively-skewed phase technique used here. Nonlinear function f(e) will generate multiple harmonic products from injection signal and the interpolated phase. They are then filtered by the transfer function H(ω) of the delay stage [10]. The single-sided locking range ω_{SL} can be estimated as



(a)



(b) (c)

Fig. 6. (a) Die photo. And layout screen capture of (b) RX1 and (c) RX2.

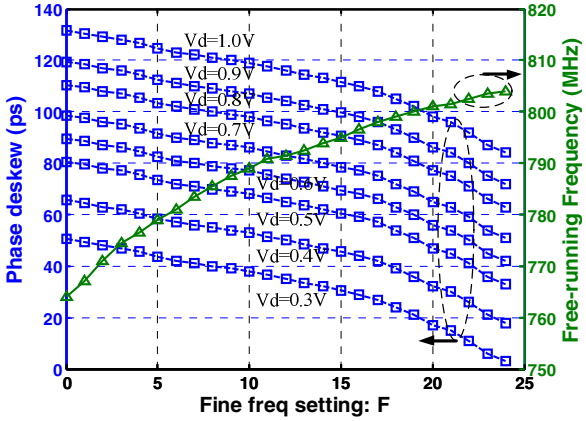


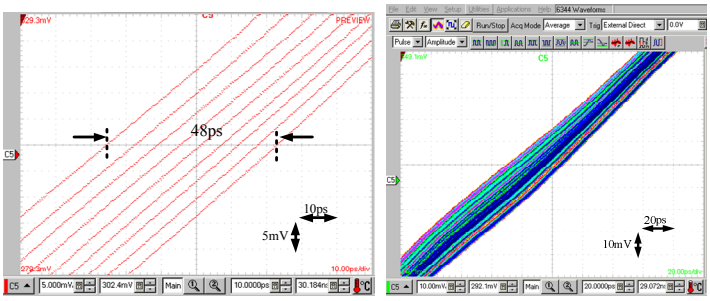
Fig. 7. Measured deskew range and free-running frequency of super-harmonic ILO across fine freq tuning.

$$\omega_{SL} = \eta \cdot \alpha_N \cdot \frac{2\omega_0}{N \sin(2\pi / N)} V_{inj} \quad (1)$$

where η is the injection efficientcy, α_N is the N-th harmonic coefficient. N is also the number of stages. ω_0 is the free-running frequency of the oscillator. And V_{inj} is the amplitude of the injection signal [11].

In order to compensate for any potential phase imbanlance due to layout mismatch, a 4-b switched capacitor bank on each phase is incorporated for individual phase trimming, with a measured resolution of 3-5ps. A scan-chain feedback loop runs at startup to adjust the phase spacing, using a histogram calibration algorithm [12]. The calibrated ten phases are then used to demux the input data.

IV. Experimental Results



(a) (b)

Fig. 8. Overlaid waveform of clock rising edge by changing fine tuning alone (a) with oscilloscope average mode on for clarity and (b) with grade color mode on.

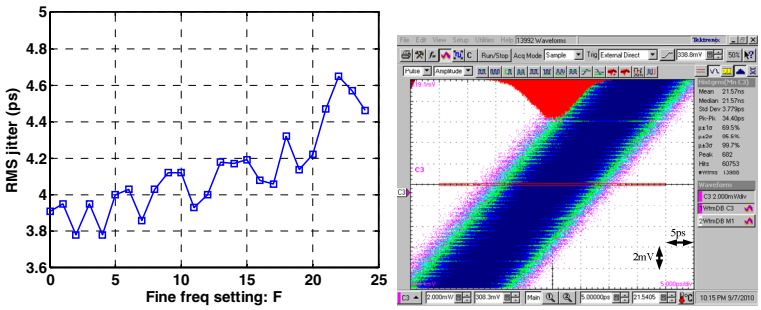


Fig. 9. (a) RMS jitter of super-harmonic ILO output across fine tuning settings, and (b) one of zoomed jitter measurement.

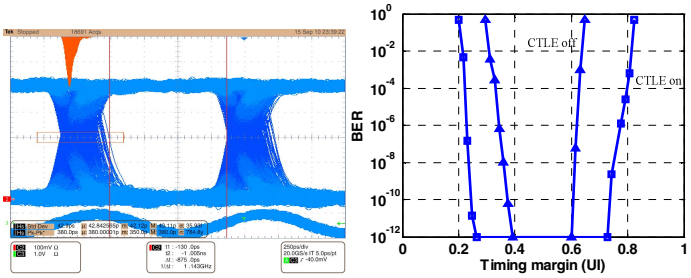
TABLE I. POWER BREAKDOWN

	Unit: mW	RX1	RX2
0.6V supply	CTLE	0.25	0.25
	10 S/Hs	N/A	0.55
	Quantizers, latches, local clock and data buffers, and others	0.4	0.52
	Super-harmonic ILO	0.24	0.25
1V supply	Amortized global clock buffer and bias	0.41	0.41
Total Power		1.3	1.98

The 1mm x 1mm testchip (Fig. 6) has been fabricated in a 65nm, 1V CMOS process. It contains three receivers (two RX1 and one RX2), the global clock distribution network, and a stand-alone super-harmonic ILO for test purposes.

First, the performance of super-harmonic ILO is examined. As shown in Fig. 7, by changing the fine tuning settings of the super-harmonic ILO alone, a 48ps deskew range with 1-3ps step resolution is achieved. Coarse deskew tuning, by changing the varactor control voltage Vd, provides another 82ps deskew, with enough margin between adjacent traces. Therefore the proposed receiver can cover the full UI (125ps for 8Gb/s) without dead zone. The deskewed clock edges are overlaid in Fig. 8.

When injecting a 4GHz clock with 800fs RMS jitter from signal generator, the super-harmonic ILO clock output exhibits jitter performance from 3.8ps RMS to 4.6ps RMS at 800MHz across the deskew settings, as shown in Fig. 9(a). Fig. 9(b) shows one of the jitter histogram measurements. The measured locking range (by changing the free-running frequency) is from 40 to 78MHz depending on the 3-b amplitude setting of the global clock buffer, which follows the fashion in Eq. (1). Due to the bandwidth limitations of the external signal generator, jitter modulation of the 4GHz clock source can only be introduced up to 40MHz. As no attenuation



(a) (b)

Fig. 10. RX1: (a) 800Mb/s 1:10 recovered data output (x=250ps/div, y=100mV/div), (b) BER bathtub curve at 8Gb/s over 20cm FR4.

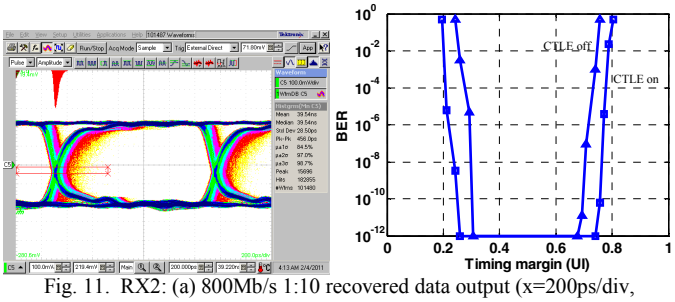


Fig. 11. RX2: (a) 800Mb/s 1:10 recovered data output (x=200ps/div, y=100mV/div), (b) BER bathtub curve at 8Gb/s over 20cm FR4.

Fig. 12 Channel response of a 20cm FR4 PCB trace.

is observed for sine-wave modulation up to this point, the bandwidth of the super-harmonic ILO jitter transfer is larger than 40MHz.

Fig. 10 and Fig. 11 show the measured recovered eye diagram of 1:10 de-multiplexed 800Mb/s data, and the measured bathtub curve at 8Gb/s with a 2^7-1 PRBS data input across a 20cm FR4 PCB trace (~-9.7dB channel loss @ 4GHz, as shown in Fig. 12) of the two receivers, with equalization of CTLE turning on or off. As expected, RX2 (the one with S/Hs) exhibits a little more timing margin.

Table I presents the power breakdown of the two receiver prototypes. RX2 consumes more power than RX1, due to its ten S/Hs and the additional loading of the local clock buffers. In total, RX1 and RX2 consume 1.3mW and 2mW respectively, which equals 0.163mW/Gb/s and 0.25mW/Gb/s at 8Gb/s.

The measured results are summarized and compared to previous designs in Table II.

V. Conclusion

In this paper, a receiver architecture with super-harmonic injection locked oscillator is proposed. The super-harmonic ILO introduces less imbalance to output phases than 1st-harmonic ILOs, and is also used to provide a full UI deskew. The receiver uses 1:10 demultiplexing ratio to ensure its operation under a low supply voltage of 0.6V. This choice of supply voltage, as well as the usage of super-harmonic ILO, greatly improves the power efficiency. Measurement result shows that one receiver prototype consumes 0.163mW/Gb/s at 8Gb/s. And the other receiver prototype with similar architecture and sample-and-hold before quantizer consumes 0.25mW/Gb/s at the same data rate. Both designs show significantly better energy efficiency compared to previous similar designs.

TABLE II. Comparision with Previous Works

	[6]	[4]	[5]	This work (RX1 and RX2)	
Data rate	6.25Gb/s	7.2Gb/s	7.4Gb/s	8Gb/s	
Architecture	Software CDR	Forwarded CK	Forwarded CK	Forwarded CK	
Phase deskew method	PLL with PI	Ring-ILO	ILO	Super-harmonic ILO	
Technology	90nm CMOS	90nm CMOS	65nm CMOS	65nm CMOS	
RX power	8.22mW	4.3mW	6.8mW	1.3mW	1.98mW
Power efficiency	1.31 mW/Gb/s	0.6 mW/Gb/s	0.92 mW/Gb/s	0.163 mW/Gb/s	0.25 mW/Gb/s
RX area	0.153mm^2	0.017mm^2	0.03mm^2	0.014mm^2	0.018mm^2

Acknowledgments

This work was partially supported by a donation from Intel and SRC grant 1836.060. The authors thank G. Balamurugan, F. O'Mahony and B. Casper of Intel for advice and use of measurement equipment. The authors also thank MOSIS and M. Flynn of U. Michigan for help with chip fabrication.

References

[1] F. O'Mahony *et al.*, "A 47x10Gb/s 1.4mW/Gb/s parallel interface in 45nm CMOS," *IEEE J. Solid-State Circuits*, vol. 45, no. 12, pp. 2828-2837, Dec. 2010.

[2] K. Fukuda *et al.*, "A 12.3mW 12.5Gb/s complete transceiver in 65nm CMOS," *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 368-369.

[3] F. O'Mahony *et al.*, "A 27Gb/s forwarded-clock I/O receiver using an injection-locked LC-DCO in 45nm CMOS," *IEEE ISSCC Dig. Tech. Papers*, Feb. 2008, pp.452-453.

[4] K. Hu *et al.*, "A 0.6mW/Gb/s, 6.4-7.2Gb/s serial link receiver using local injection-locked ring oscillators in 90nm CMOS", *IEEE J. Solid-State Circuits*, vol. 45, no. 4, pp. 899-908, Apr. 2010.

[5] M. Hossain and A. C. Carusone, "A 6.8mW 7.4Gb/s clock-forwarded receiver with up to 300MHz jitter tracking in 65nm CMOS," *IEEE ISSCC Dig. Tech. Papers*, Feb. 2010, pp. 158-159.

[6] J. Poulton *et al.*, "A 14-mW 6.25-Gb/s transceiver in 90-nm CMOS," *IEEE J. Solid-State Circuits*, vol. 42, no. 12, pp. 2745-2757, Dec. 2007.

[7] M. Dessouky and A. Kaiser, "Very low-voltage digital-audio ΔΣ modulator with 88-dB dynamic range using local switch bootstrapping," *IEEE J. Solid-State Circuits*, vol. 36, no. 3, pp. 349-355, Mar. 2001.

[8] D. Schinkel *et al.*, "A double-tail latch-type voltage sense amplifier with 18ps setup+hold time," in *IEEE ISSCC Dig. Tech. Papers*, Feb. 2007, pp. 314-315.

[9] S.-J. Lee *et al.*, "A novel high-speed ring oscillator for multiphase clock generation using negative skewed delay scheme," *IEEE J. Solid-State Circuits*, vol. 32, no. 2, pp. 289-291, Feb. 1997.

[10] J. Hu and B. Otis, "A 3uW, 400 MHz Divide-by-5 Injection-Locked Frequency Divider with 56% Lock Range in 90nm CMOS," *IEEE Radio Frequency Integrated Circuit (RFIC) Symposium*, June 2008, pp. 665-668.

[11] W.-Z. Chen and C.-L. Kuo, "18GHz and 7 GHz superharmonic injection-loced dividers in 0.25 um CMOS technology," *Proc. of ESSCIRC*, Sep. 2002, pp. 89-92.

[12] L. Lee, C.-K. K. Yang, "A sub-10ps multi-phase sampling system using redundancy," *IEEE ISSCC Dig. Tech. Papers*, Feb. 2005, pp. 510-511.