A Sub-Nyquist Rate Compressive Sensing Data Acquisition Front-End

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***Abstract*—This paper presents a sub-Nyquist rate data acquisition front-end based on compressive sensing theory. The front-end randomizes a sparse input signal by mixing it with pseudo-random number sequences, followed by analog-to-digital converter sampling at sub-Nyquist rate. The signal is then reconstructed using an L1-based optimization algorithm that exploits the signal sparsity to reconstruct the signal with high fidelity. The reconstruction is based on *a priori* signal model information, such as a multi-tone frequency-sparse model which matches the input signal frequency support. Wideband multi-tone test signals with 4% sparsity in 5~500 MHz band were used to experimentally verify the front-end performance. Single-tone and multi-tone tests show maximum signal to noise and distortion ratios of 40 dB and 30 dB, respectively, with an equivalent sampling rate of 1 GS/s. The analog front-end was fabricated in a 90 nm complementary metal–oxide–semiconductor process and consumes 55 mW. The front-end core occupies 0.93 mm^2.**

***Index Terms*—Analog-to-digital converters (ADCs), compressive sensing (CS), low-power circuit, sub-Nyquist ADC, wideband front-end.**

I. Introduction

THERE are well understood trade-offs between analog-to-digital converter (ADC) resolution, sampling speed, and power [1], with the ADC architecture determining the optimal power-speed-resolution region. Flash ADCs [36] achieve high sampling rates at low resolution (usually < 7 bits), pipeline ADCs [38], [44], [47] can achieve resolution < 14 bits when calibrated at a sampling rate up to few hundred MS/s, and successive approximation register architecture (SAR) [37], [45] and sigma-delta ADCs [39], [42], [46] can achieve high resolution (> 12 bits) at limited effective signal bandwidths up to around 100 MHz without time-interleaving. However, an ADC with both high resolution and high sampling rate is difficult to design for systems where power consumption is a significant constraint.

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A conventional receiver typically down converts the input signal to an intermediate frequency [41]. If the signal is multi-band, consisting of multiple sub-bands with known locations, then the input signal sub-bands can be individually selected for down-conversion to baseband. In this scenario, a single ADC is suitable for sampling the baseband signal.

However, development of innovative wideband receivers calls for ADCs with both high resolution and high sampling rate. For example, software defined radio (SDR) architectures [3] tend to place the ADC right after the antenna, and in cognitive radio (CR) [4], [5] the location of signals of interest are unknown. In these applications down-conversion is not easily applicable and it is desired to simultaneously observe a large section of spectrum. As the sampling rate of a traditional ADC needs to be at least the Nyquist rate in order to achieve alias free sampling [6], the required sampling rate could reach up to several gigahertz. The ADC speed is pushed towards the limit of the technology and both power consumption and jitter effects increase significantly. One way to lower the power consumption is to design a front-end that utilizes several ADCs to provide a combined sampling rate, such as time-interleaving structures [7]–[11] and multi-channel filter-bank approaches [12], [13], [40]. In these cases, the overall system is still operating at the Nyquist rate, so the total power reduction is limited.

An alternative to the Nyquist sampling theory is the recently proposed compressive sensing (CS) approach, such that when the signal is sparse the data acquisition system may work below the Nyquist rate to significantly lower the system complexity and save power [14]–[20]. In wireless communication systems, many channels are typically unoccupied and the signal is sparse in the frequency domain [21]. This makes it possible to exploit the CS theory in these systems and employ low speed ADCs to sample a wide spectrum.

This paper presents a CS front-end architecture developed in 90 nm complementary metal–oxide–semiconductor (CMOS). After a brief introduction to the CS theory, Section II introduces the front-end architecture which replaces the typical local oscillator (LO) signal by a pseudo-random number (PN) sequence generator (Fig. 1). The input signal is randomized by the PN sequence which spreads the spectrum over the entire bandwidth. Then, a simple integrator serves as linear projector and its output can be sampled at a fraction of the Nyquist rate. The sub-Nyquist sampled-data is processed by an L1-regularized optimization algorithm that relies on models for the sparse signal support and the random linear projector composed by the integration of the signal and the PN sequence. The design specifications of the specific implementation are detailed in Section III.

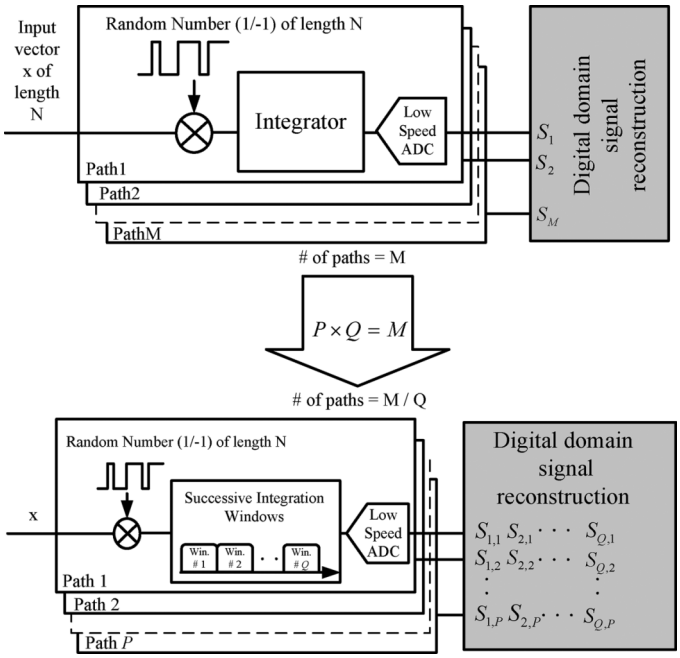

Fig. 1. Parallel circuit implementation of compressed sensing.

Section IV summarizes the CS front-end experimental results. A comparison between the CS system and conventional Nyquist rate ADCs is presented in Section V. Finally, Section VI concludes the paper.

II. Compressive Sensing Front-End Architecture

A. Compressive Sensing Fundamentals

Within the CS framework, a signal vector $x \in R^{N\times 1}$ is called K-sparse if it can be written in the form $x = \sum_{i=1}^{N} y_i \Psi_i$, or in the equivalent matrix form $x = \Psi y$, where $\Psi_i(t)$ is a known signal basis function and y_i is the corresponding basis coefficient. At any time only $K \ll N$ coefficients are nonzero and the signal sparsity is represented by the ratio K/N. For frequency-domain sparse signals, we can utilize the Fourier basis, i.e., $\Psi \in C^{N\times N}$ is the N-point discrete Fourier transform matrix.

With traditional sampling techniques sparse signals are first acquired at full Nyquist rate, and afterwards the signal is processed through the compression stage to obtain a sparse representation. In the approach of this paper, instead of employing full Nyquist sampling, we obtain the nonzero coefficients directly by taking only a small number of linear measurements of the signal at sub-Nyquist rate. Signal reconstruction from the sparse representation is achieved by using specially designed measurements and locating the sparsest solution out of the multiple solutions which satisfy the constraints presented below [14]–[20].

The measurement of x is performed by projecting it over a random basis Φ that is incoherent with Ψ, i.e., $s = \Phi\Psi y$, where $s \in R^{M\times 1}$ are the samples obtained at sub-Nyquist rate ($M < N$). Φ is called the *measurement matrix* and $V = \Phi\Psi$ is called the *reconstruction matrix*. For robust signal recovery, it is essential that the measurement matrix satisfies the restricted isometry property (RIP) [14], [15], [28]. A large number of random matrices have the RIP with high probability. For example, the random matrices whose entries are independent and identically distributed (i.i.d.) Gaussian, as well as i.i.d. Bernoulli (± 1). The Bernoulli random matrix is of particular interest because realizations can be easily generated with digital circuits.

To recover the original K-sparse signal from M incomplete measurements, a natural approach is to find the sparsest solution from the infinitely many solutions that satisfy the constraints $s = \Phi\Psi y$. Mathematically, this is accomplished by solving the following l_0 optimization problem:

$$\hat{y} = \arg\min \|y\|_0, \quad s.t. \quad s = \Phi\Psi y$$

where $\|\cdot\|_0$ is the l_0 norm. Although this optimization can recover a K-sparse signal from just $M = 2K$ compressive measurements, unfortunately it is a combinatorial NP-complete problem and computationally intractable [29], [30]. Moreover, the recovery is not stable in the presence of noise [31]. Fortunately, in practice the above problem can be relaxed to the following l_1 optimization through convex relaxation

$$\hat{y} = \arg\min \|y\|_1, \quad s.t. \quad s = \Phi\Psi y \tag{1}$$

where $\|\cdot\|_1$ is the l_1 norm. To solve this problem, there are many computationally tractable convex optimization or greedy algorithms available, such as linear programming (LP) [32], the Danzig Selector [33], orthogonal matching pursuit (OMP) [34], stagewise OMP [35], and others. With LP, the minimum required M is on the order of $K\log_2(N/K)$.

B. Front-End Circuit Architecture

The vector s may be generated using the first front-end shown at the top of Fig. 1. The signal is fed into M parallel paths, and in each path it is mixed with an independent binary PN sequence. These PN sequences form the rows of the matrix Φ. The integration yields the inner product of x and the PN sequence, which forms the vector s. In this scheme, the number of parallel paths is M, which is usually too big for practical circuit implementation. A more realistic solution is shown at the bottom of Fig. 1. The randomized signal after each mixer is equally divided into many segmented integration windows in the time domain for generating more samples in each path. Each path integrates Q segments of the randomized signal, yielding Q samples in each path. The overall number of required samples remains M [23] so the required number of parallel paths is $P = M/Q$.

The circuit implementation of a single path based on segmented integration is shown in Fig. 2 [22]. In the single parallel path, input signals are converted into signal current and mixed with the PN binary sequences (1 or -1) The mixer output current is then integrated over segmented integration windows, with the integration time, T_i, being the sampling window duration. For this prototype, the "sample" switches steer randomized current between two time-interleaved integrator branches that provide successive integrated samples. The transfer function of the integrator is a sinc-type low-pass filter (LPF), with the sampling rate ($1/T_i$) and the bandwidth of the LPF ($1/2T_i$) controlled by the frequency of the clock signals. Integrator outputs are then sampled and digitized for further processing in the digital domain.

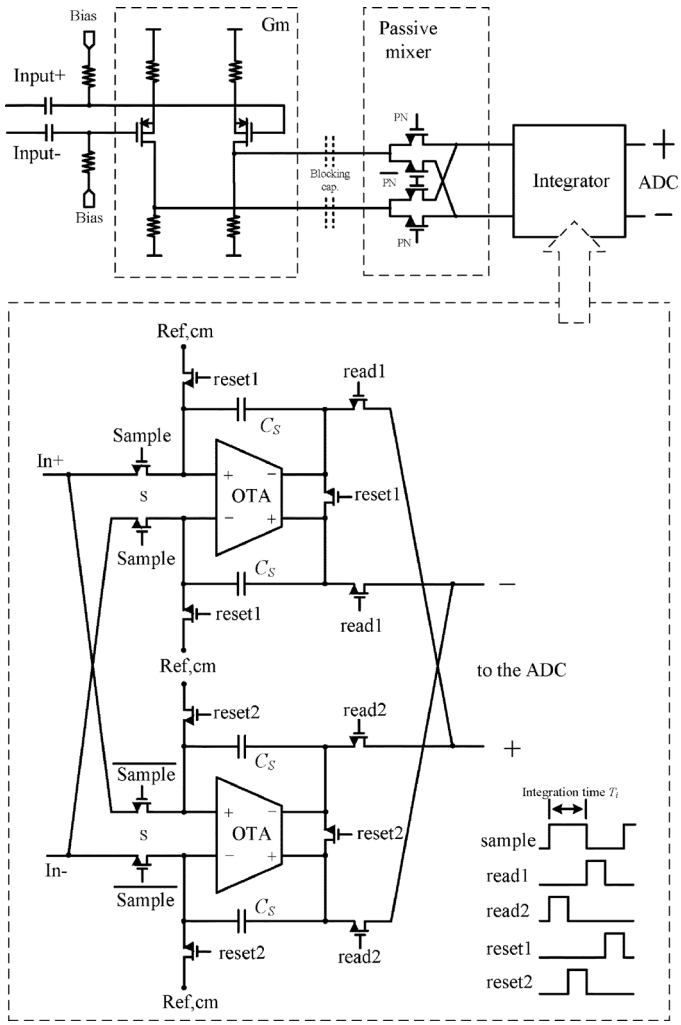

Fig. 2. Detailed CS front-end circuitry for a single path.

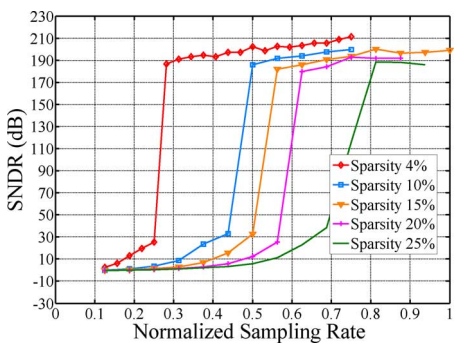

Fig. 3. Simulated reconstructed signal SNDR versus signal sparsity and sampling rate.

If circuit nonidealities are ignored, the CS algorithm can almost perfectly reconstruct a sparse signal with a sampling rate lower than the Nyquist rate. Employing the reconstruction algorithm reported in [23], the reconstructed signal quality is simulated and plotted in Fig. 3. In this simulation, all active sub-carriers have the same amplitude. The reconstructed signal quality is represented by its signal-to-noise and distortion ratio (SNDR). The system sampling rate is defined as $\mathrm{FS}_{\mathrm{patch}}P$, where $\mathrm{FS}_{\mathrm{path}}$ is the sampling rate of each single path and P is the number of paths. In Fig. 3, the system sampling rate is normalized with respect to the Nyquist rate.

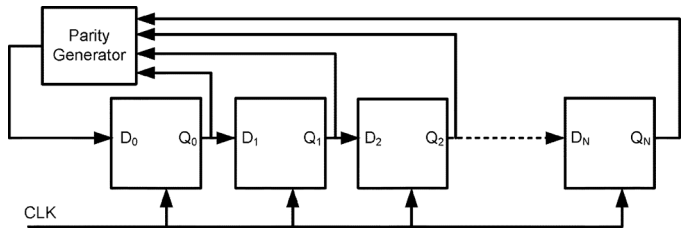

Fig. 4. Traditional PN generator.

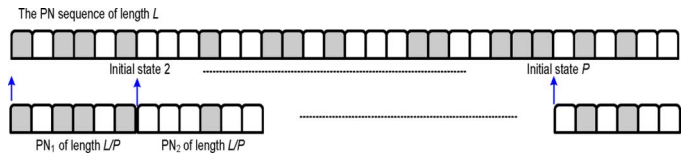

Fig. 5. Generation of the uncorrelated multi-path PN sequences.

CS has a natural performance threshold with respect to the sampling rate. The sampling rate has to be higher than that threshold otherwise the performance falls catastrophically.

Fig. 3 shows that when the sampling rate achieves a certain threshold depending on the signal sparsity, the CS system can obtain perfect signal quality ($\mathrm{SNDR} > 100$ dB). For example, when the sparsity is 4% the required system sampling rate is as low as 26% of the Nyquist rate. CS would require either *a priori* knowledge of the signal sparsity or a good way to estimate the signal sparsity using just a few signal samples.

C. PN Generator

In the above presented math model, the continuous analog input signal is represented by a discrete time vector x. This representation is alias-free only if the data rate of x, as well as the PN sequence, is higher than twice the bandwidth of the analog input. Thus, the speed of the PN generator circuit needs to be as high as the Nyquist rate. Throughout the paper f_{clk} is defined as the clock frequency of the PN generator, where f_{clk} needs to be set to at least the Nyquist rate of the input signal.

The PN generator is formed by a linear feedback shift register circuit, shown in Fig. 4. The outputs of the flip-flops are fed back to the first one through a parity generator, which yields output of "1" if an odd number of its inputs are at logic "1" and yields "0" if an even number of its inputs are at logic "1" [24]. The generated PN sequence only maintains randomness for a finite length and will repeat itself at the end of the sequence. With W as the number of the employed flip-flops, the maximum achievable PN length $L = 2^W - 1$ is obtained with proper selection of the parity generator's inputs. For example, when 11 flip-flops are used the optimum parity generator is simply a XOR gate, fed by the outputs of the eighth and the eleventh flip-flops. The length of the generated PN sequence is 2047. Multiple uncorrelated PN sequences can be obtained by splitting the PN sequence (Fig. 5). For example, eight identical PN generators with different initial states can simultaneously generate eight uncorrelated PN sequences of equal length 256 (Fig. 5). Note that one of the sequences is only of length 255 after split. Since

the randomness is maintained with either a "0" or "1" added to its end, this PN sequence of length 256 is formed by having the PN generator run for one more f_{clk} cycle.

III. Prototype Design Specifications

While the proposed system was designed to target a 1.5 GHz instantaneous signal bandwidth and 3 GS/s equivalent sampling rate [22], test equipment limitations allow for experimental characterization with only an instantaneous signal bandwidth of 500 MHz. A wideband multi-tone BPSK signal with 100 carriers allocated from 5 to 500 MHz at a 5 MHz frequency spacing between adjacent carriers serves as the input test signal. The sparsity of this input signal is around 4% at default, which means that there are at most four active tones in a given sampling interval.

For this experimental 500 MHz instantaneous bandwidth signal, the Nyquist rate is 1 GS/s and the default compressive sensing system sampling rate is set to be 36% of the Nyquist rate or 360 MS/s. According to Fig. 3, this sampling rate is above the threshold for successful signal reconstruction. In the proposed prototype eight parallel paths are employed, thus the sampling rate for a single path is 45 MHz. A single testing run lasts a duration of $1/5\ \mathrm{MHz} = 200\ \mathrm{ns}$, with each path yielding nine samples and an overall number of 72 samples per test run for the eight paths. The PN sequences' data rate is set to 1.25 GHz, which is somewhat above the minimum Nyquist rate, and the length of the eight uncorrelated PN sequences is $200\ \mathrm{ns} \times 1.25\ \mathrm{GHz} = 250$. Based on discussion in Section II-C, 8 PN generators composed of 11 flip-flops can be employed.

IV. Experimental Results

A. Signal Reconstruction and Calibration

In the optimization problem (1) $\Phi\psi^H$ is called the reconstruction matrix. In order to deal with practical system nonidealities such as sampling capacitor charge leakage and the distortion from aperture error of the PN sequence, a calibration step is required to measure the distorted reconstruction matrix. The calibration approach is depicted in Fig. 6, where y is the input signal spectrum and s contains the sampled measurements. Here, V represents the ideal reconstruction matrix $\Phi\psi^H$ and $V + \Delta V$ is the distorted matrix that contains all the linear static nonidealities represented by ΔV. The size of matrix $V + \Delta V$ is MN, where N is the length of y, and M is number of the overall sampled measurements for each carrier. When a single carrier signal is transmitted through the front-end, the measured output s corresponds to one of the columns of $V + \Delta V$. Based on the superposition principle, the complete reconstruction matrix $V + \Delta V$ can be measured by transmitting single carriers one at a time through the receiver. The signal reconstruction based on the optimization problem (1) employs the measured matrix $V + \Delta V$ [25].

B. Test-Bench Setup

A single front-end path, including all the circuitry of Fig. 1 except for the low-speed ADCs, was fabricated in a 90 nm CMOS process. The layout and die photo of this circuit is shown in Fig. 7. The area of a single path is $350\ \mu\mathrm{m} * 330\ \mu\mathrm{m}$. The complete proposed CS system is implemented employing eight chips on a single board.

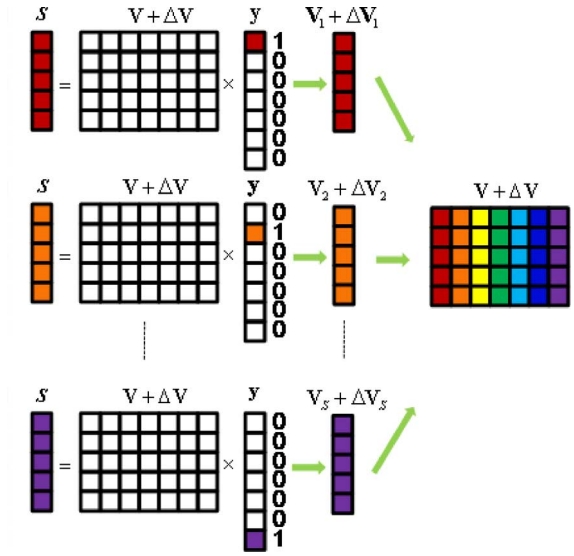

Fig. 6. Illustration of the direct training calibration.

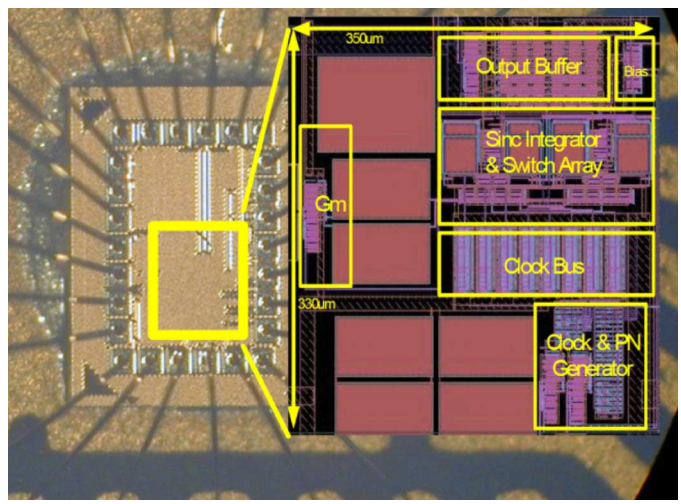

Fig. 7. Layout and die photo of one path ($350\ \mu\mathrm{m} \times 330\ \mu\mathrm{m}$) of the parallel path CS receiver.

The wideband multi-tone input signal, the master clock of the system, and the periodic triggering signal for resetting the initial state of the PN generator are generated externally. The 500 MHz multi-tone test input signal generator provides the PN master clock at 1.25 GHz with 4.13 ps rms jitter. The ADC in each path is not implemented on chip. Instead, a high-speed digital oscilloscope is employed to perform as the ADCs and capture the samples, and the signal reconstruction is done using Matlab.

C. Experimental Results

The measured output waveform of a single vector is shown in Fig. 8; these samples correspond to the integrator output shown in Fig. 2. Details of the output waveform are shown in Fig. 9, with the "read" and "reset" phases as well as sampled

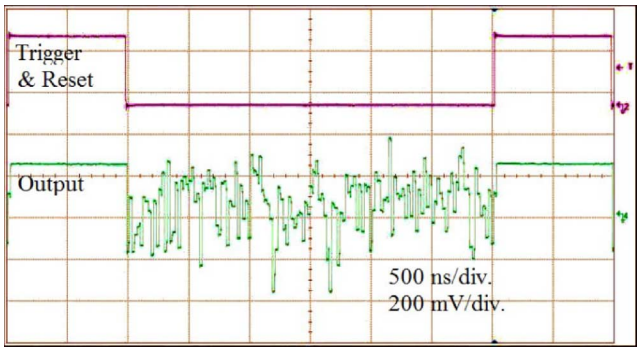

Fig. 8. Measured sampled output of a single vector.

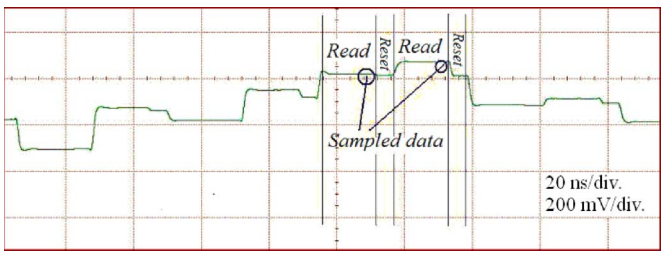

Fig. 9. Details of the receiver output waveform.

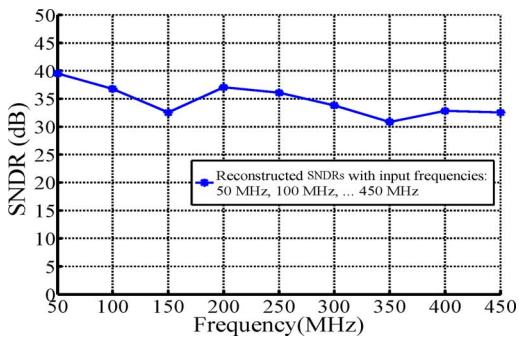

Fig. 10. Reconstructed single tone SNDR versus input tone frequency.

data phases highlighted. The voltages at the end of the "read" phases were capture by the oscilloscope for further processing.

The reconstructed signal SNDR is defined as the overall signal power over the noise power of all other undesired frequency components, including the overall integrated noise power and harmonic distortion components. When the input signal contains K tones, any energy from the other 100-K tones present in the reconstructed spectrum is considered as noise. The measured SNDR for a single tone test over the bandwidth of interest is depicted in Fig. 10. For this plot the frequency of the single test tone was swept in the 50–450 MHz frequency range. The maximum achievable SNDR with the single tone test is around 40 dB. The SNDR degrades gradually to 34 dB with increasing frequency because the front-end gain rolls off at high frequency. A predistortion block or equalizer in front of the Gm stages in Fig. 2 may help to create flat gain, although this would require additional power.

Multi-tone wideband input signals generated by an arbitrary waveform generator were also used for front-end characterization. An external magnitude equalizer was employed to create

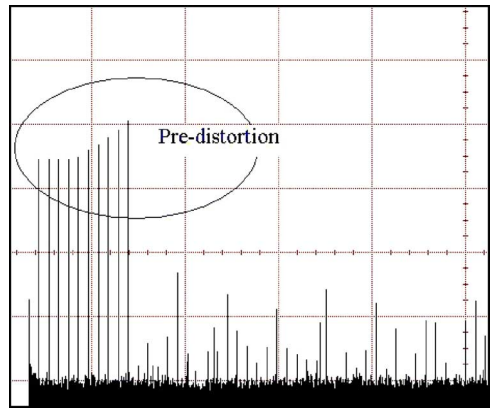

Fig. 11. Original spectrum of the multi-tone test signal.

TABLE I
TEST RESULTS WITH MULTI-TONE BPSK INPUT SIGNALS

Input Frequencies (MHz)	Reconstructed Spectrum	Reconstructed SNDR (dB)
Case 1: 50, 250, 490	Fig. 12	29.2627
Case 2: 50, 250, -490	Not shown	29.616
Case 3: 20, 70, 250, 450	Fig. 13	27.74
Case 4: 50, 150, 250, 490	Not shown	29.42
Case 5: -20, -70, 250, 450	Fig. 14	24.53

a testing environment where multi-tone input signals have unequal carrier amplitudes. A 10 tone wideband signal spanning 50~500 MHz is generated to illustrate the transfer function of the equalizer, as shown in Fig. 11.

The system was extensively characterized, with some of the test results obtained with multi-tone BPSK input signals given in Table I. In the frequency column, the negative frequency represents a carrier with its phase shifted by 180°. The selected reconstructed spectra for cases 1, 3, and 5 are shown in Figs. 12–14. It is shown that the input frequency components were successfully located by the CS algorithm. Unequal carrier amplitudes agree with the original input spectrum. Due to the higher peak-to-average ratio (PAR) of employed multi-tones input signal, the maximum achievable SNDR is about 10 dB lower than that of the single tone test. In addition to the desired signal tones, in the reconstructed signal spectrum there exist some nonideal frequency components. They are not directly related to distortions or intermodulations of the input signal tones. Instead, they are the interpretation of the noise floor and randomized OTA distortions [50]. Note that when there is phase shift of the BPSK signal, dc component may show up in the reconstructed spectrum because of mismatches of the front-end differential circuit as shown in Fig. 14. The dc component is removed before the SNDR is calculated.

Two tone tests have also been implemented to specifically measure the linearity of the Gm stages. However, no third-order intermodulations were observed in the reconstructed spectrum with the full scale input, suggesting that the Gm distortion is smaller than the architecture noise floor.

The effective number of bits (ENOBs) of the CS data acquisition system is 6.4 dB calculated from the 40 dB SNDR achieved

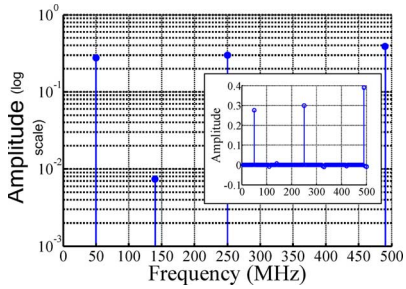

Fig. 12. Reconstructed spectrum for *Case 1*.

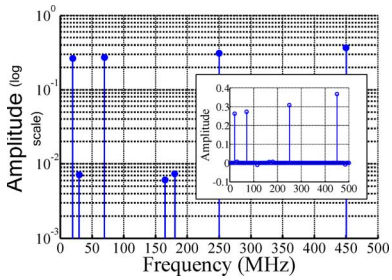

Fig. 13. Reconstructed spectrum for *Case 3*.

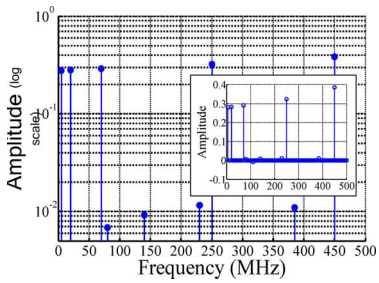

Fig. 14. Reconstructed spectrum for *Case 5*.

in the single tone test. The resolution is mainly limited by clock jitter which is further discussed in Section V. The on-chip power consumption is 54 mW taking into account Gm stages, integrators and PN generators in all eight paths. The 8 PN generators consume 24 mW. The overall power consumption of the CS system is the on-chip 54 mW plus ADC power. Though the ADC function in the prototype is performed by a digital oscilloscope, the ADC power may be estimated by the technology trend of state-of-arts ADCs [1], [22]. Low-speed and low-resolution SAR ADCs consume power less than 100 μW [49]. The estimated power of the eight required 6~7 bits ADCs with 45 MHz sampling rate consumes less than 1 mW that is negligible compared to the on-chip front-end so the overall power of the CS system is estimated as 54 mW. The FOM of the CS system from the perspective of ADC system is $\mathrm{FOM} = P/\left(2^{\mathrm{ENOB}} \cdot 1\ \mathrm{GS/s}\right) = 0.66\ \mathrm{pJ/conversion\ step}$, where P is the power consumption.

V. Comparison to Nyquist Rate Systems

A. Jitter-Limited SNR

The jitter variance of the master CLK from the instrument or the phase-locked loop (PLL) driving the PN generator is transferred to the PN waveform. In the CS system, analog blocks and ADCs are working at low speed and only the PN generator runs at relatively high speed so the PN jitter has significant impact to the system and it limits the reconstructed SNR. Studies have shown that the jitter-limited SNR depends on the spectrum distribution of the input signal [22]. After mixing with the PN sequences, a lower frequency input signal contributes more baseband power. Thus, better SNR is obtained when the input signal power is at lower frequency, and it degrades with a higher frequency input signal.

When the input signal power is equally distributed over the entire bandwidth of interest from dc to $f_{\mathrm{clk}}/2$, the jitter limited SNR is given by

$$\mathrm{SNR_j} = \frac{0.335}{\sigma_{\mathrm{j}}^2 {f_{\mathrm{clk}}}^2} \tag{2}$$

where σ_{j} is the jitter standard deviation. According to this result, SNRj is 41 dB with 4.13 ps rms jitter and 1.3 GS/s of f_{clk}, which agrees with the testing results in Section IV. In the extreme case when all the input signal power is located at the upper edge of the bandwidth ($f_{\mathrm{clk}}/2$), the worst case SNR is then computed as

$$\mathrm{SNR_j} = \frac{0.2}{\sigma_{\mathrm{j}}^2 {f_{\mathrm{clk}}}^2}. \tag{3}$$

On the other hand, the performance of Nyquist rate ADCs such as time-interleaved ADCs is limited by the sampling clock jitter that degrades the S/H performance as follows [26], [40]:

$$\begin{aligned}\mathrm{SNR_j} &= \frac{1}{\left(2\pi f_{\mathrm{signal}}\right)^2 {\sigma_{\mathrm{jitter}}}^2} \\ &= \frac{1}{\pi^2 {f_{\mathrm{Nyquist}}}^2 {\sigma_{\mathrm{jitter}}}^2}\Big|_{f_{\mathrm{signal}}=f_{\mathrm{Nyquist}}/2}.\end{aligned} \tag{4}$$

A comparison of this SNR with that of (3) shows that the conventional solutions using a S/H running at the Nyquist rate demands lower clock jitter than the proposed system.

B. System Power Consumption and FOM

Equations (3) and (4) indicate that for achieving the same system SNR, the CS system and the conventional Nyquist rate system have different requirements on clock jitter. This may be quite significant when overall system power consumption is computed. The power consumption of the PLL that generates the master clock can be considered to estimate the overall power of the complete data acquisition system. A typical PLL's FOM can be defined as

$$\mathrm{FOM_{PLL}} = 10\log\left[\left(\frac{\sigma_{\mathrm{jitter}}}{1\ \mathrm{s}}\right)^2 \cdot \left(\frac{\mathrm{Power_{PLL}}}{1\ \mathrm{mW}}\right)\right]. \tag{5}$$

Publications on low-jitter PLL designs show a common FOM value of -230 dB [27]. Power consumption of the required PLLs for recently published wideband ADC systems are estimated from (4)(5) assuming the jitter limited SNR is 5 dB better than the overall ADC ENOB. The performance of several high-frequency architectures are summarized in Table II.

TABLE II
COMPARISON OF HIGH SPEED DATA ACQUISITION SYSTEMS. NONITALICIZEDNUMBERS ARE EXPERIMENTAL RESULTS, WHILE *ITALICIZED* NUMBERS ARE FROM ESTIMATION OR SIMULATION

Design	[9]	[10]	[11] ADC (1)	[11] ADC (2)	This work sim.	This work test
Sampling Rate (GS/s)	1	0.8	1.35	1.8	*3*	1
ENOB (SNDR in dB)	8.85 (55)	9 (56)	7.7 (48.2)	7.9 (49.4)	*7 (44)*	6.4 (40)
ADC & Front-end Power (mW)	250	350	180	420	*120.8*	54
Estimated PLL Power (mW) (jitter: ps)	*98 (0.32)*	*98 (0.32)*	*37 (0.52)*	*89 (0.34)*	*40 (0.5)*	*1 (4.1)*
Power (mW)	348	448	217	509	*160.8*	55
FOM （pJ/conversion step）	0.78	1.08	0.77	1.19	*0.41*	0.66
Signal Sparsity	Arbitrary				4%	4%

$$\text{FOM} = \frac{P}{2^{ENOB} FS}$$

P is the overall system power and FS is the ADC sampling rate.

The PLL power of the CS system for comparison are estimated from (3)–(5). The proposed CS architecture outperforms the other architectures in front-end power consumption, as well as in the PLL power. As a result, the proposed CS system achieves better FOMs compared with state-of-the-art Nyquist ADCs. The FOM from testing is 0.66 pJ/conversion step. Furthermore, a better FOM can be obtained when the system is working at higher sampling rates, based on simulation results discussed in Section V-C.

C. FOM at Higher Sampling Rates

The percentage of PLL power and ADC power is more significant at higher sampling rates. In the proposed CS system the PLL and analog ADC specs are relaxed so the FOM improves at higher speed.

In our test bench presented in Section IV, the maximum bandwidth of the multi-tone signal is limited to 500 MHz by the finite bandwidth of the state-of-art instrument in lab. However, cadence spectre is employed to simulate the performance of the system with wider signal bandwidths and at higher sampling rates.

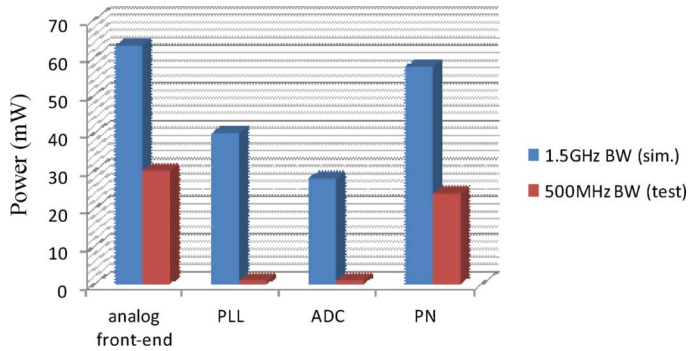

Fig. 15. Power breakdown of the proposed CS system.

In simulation a 1.5 GHz instantaneous signal bandwidth is employed. The system is set to run at 30% Nyquist rate, which is 880 MHz, and each path samples at 110 MS/s. With 0.5 ps rms jitter [48], the maximum achievable simulated reconstructed SNDR was found to be around 50 dB. The Gm stages and integrators consume 16 mW and 9.6 mW, while the PN generator consumes 57.6 mW running at 3 GHz. 110 MS/s and 8 bits ENOB ADCs are required to digitize the front-end output signal. We estimate ADC overall power consumption to be around 28 mW according to the technology trend provided in [22]. The estimated overall power consumption is 120.8 mW. In this case, the CS system equals a 3 GS/s and 7-bits ADC. The FOM is 0.41 pJ/conversion step.

Both FOMs provided by testing and simulation are provided in Table II. The power breakdown of the proposed CS system is summarized in Fig. 15.

The FOM improvement of the CS system is a result of the power consumption reduction due to the lower speed required in the baseband analog circuits including the low-speed ADCs. Furthermore, because of the sub-Nyquist operation the proposed architecture SNR is not limited by sampling jitter, but by the PN sequence generator jitter. Analysis of the impact of PN jitter (3), (4) demonstrates that the CS system is more clock jitter tolerant than conventional Nyquist samplers when targeted for the same specifications, which also saves significant amount of power from the clock synthesizer.

VI. CONCLUSION

A sub-Nyquist rate data acquisition system based on compressive sensing has been implemented in a 90 nm technology. The proposed prototype can achieve 7 bits ENOB and 3 GS/s sampling rate in simulation given a 0.5 ps clock rms jitter. Experimentally, with a 4.13 ps rms jitter of the master clock and 1 GS/s equivalent sampling rate, 40 dB peak SNDR is achieved with single tone input and 24–30 dB peak SNDR is obtained when multi-tone input signals are employed.

The proposed CS front-end achieves a better FOM compared with state-of-the-art Nyquist ADCs when dealing with sparse signals. The design bottleneck is the PN generator that works at the Nyquist rate and has considerable power consumption. Leveraging CMOS technology scaling is expected to alleviate this issue. In summary, the overall FOM is improved, especially when systems are pushed to work at higher frequencies, as the

cost of increasing the PN generator frequency is much less than pushing Nyquist ADC or PLL performance to the limits of the process technology.

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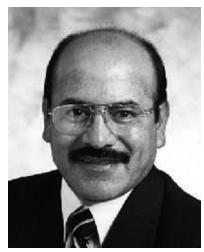

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