## 7.5 A Ring-Resonator-Based Silicon Photonics Transceiver with Bias-Based Wavelength Stabilization and Adaptive-Power-Sensitivity Receiver

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Silicon photonic links based on ring-resonator devices provide a unique opportunity to deliver distance-independent connectivity, whose pin-bandwidth scales with the degree of wavelength-division multiplexing. However, reliability and robustness are major challenges to widespread adoption of ring-based silicon photonics. In this work, a CMOS photonic transceiver architecture is demonstrated that incorporates the following enhancements: transmitters with independent dual-edge pre-emphasis to compensate for modulator bandwidth limitations; a bias-based tuning loop to calibrate for resonance wavelength variations; and an adaptive sensitivity-bandwidth receiver that can self-adapt for in-situ variations in input capacitance, modulator/photodetector performance, and link budget.

Carrier-injection silicon ring modulators are capable of high extinction ratio operation in a low area footprint. For example, the 5μm diameter devices used in this work exhibit a quality factor of ~8000 [1]. However, operating speed is limited by relatively slow carrier dynamics, such that the device exhibits different time constants for rising and falling edges. This work introduces CMOS drivers that independently control the rising- and falling-edge pre-emphasis levels in order to compensate for this non-linear transient behavior. As shown in Fig. 7.5.1, two driver versions are developed. A differential driver, with 0V average bias level, provides a $4V_{pp}$ output swing to allow for high-speed operation, while a single-ended driver provides a $2V_{pp}$ output swing on the modulator cathode and introduces bias-tuning DAC on the anode for an adjustable DC-bias level. Both drivers use pulsed-cascode output stages with only thin-oxide core devices [2] to reliably provide a per-terminal output swing of twice the nominal 1V supply. Each output driver consists of a main driver, positive-edge and negative-edge pre-emphasis pulse drivers in parallel. Tunable delay cells allow for independent control of the rising and falling edge pre-emphasis intensity. Figure 7.5.3 shows 5Gb/s $2^7$-1 PRBs optical eye diagrams for the $4V_{pp}$ driver. Without pre-emphasis the eye is completely closed, while enabling pre-emphasis allows for a healthy eye margin. Note that the current experimental results are limited by the wire-bonded modulator BW, as the CMOS transmitter is electrically verified up to 9Gb/s.

One problem with ring resonators is that their resonance is sensitive to temperature variation and fabrication tolerances. A closed-loop adaptation scheme is therefore necessary to tune the ring to resonate at the input laser wavelength. Figure 7.5.2 shows the device behavior when the bias voltage increases, such that the resonance frequency blue shifts due to the accumulation of free carriers in the ring waveguide. In this work, a bias tuning method is used within the $2V_{pp}$ driver, allowing for both improved tuning power efficiency and speed relative to heater-based tuning. A 9b segmented bias DAC that uses a coarse 3b non-linear R-string DAC to match the p-i-n I-V characteristics and a fine 6b linear R-2R DAC, provides the adjustable bias to tune the modulator. This bias DAC is part of an automatic control loop that also includes a monitor photodetector, low-bandwidth TIA, clocked comparator, finite-state machine (FSM), and a reference DAC. Due to the unavailability of modulators with drop ports, the bias-tuning-loop operation is demonstrated by monitoring the power of the through port. The loop starts at an initial reference voltage, tunes the ring resonance through the bias-tuning DAC to produce an output equal to this reference voltage, and then steps the reference voltage down until the minimum output is reached to guarantee maximum modulation depth. This loop uses digital controls to also allow operation with devices that have drop ports, eliminating any power splitting necessary to monitor the through port. Figure 7.5.3 shows the effectiveness of this bias-based control, with 500Mb/s eye diagrams displaying >10dB extinction ratio at the input wavelength of 1286.93nm. The maximum tuning power is 425μW for a resonance range of 0.22nm, which can be leveraged as a fine-control in a dual thermal/bias tuning scheme to improve overall tuning efficiency.

The receiver architecture consists of a quarter-rate forwarded-clock scheme to produce the receive-side data sampling clocks, with one clock channel bundled with 4 optical channels. Both data and clock receivers use the same inverter-based TIA [3], shown in Fig. 7.5.4. An offset control loop biases the inverters around the trip-point for maximum gain by subtracting the average photocurrent from the input node. The clock receiver further amplifies the TIA output to full-scale by a main amplifier that also contains a duty-cycle distortion loop. A multi-stage digitally-controlled capacitive delay line proceeds the main amplifier, providing approximately 130ps skew adjustment between the clock and data channels. This clock is then locally converted from singled-ended to differential before being injected by AC-coupling into a 2-stage differential oscillator. This injection-locked oscillator then generates quadrature phase clocks that are distributed to all 4 quantizers within a single channel.

Each data-channel TIA output is quantized and 1:4 demuxed by quadrature-clocked comparators whose offsets are digitally calibrated to maximize receiver sensitivity. Due to the large variations in fiber coupling and photodiode capacitance, some channels in a multi-channel photonic link system may intrinsically require higher sensitivity or bandwidth. However, using a single fixed TIA design to cover the worst-case link budget results in conservative overdesign and excessive power consumption. This work introduces a self-adaptive receiver that can trade-off TIA sensitivity for power/performance. An extra $5^{th}$ comparator with a 6b programmable threshold is introduced that serves as an eye monitor, setting the minimum voltage margin needed to correctly slice the input signal for a required bit-error rate. By comparing its output with the normal data comparator on the same clock phase, eye-closure can be detected before a bit-error actually occurs. This information is used to control a 6b R-2R voltage DAC that sets the LDO-generated TIA supply voltage to the minimum level required to achieve the sensitivity and bandwidth for a given BER. A software-controlled outer loop monitors the bit-error rate, adjusts the eye-monitor comparator threshold via a serial test interface, and adjusts the voltage margin. 8Gb/s optical measurements (Fig. 7.5.5) show that for a BER = $10^{-15}$, relaxing the input sensitivity by ~2dB enables the TIA supply to be decreased by 5%, resulting in a 14% reduction in TIA power.

The optical transceiver is fabricated in a GP 65nm CMOS process. Both the ring resonator modulators and discrete p-i-n photodetectors are attached with wire-bonds, as shown in Fig. 7.5.7. Figure 7.5.6 shows the transceiver performance summary. The $4V_{pp}$ transmitter achieves 808fJ/bit at 5Gb/s, while the $2V_{pp}$ transmitter demonstrates bias-based resonator tuning with a 12% power overhead. The receiver achieves -18dBm sensitivity at 10Gb/s with an emulated electrical input, and -12.7dBm sensitivity for an 8Gb/s optical input, limited by the wirebond integration and the photodiode with higher capacitance. With an 8Gb/s optical input, the receiver energy efficiency is 275fJ/bit.

*Acknowledgements:*
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*References:*
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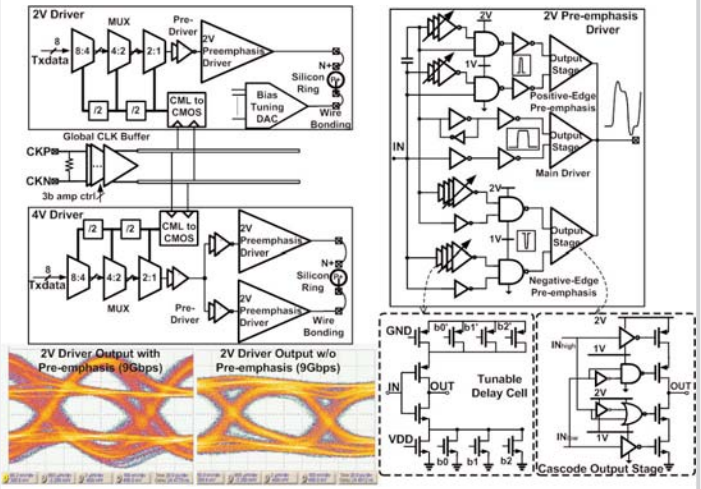


Figure 7.5.1: Block diagram of the ring modulator transmitter and detailed driver schematic.

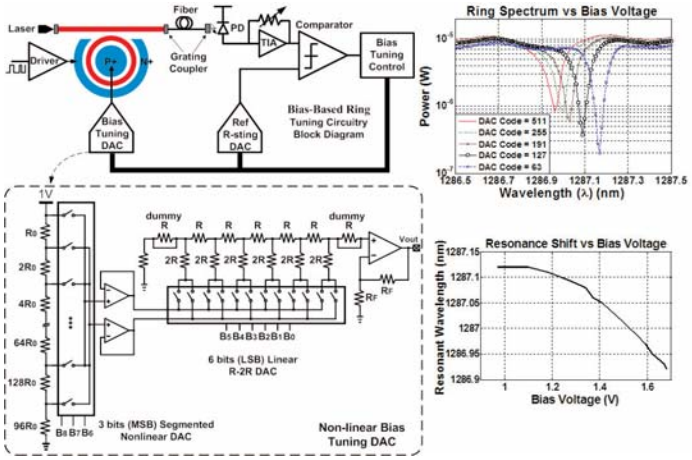


Figure 7.5.2: Ring modulator tuning circuit and ring spectrum versus bias tuning DAC output.

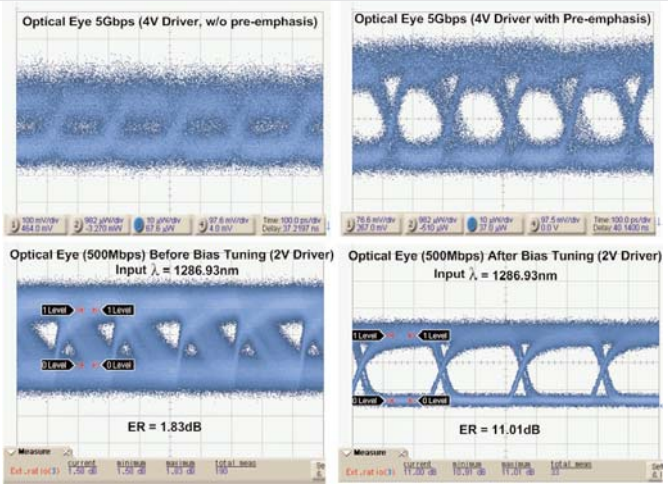


Figure 7.5.3: 5Gb/s optical eye-diagram using the 4Vpp swing driver with & without pre-emphasis outputs and 500Mb/s optical eye-diagrams using the 2Vpp swing driver demonstrating the automatic bias tuning stabilizing to 1286.93nm.

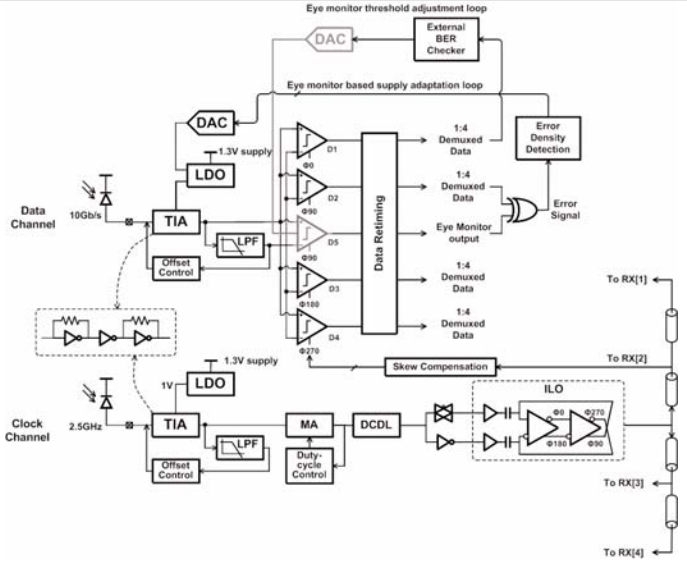


Figure 7.5.4: Receiver block diagram.

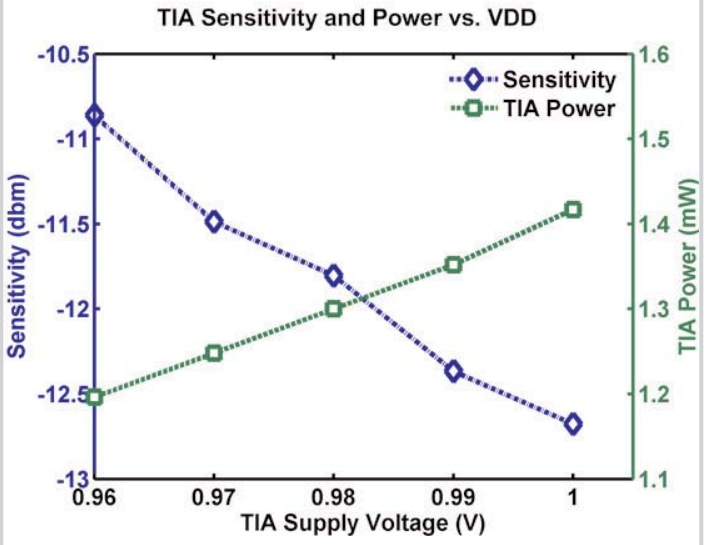


Figure 7.5.5: TIA sensitivity and power consumption versus VDD.

| | This Work | [3] | [4] |
|---|---|---|---|
| **Ring Radius** | 2.5μm | 12μm | 7.5 μm |
| **Ring Mode** | Carrier-injection | Depletion | Depletion |
| **Ring Quality Factor (Q)** | ~8,000 | ~15,000 | ~13,000 |
| **Technology** | 65nm CMOS | 40nm CMOS | 130nm CMOS SOI |
| **Supply Voltage** | 1V, 2V, 2.5V | 1V, 1.3V, 2V | 1.2V/-1.2V |
| **TX Optical Data Rate** | 5Gb/s ($4V_{pp}$ TX) | 10Gb/s | 25Gb/s |
| **TX Electrical Data Rate** | 9Gb/s | 10Gb/s | 25Gb/s |
| **ER** | >10dB | 7dB | 6.9dB |
| **Tuning Method** | Voltage Bias | Thermal | N/A |
| **Wavelength Tuning Range** | 0.22nm | 1.6nm | N/A |
| **Area** | | | |
| $4V_{pp}$ Transmitter | $0.041mm^2$ | $0.00012mm^2$ | N/A |
| $2V_{pp}$ Transmitter (include Bias Tuning) | $0.08mm^2$ | | |
| **TX Power** | | | |
| $4V_{pp}$ Transmitter | 4.04mW | | |
| $2V_{pp}$ Transmitter (include Bias Tuning) | 3.57mW | 1.35mW | 207.6mW |
| Tuning | 0.43mW | 1.25mW | |
| **RX Input Capacitance** | >200fF | 40~60fF | 20fF |
| **RX Sensitivity** | | | |
| Optical input data | -12.7dBm @ 8Gb/s | -15dBm @ 10Gb/s | -6dBm @ 10Gb/s |
| Optical input clock | -18dBm @ 2GHz | | |
| Electrical input data | <16uA@ 10Gb/s | | |
| Electrical Input clock | <8uA@2.5GHz | | |
| **RX Power** | | | |
| TIA | 1.42mW | 3.95mW | 48mW |
| Comparator and others | 0.78mW | | |
| **RX Area** | | | |
| Clock RX | $0.032mm^2$ | $0.008mm^2$ | N/A |
| Data RX | $0.036mm^2$ | | |

Figure 7.5.6: Transceiver performance summary and comparison.

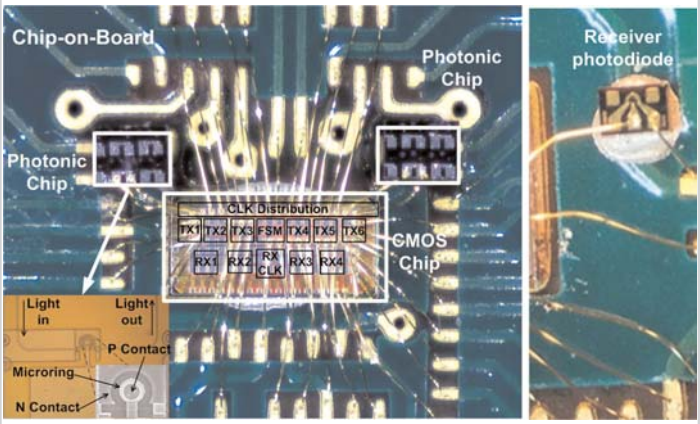


**Figure 7.5.7: Micrograph of the CMOS transceiver, bonded optical ring resonator and photodiode.**


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